300W Isolated DC-DC Converter

Design Guide

RD024-DGUIDE-03

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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1. Introduction

This design guide describes guidelines for the circuit design and layout of a 300W isolated DC-DC converter. Refer to the reference guide for the specifications, operating method, and electrical performance data of this converter.

Components marked “Not Mounted” in the Bill of Materials (BOM) are not mounted on the PCB even if component are shown in the circuit diagram. The PCB reserves mounting space for them necessary to modify circuit constants when designing a circuit.

1.1. Power MOSFETs used

Toshiba offers the U-MOSVIII and U-MOSIX low-voltage MOSFET series suitable for primary (main switch) and secondary (synchronous rectification) sides of DC-DC converters. Toshiba provides MOSFETs with wide range of V_{DSS} of 30V to 250V and various on-resistance types in each V_{DSS} class. Therefore, you can find suitable MOSFETs when designing a DC-DC converter, according to its circuit topology, input and output voltages, output specification, and the locations of MOSFETs on circuit (primary or secondary side). Figure 1.1 shows the lineup of the U-MOSVIII and U-MOSIX MOSFET series.

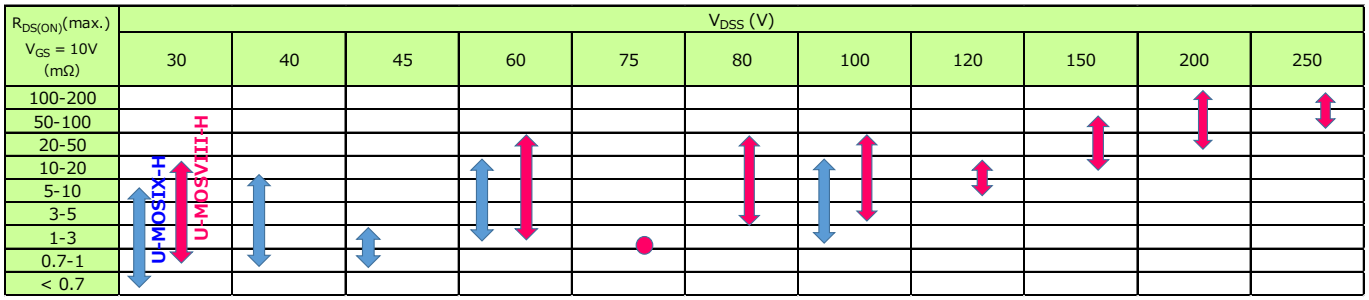

Figure 1.1 Product lineup of the U-MOSVIII and U-MOSIX MOSFET series

The following describes the MOSFETs used in this 300W isolated DC-DC converter. Because this converter has an input voltage range of 36 to 75V, an output voltage of 12V, and a phase-shifted full-bridge topology, MOSFETs with 100V of V_{DSS} are selected for both the primary and secondary sides. The primary side uses the TPN1200APL with an excellent balanced drive and conduction losses, whereas the secondary side uses the TPH3R70APL with low on-resistance, prioritizing a reduction in conduction loss.

TPN1200APL

For the main switch on the primary side

V_{DSS} = 100V, $R_{DS(ON)}$ = 12mΩ (max.) at V_{GS}=10V, TSON Advance package

Balanced drive and conduction loss are achieved by applying the latest U-MOSIX-H process.

TPH3R70APL

For the synchronous rectifier on the secondary side

V_{DSS} = 100V, $R_{DS(ON)}$ = 3.7mΩ (max.) at V_{GS}=10V, SOP Advance package

Low power loss in synchronous rectification is achieved by applying the latest U-MOSIX-H process.

2. Circuit design

This section describes major considerations for the circuit design of this 300W isolated DC-DC converter.

2.1. Phase-shifted full-bridge (PSFB) circuit

The 300W isolated DC-DC converter generates a 12V output with a phase-shifted full-bridge (PSFB) circuit. The PSFB circuit alternately turns on and off the high-side and low-side MOSFETs of each arm on the primary side with a duty cycle of 50% and adjusts the arm-to-arm turn-on timing (phase) to regulate the output voltage. To prevent cross conduction, a dead time is inserted between the switching of the high-side and low-side MOSFETs. These MOSFETs achieve zero-voltage switching (ZVS) thanks to resonance during switching transitions. Zero-voltage switching helps reduce switching loss, making it possible to create a high-efficiency power supply. This converter uses the LM5046 PSFB PWM controller from Texas Instruments to constitute a PSFB circuit. This subsection describes the basic design of the PSFB circuit in this converter. For the detailed peripheral circuit design of the PSFB PWM controller, refer to the LM5046 datasheet and other related documents from Texas Instruments. Refer to the Reference Guide (RD024-RGUIDE-03) for the detailed specifications of this converter, RD024-SCHEMATIC-01 for circuit diagrams, and RD024-BOM-01 for a bill of materials.

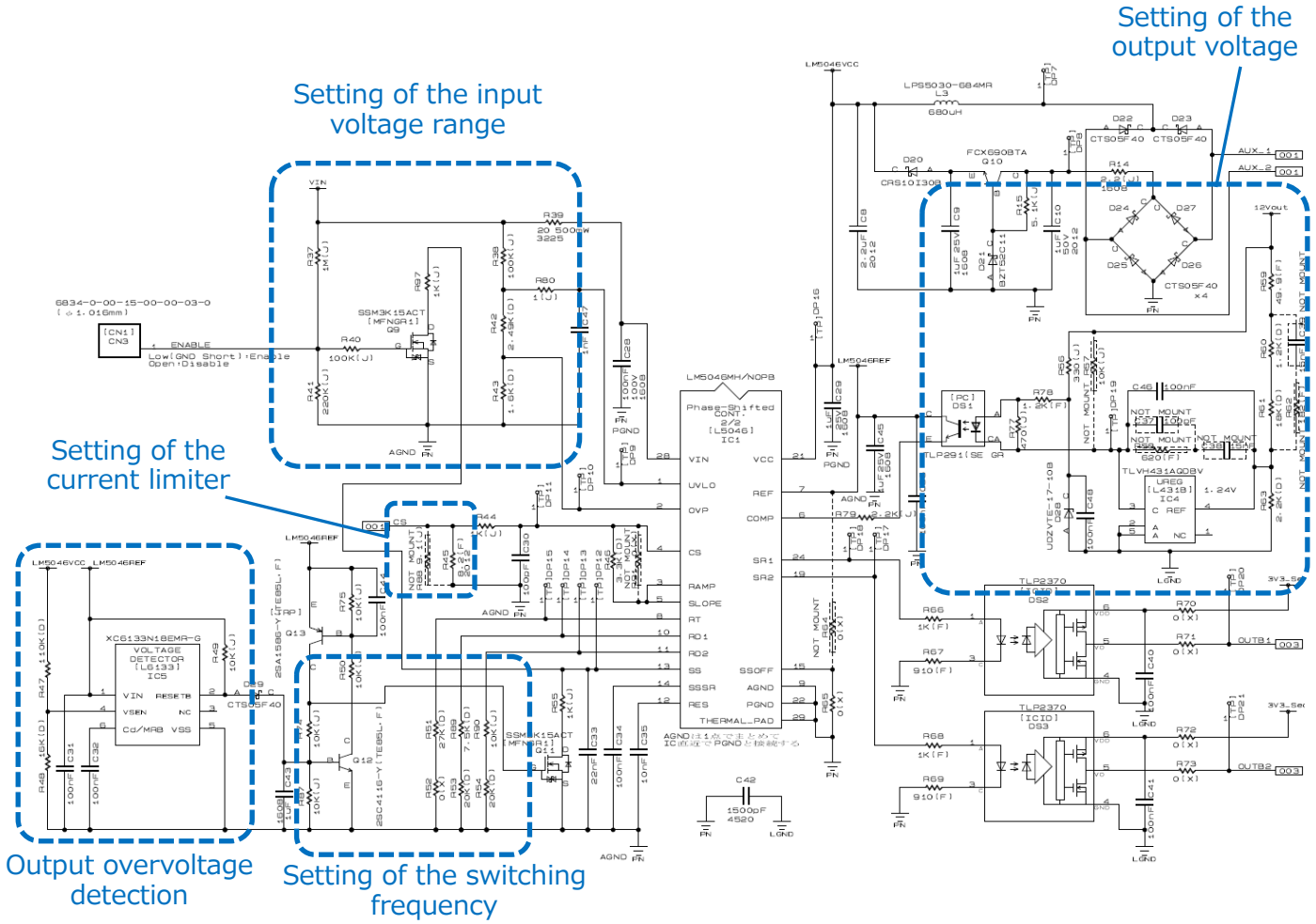

Figure 2.1 PSFB circuit 1 (around the controller)

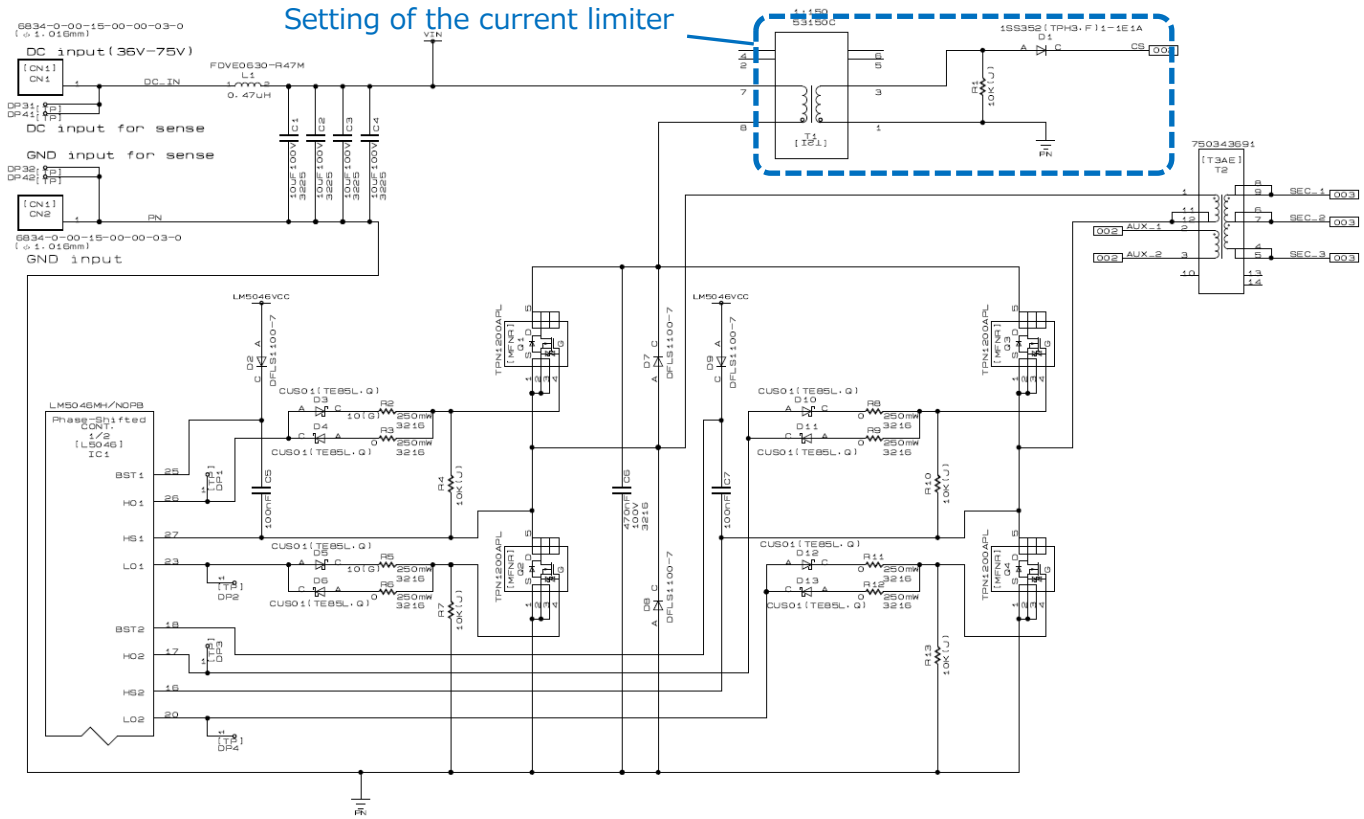

Figure 2.2 PSFB circuit 2 (around the MOSFET bridge on the input side)

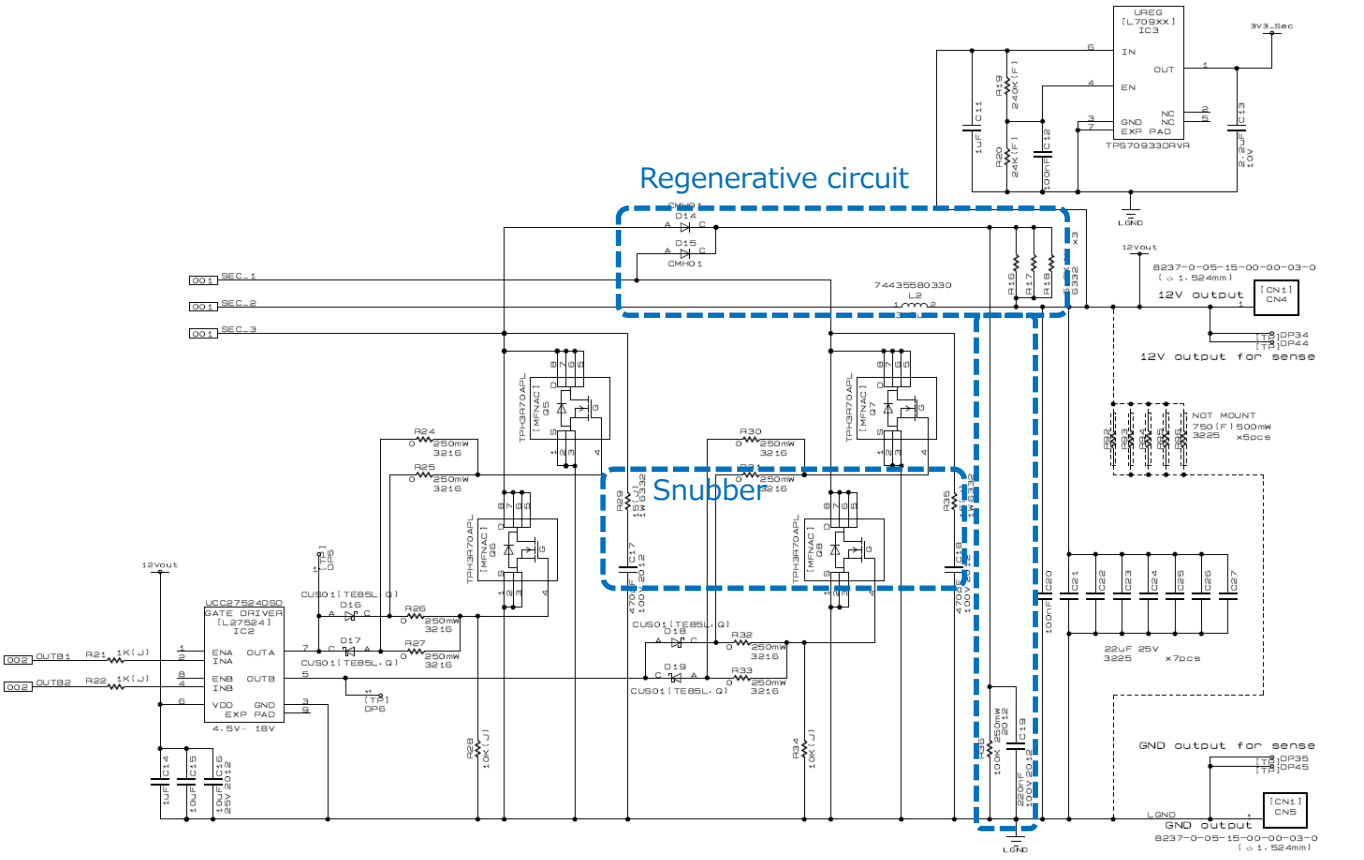

Figure 2.3 PSFB circuit 3 (around synchronous rectification MOSFETs on the output side)

Setting the minimum input operating voltages

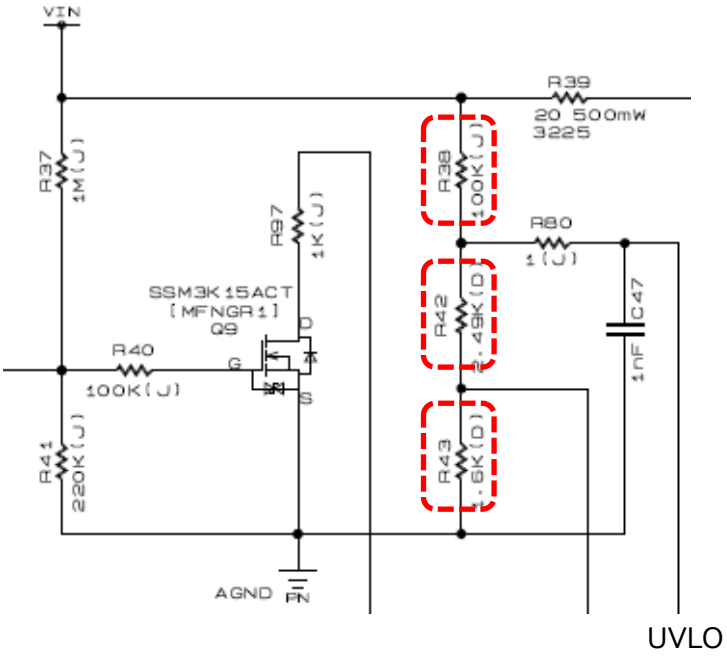

Figure 2.4 Setting the input voltage range

The input operating voltage range of this converter can be programmed with external resistors (R38, R42, and R43). The input voltage (V_{in}) is divided by R38, R42, and R43, and the divided voltage is fed to the UVLO pin of the PSFB PWM controller to program the minimum input operating voltages ($V_{in\_min\_on}$ and $V_{in\_min\_off}$). The UVLO pin voltage is generated by this divided voltage and voltage generated by an internal hysteresis current (20μA). The PSFB PWM controller enters the active mode when the UVLO pin voltage reaches 1.25V. The internal hysteresis current is disabled once the PSFB PWM controller enters the active mode. The PSFB PWM controller shuts down when the UVLO pin voltage drops below the 1.25V threshold. The minimum input operating voltages ($V_{in\_min\_on}$ and $V_{in\_min\_off}$) are calculated by following equations:

$$\boldsymbol{V_{in\_min\_on}(V) = 1.25(V) \times \frac{(R38 + R42 + R43)}{(R42 + R43)} + 20(\mu A) \times R38}$$

$$\boldsymbol{V_{in\_min\_off}(V) = 1.25(V) \times \frac{(R38 + R42 + R43)}{(R42 + R43)}}$$

As shown in Figure 2.4, this converter uses a 100kΩ resistor for R38, a 2.49kΩ resistor for R42, and a 1.6kΩ resistor for R43, setting $V_{in\_min\_on}$ and $V_{in\_min\_off}$ to 33.81V and 31.81V respectively. Figure 2.5 shows the operating modes of the PSFB PWM controller, depending on the relationship between the input voltage (V_{in}) and the UVLO pin voltage.

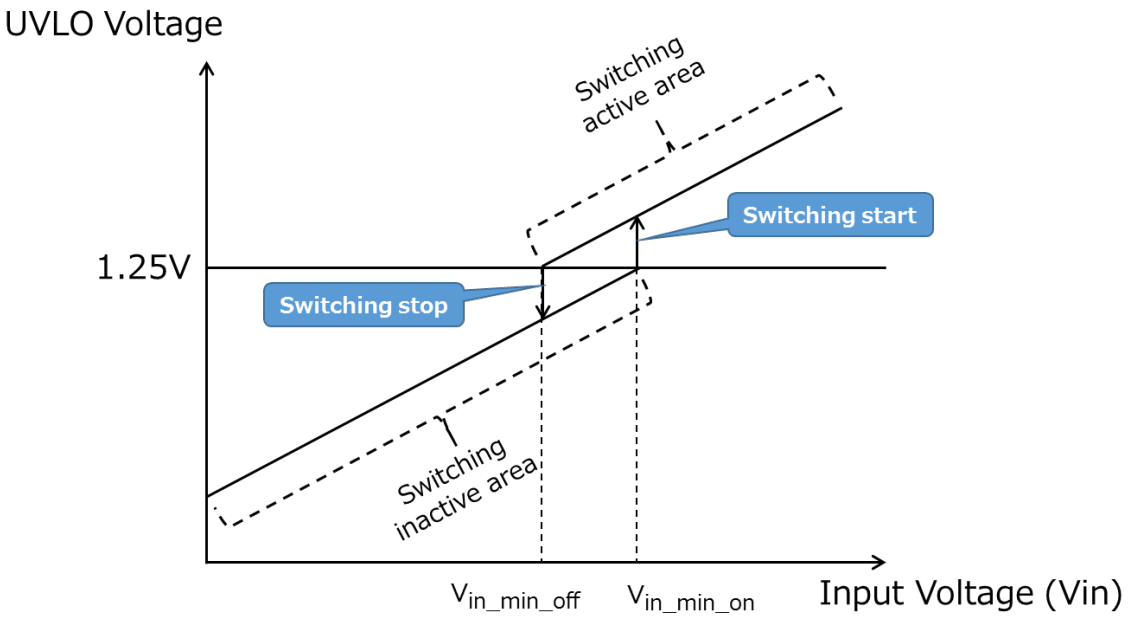

Figure 2.5 Operating modes according to the input power source and UVLO pin voltages

Setting the maximum input operating voltages

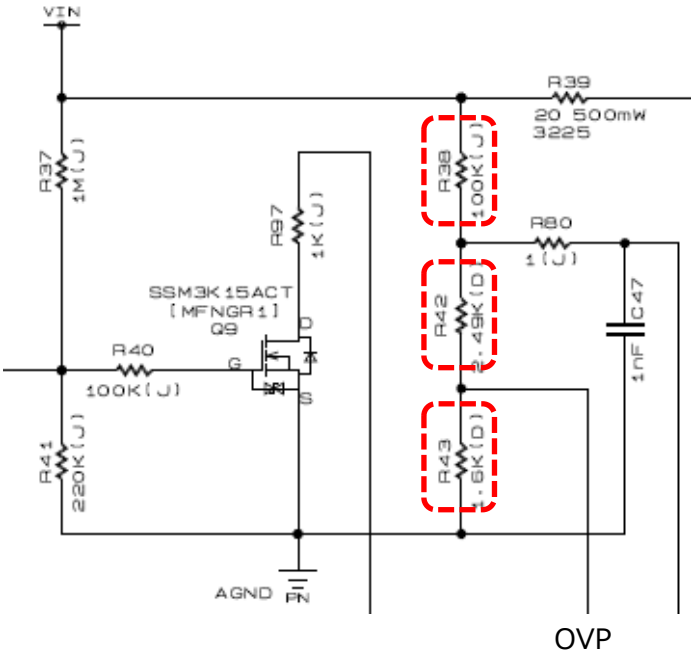

Figure 2.6 Setting the input voltage range

The input operating voltage range of this converter can be programmed with external resistors (R38, R42, and R43). The input voltage (V_{in}) is divided by R38, R42, and R43, and the divided voltage is fed to the OVP pin of the PSFB PWM controller to program the maximum input operating voltages ($V_{in\_max\_on}$ and $V_{in\_max\_off}$). The OVP pin voltage is generated by this divided voltage. The PSFB PWM controller shuts down when the OVP pin voltage reaches 1.25V. Then, the hysteresis current is enabled, and the PSFB PWM controller enters active mode when the UVLO pin voltage drops below 1.25V. The maximum input operating voltages ($V_{in\_max\_on}$ and $V_{in\_max\_off}$) are calculated by following equations:

$$\boldsymbol{V_{in\_max\_off}(V) = 1.25(V) \times \frac{(R38 + R42 + R43)}{(R43)}}$$

$$\boldsymbol{V_{in\_max\_on}\,(V) = 1.25(V) \times \frac{(R38 + R42 + R43)}{(R43)} - 20(\mu A) \times (R38 + R42)}$$

As shown in Figure 2.6, this converter uses a 100kΩ resistor for R38, a 2.49kΩ resistor for R42, and a 1.6kΩ resistor for R43, setting $V_{in\_max\_on}$ and $V_{in\_max\_off}$ to 81.32V and 79.27V respectively. Figure 2.7 shows the operating modes of the PSFB PWM controller, depending on the relationship between the input voltage (V_{in}) and the OVP pin voltage.

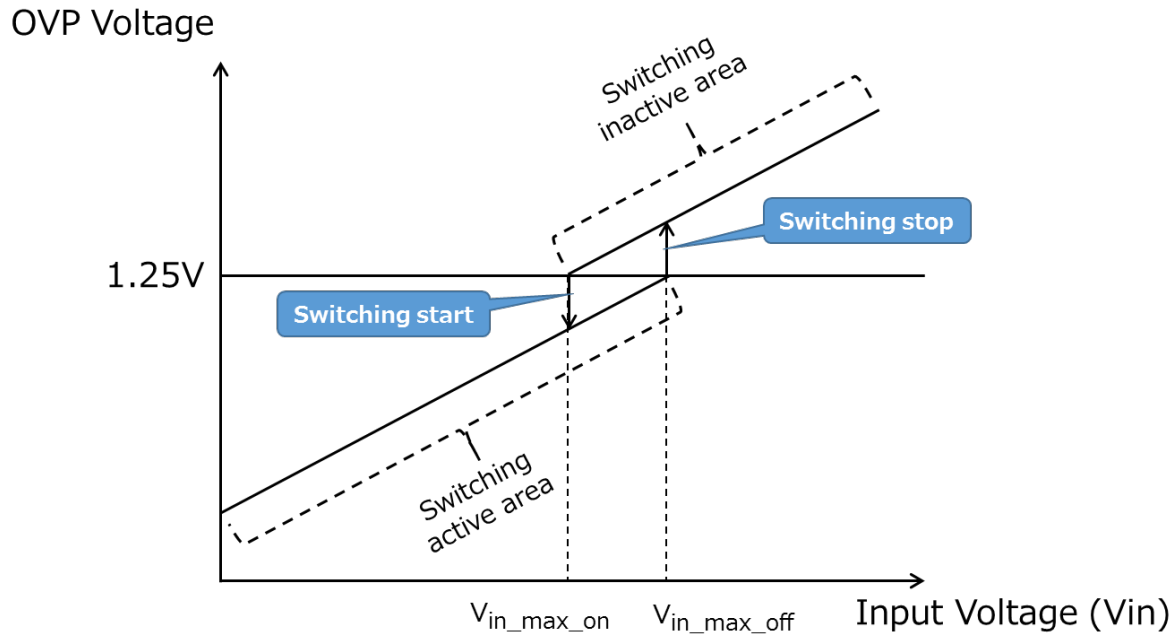

Figure 2.7 Operating modes according to the input power source and OVP pin voltages

Setting the output voltage

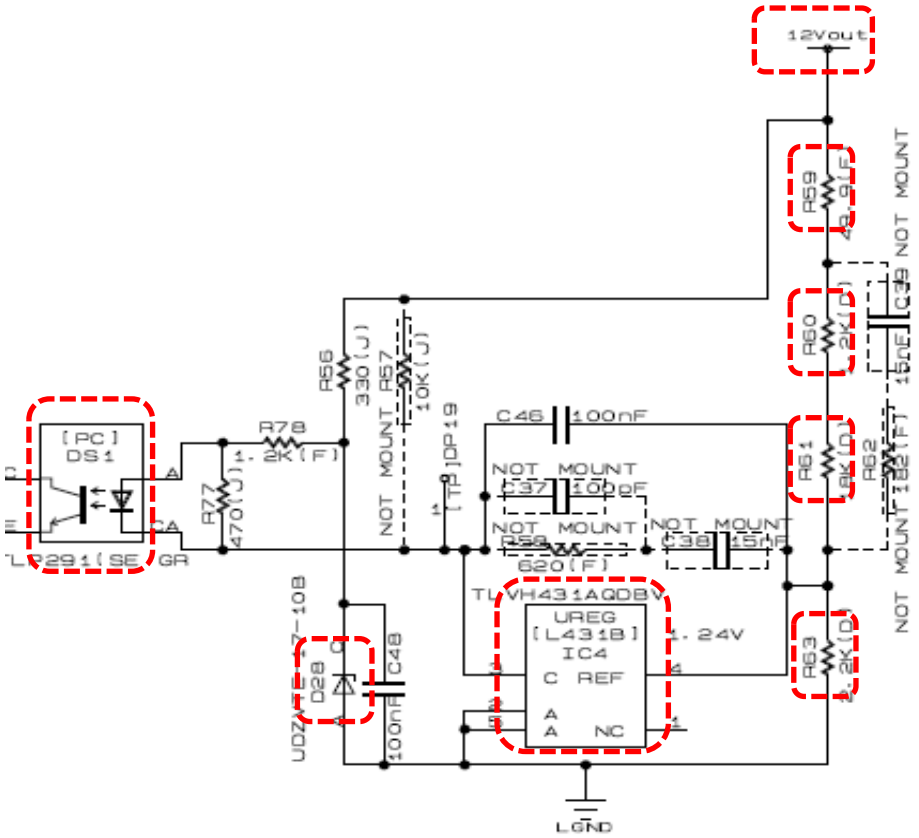

Figure 2.8 Setting the output voltage

The output voltage (V_{out}) of the PSFB circuit can be programmed with external resistors (R59, R60, R61, and R63) and a shunt regulator (IC4). The output voltage from the PSFB circuit is divided by resistors (R59, R60, R61, and R63). The shunt regulator (TLVH431AQDBV) regulates the photocoupler (DS1) current so that the divided voltage equals the reference voltage (V_{REF}). The PSFB PWM controller maintains the output voltage (V_{out}) at a constant level according to the feedback current from the photocoupler (DS1). The output voltage (V_{out}) is calculated by following equation:

$$V_{out}\ (V) = \frac{V_{REF}(V) \times (R59 + R60 + R61 + R63)}{R63}$$

As shown in Figure 2.8, this converter uses a 49.9Ω resistor for R59, a 1.2kΩ resistor for R60, a 18kΩ resistor for R61, and a 2.2kΩ resistor for R63, setting the output voltage (V_{out}) to 12.09V. A Zener diode (D28) is used to stabilize the photocoupler (DS1) power supply in order to prevent output oscillation.

Setting the switching frequency

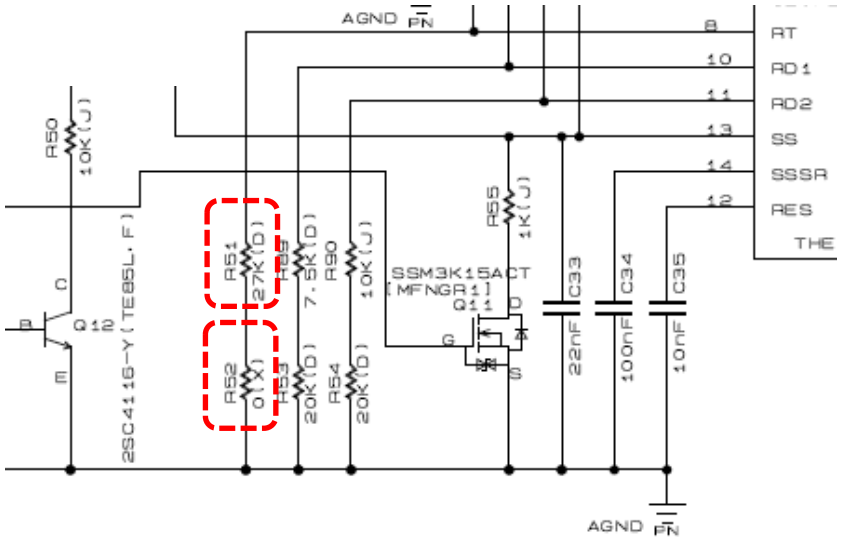

Figure 2.9 Setting the switching frequency

The switching frequency (f_{PWM}) of the PSFB circuit can be programmed with external resistors (R51 and R52). It is calculated by following equation:

$$f_{PWM}(Hz) = \frac{1}{\left(R51(\Omega) + R52(\Omega)\right) \times 1 \times 10^{-10}}$$

As shown in Figure 2.9, this converter uses a 27kΩ resistor for R51 and a 0kΩ resistor for R52, setting the switching frequency (f_{PWM}) to 370kHz. The PSFB PWM controller switches the left and right arms of the MOSFET bridge on the input side (Q1-Q2 and Q3-Q4) at half the frequency of f_{PWM}. As a result, a ripple voltage at a frequency of f_{PWM} is generated in the output.

Current limiter

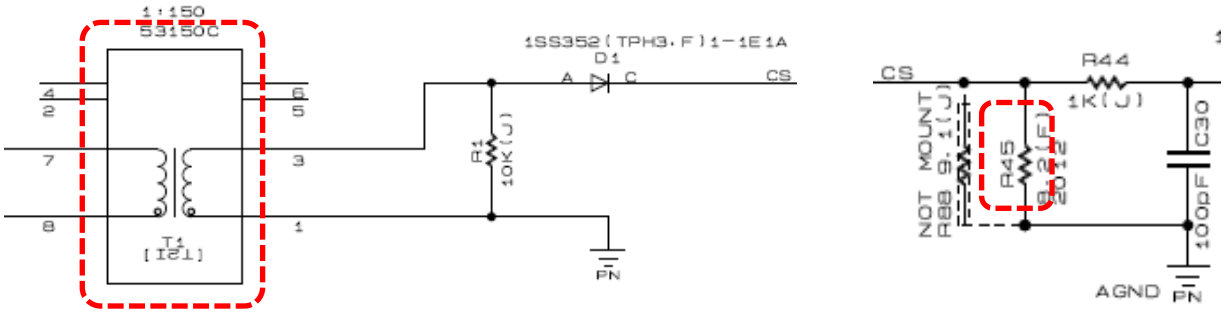

Figure 2.10 Current limiter

If the voltage of the CS pin of the PSFB PWM controller exceeds the current limit threshold of 0.75V, the PSFB PWM controller controls the MOSFET bridge on the input side to limit the current. Figure 2.2 shows the PSFB circuit peripheral aria of the MOSFET bridge on the input side. The current limiting level (I_limit) is determined by the current limit threshold (0.75V), the value of the current-sensing resistor (R45), and the turns ratio of the current transformer (T1). The current limiting level is calculated by following equation:

$$I\_limit = \frac{0.75}{R45 \times (transfomer\ turns\ ratio)}$$

As shown in Figure 2.10, this converter uses an 8.2Ω resistor for R45 and a transformer with a turns ratio of 1:150 for T1, setting the current limiting level to 13.7A.

Gate drive circuit

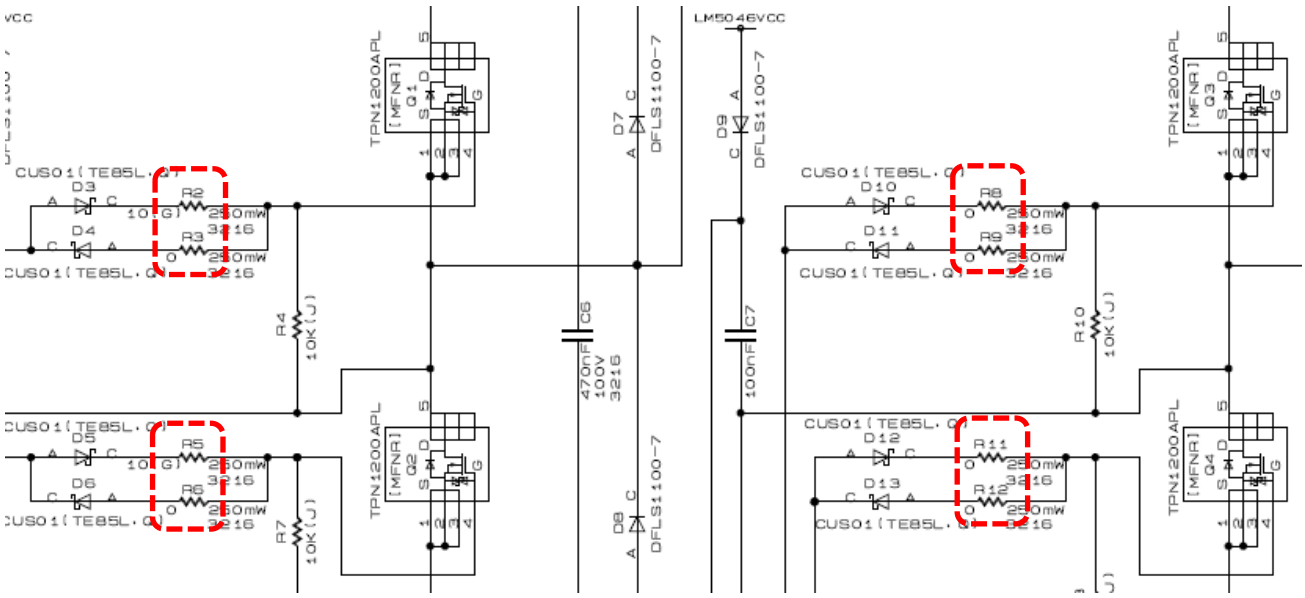

Figure 2.11 Gate drive circuit

The gate drive circuit affects power efficiency and electromagnetic interference (EMI). Generally, power efficiency and EMI have a relation of a trade-off. Designing a gate drive circuit is a balancing act between power efficiency and EMI. The PSFB circuit exhibits low EMI due to zero-voltage switching. However, if EMI is considered to be caused by the presence of a hard-switching region, determine whether increasing the values of series gate resistors for the Q1 to Q4 MOSFETs (R2, R3, R5, R6, R8, R9, R11, and R12) helps reduce EMI. The balance between power efficiency and EMI can be adjusted separately for MOSFET turn-on and turn-off transitions. As shown in Figure 2.11, this converter uses 10Ω resistors for R2 and R5 and uses 0Ω resistors for R3, R6, R8, R9, R11, and R12.

Transformer

When the “on” duty cycle on the synchronous rectifier side of a transformer is set to 60% in the steady state of the PSFB circuit, a rectangular wave with an amplitude of 20V or so is required on the secondary side because the output voltage is 12V. Since the typical input voltage of this converter is 48V, a transformer (T2) with a turns ratio of 5:2:2:2 (a center-tapped transformer with an auxiliary winding) is selected. As a result, T2 generates a 19.2V rectangular wave on the secondary side. In addition, the isolation voltage between the primary and secondary sides, an increase in the winding temperature, flux saturation, core loss, and other factors should be fully considered. Refer to the bill of materials (RD024-BOM-01) for the specifications of the transformer used in this converter.

Also, this converter uses the leakage inductance of the transformer to activate zero-voltage switching. If LC resonance of leakage inductance is insufficient, zero-voltage switching is not

activated, and may cause a low power efficiency, an increase in EMI, and other problems. In such cases, use a resonance coil to achieve zero-voltage switching over a wide load range.

Output capacitor

The output capacitor (C_{out}) is selected so that the output voltage ripple (V_{ripple}) meets the required specification. The following ripple voltages combine to generate a ripple in the output voltage (V_{ripple}):

1. Ripple voltage (V_{ripple_ESR}) generated by a ripple current (ΔI) and the equivalent series resistance (ESR) of the output capacitor
2. Ripple voltage (V_{ripple_Cap}) generated by a ripple current (ΔI), the output capacitor (C_{out}), and the switching frequency (f_{PWM})
3. Ripple voltage (V_{ripple_ESL}) generated by the switching voltage (V_{sw}) and the equivalent series inductance (ESL) and inductance (L) of the output capacitor

These ripple voltages are calculated by following equations:

$$V_{ripple\_ESR} = \Delta I \times ESR$$

$$V_{ripple\_Cap} = \frac{\Delta I}{8 \times C_{out} \times f_{PWM}}$$

$$V_{ripple\_ESL} = \frac{V_{sw} \times ESL}{L}$$

where,

$$\Delta I = \frac{(V_{SW} - V_{out}) \times V_{out}}{V_{SW} \times f_{PWM} \times L}$$

Suppose that the switching voltage (V_{sw}) is 19.2V, the output voltage (V_{out}) is 12.09V, the switching frequency (f_{PWM}) is 370kHz, and the inductance (L) is 3.5μH. Then, the ripple current (ΔI) is calculated to be 3.45A.

Suppose that that the equivalent series resistance (ESR) is 0.29mΩ (2mΩ for seven capacitors at 500kHz), the output capacitor (C_{out}) is 50.4μF (seven 7.2μF capacitors at 12VDC and 0.01VAC), the equivalent series inductance (ESL) of an output capacitor is 0.14nH (1nH for seven capacitors), and the inductance (L) is 3.5μH. Then, V_{ripple_ESR} = 0.99mV, V_{ripple_Cap}=23.1mV, and V_{ripple_ESL} = 1.2mV. Because V_{ripple_Cap} is out of phase from V_{ripple_ESR} and V_{ripple_ESL}, adding them up does not provide V_{ripple}. However, the sum of V_{ripple_Cap}, V_{ripple_ESR}, and V_{ripple_ESL} can be used as a guide for the output voltage ripple (V_{ripple}) .

Adjust C_{out}, ESR, and ESL of the output capacitor so that the output voltage ripple meets the required specification. In addition,

1. Determine that undershoot and overshoot at the output terminal do not exceed the specified voltage when the load rappidly fluctuates.
2. Determine that the ripple current through the output capacitor does not exceed the acceptable limit.
3. Consider the tolerance and aging degradation of the output capacitor.

Reducing the surge voltage on synchronous rectification MOSFETs

The drain-source voltage of the synchronous rectification MOSFETs (Q5, Q6, Q7, and Q8) on the secaondary side is affected by surge voltage when power is transmitted from the primary side to the secondary side. This converter has regenerative and snubber circuits to reduce the surge voltage.

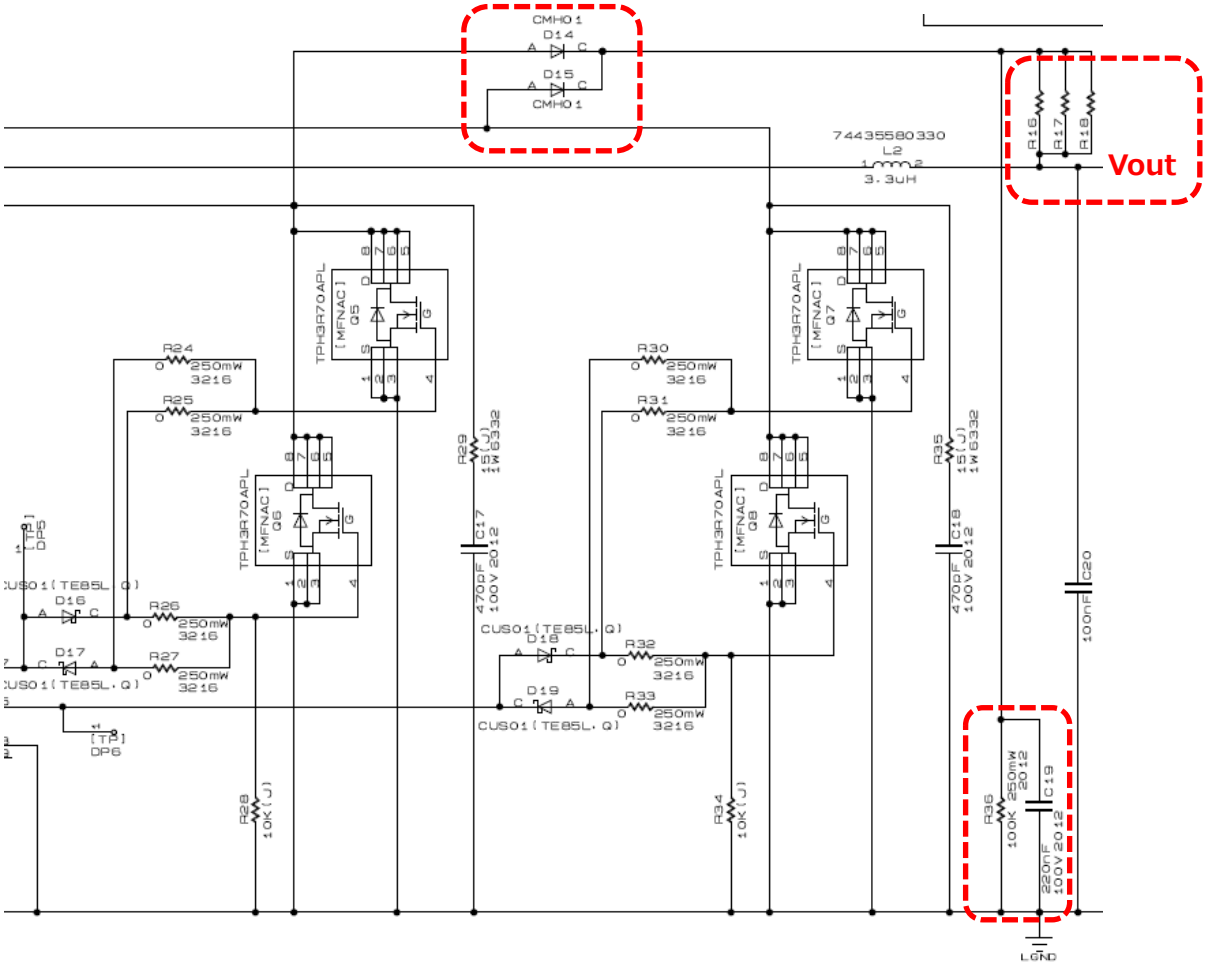

Figure 2.12 Regenerative circuit

D14, D15, R16, R17, R18, R36, and C19 constitute a regenerative circuit as shown in Figure 2.12. The surge voltage (V_{srg}) generated at Q5, Q6, Q7, and Q8 is absorbed by C19 and regenerates to the output via R16, R17, and R18. At this time, the power loss (P_{d_Rreg}) generated by R16, R17, and R18 is calculated by following equation:

$$P_{d\_Rreg} = \frac{(V_{srg} - V_{out})^2}{R16}$$

Suppose that V_{out} is 12.09V, the surge voltage is 60V, and R16, R17, and R18 are 6.8kΩ. Then, the power loss (P_{d_Rreg}) dissipated by R16, R17, and R18 is calculated to be 338mW per resistor. Adjust the values and ratings of each component according to the actual surge voltage.

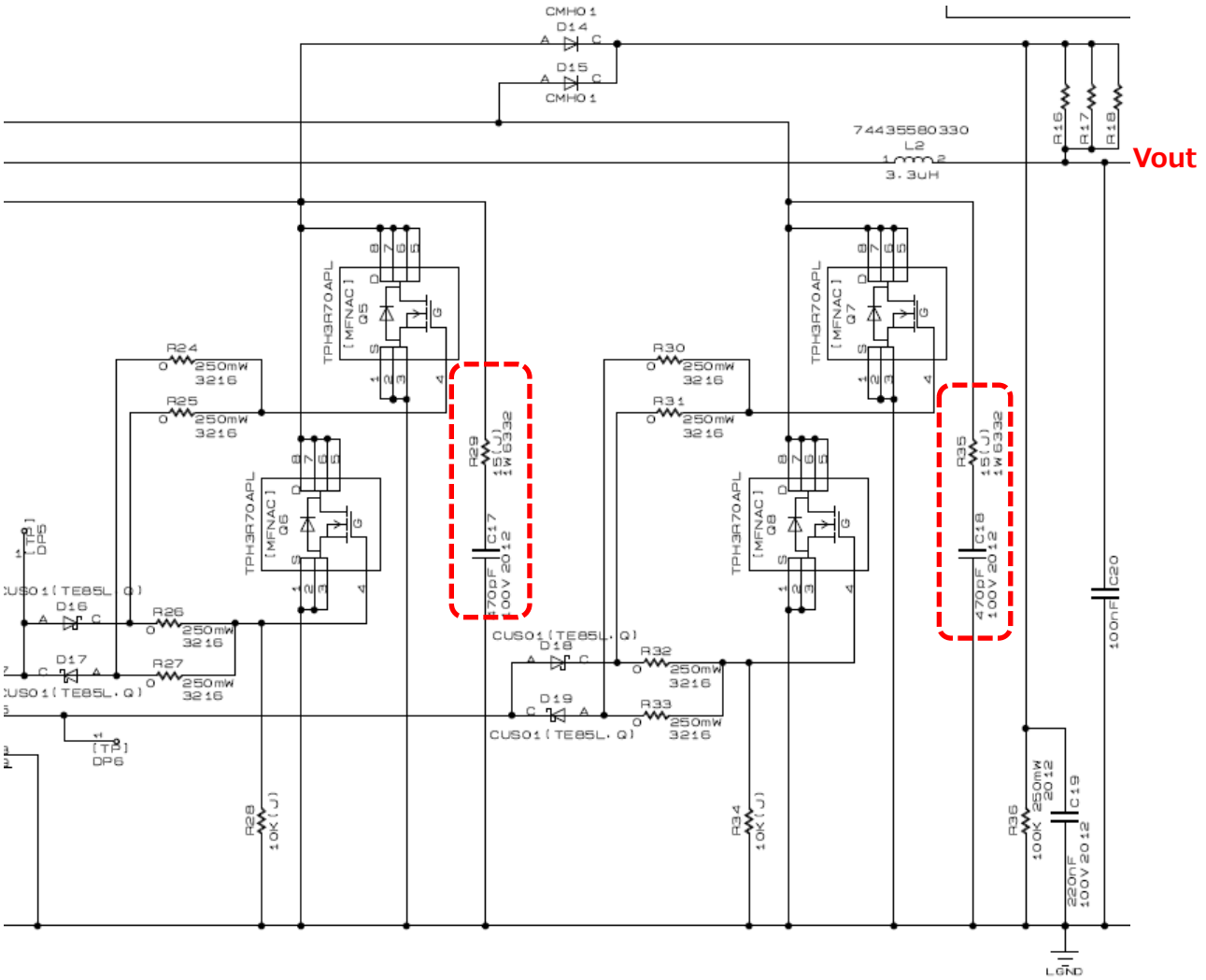

Figure 2.13 Snubber

R29-C17 and R35-C18 constitute RC snubber circuits as shown in Figure 2.13. These RC snubber circuits suppress the surge voltage (V_{srg}) generated at Q5, Q6, Q7, and Q8. At this time, the power loss dissipated by resistors R29 and R35 is calculated by following equation:

$$P_{d\_Rsnb} = C17 \times (V_{srg})^2 \times \left(\frac{f_{PWM}}{2}\right)$$

When the surge voltage (V_{srg}) is 60V and C17 and C18 are 470pF, the power loss dissipated by R29 and R35 (P_{d_Rsnb}) is calculated to be 313mW per resistor. Adjust the values and ratings of each component according to the actual surge voltage.

Output overvoltage detection circuit

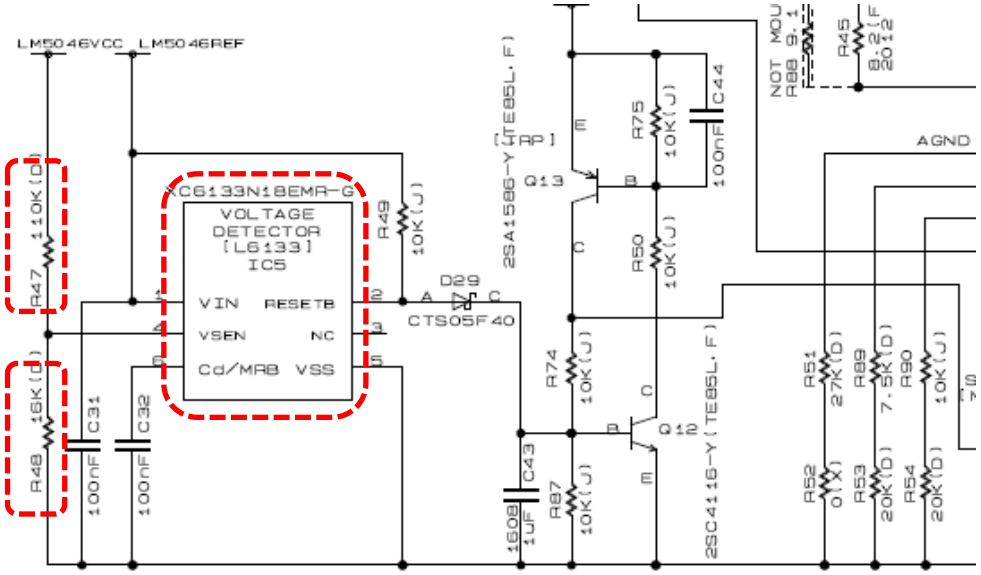

Figure 2.14 Output overvoltage detection circuit

The threshold for output overvoltage detection (V_{ovp}) is programmed with the detection voltage (V_{det}=1.8V) of the voltage detector (XC6133N18EMR-G) and external resistors (R47 and R48). The output voltage is monitored indirectly by the auxiliary supply voltage (V_{aux}). When V_{aux} reaches V_{ovp}, the voltage detector is activated and latches the SS pin of the PSFB PWM controller at a low level, then disable the switching operation. V_{ovp} is calculated by following equation:

$$V_{ovp} = \frac{(V_{det} + 90mV) \times (R47 + R48)}{R48}$$

As shown in Figure 2.14, this converter uses a 110kΩ resistor for R47 and a 16kΩ resistor for R48, setting V_{ovp} to 14.9V. Once this converter is shut down because of overvoltage detection, either of the following conditions must be fulfilled in order to return to the active mode.

1. Reset the Enable pin (i.e., open the Enable pin then reconnect it to GND)
2. Disable and re-enable the output of an external regulated DC power supply

If you need to monitor the output voltage directly, add an overvoltage detection circuit on the output side.

3. PCB design

This section describes considerations for the PCB design for the 300W isolated DC-DC converter.

3.1. PCB trace design

Creepage distance

Ensure appropriate spatial distance and creepage distances according to the safety standards specified in the required specification. Table 3.1 shows the creepage distances ensured in this converter. The required spatial and creepage distances vary depending on the operating environment, materials, material contamination levels, humidity, altitude (i.e., air pressure), and other factors.

Table 3.1 Minimum creepage distances (design values)

Line 1	Line 2	Creepage distance between Line 1 and Line 2
Input (photocoupler)	Output (photocoupler)	2.0mm
Input (transformer)	Output (transformer)	2.0mm

Current capacity

Each trace on PCB must be wide enough not to cause a temperature rise or IR drop when the maximum current flows through each trace.

3.2. PCB trace design for the PSFB circuit

This subsection describes the considerations for PCB design peripheral area of the PSFB circuit. Figure 3.1 shows the PSFB circuit (around the controller). Figure 3.4 and Figure 3.5 show the PCB traces that require special attention in the PSFB circuit. Refer to the datasheet of the PSFB PWM controller and the related documents for the guidelines on the layout of peripheral area of the controller.

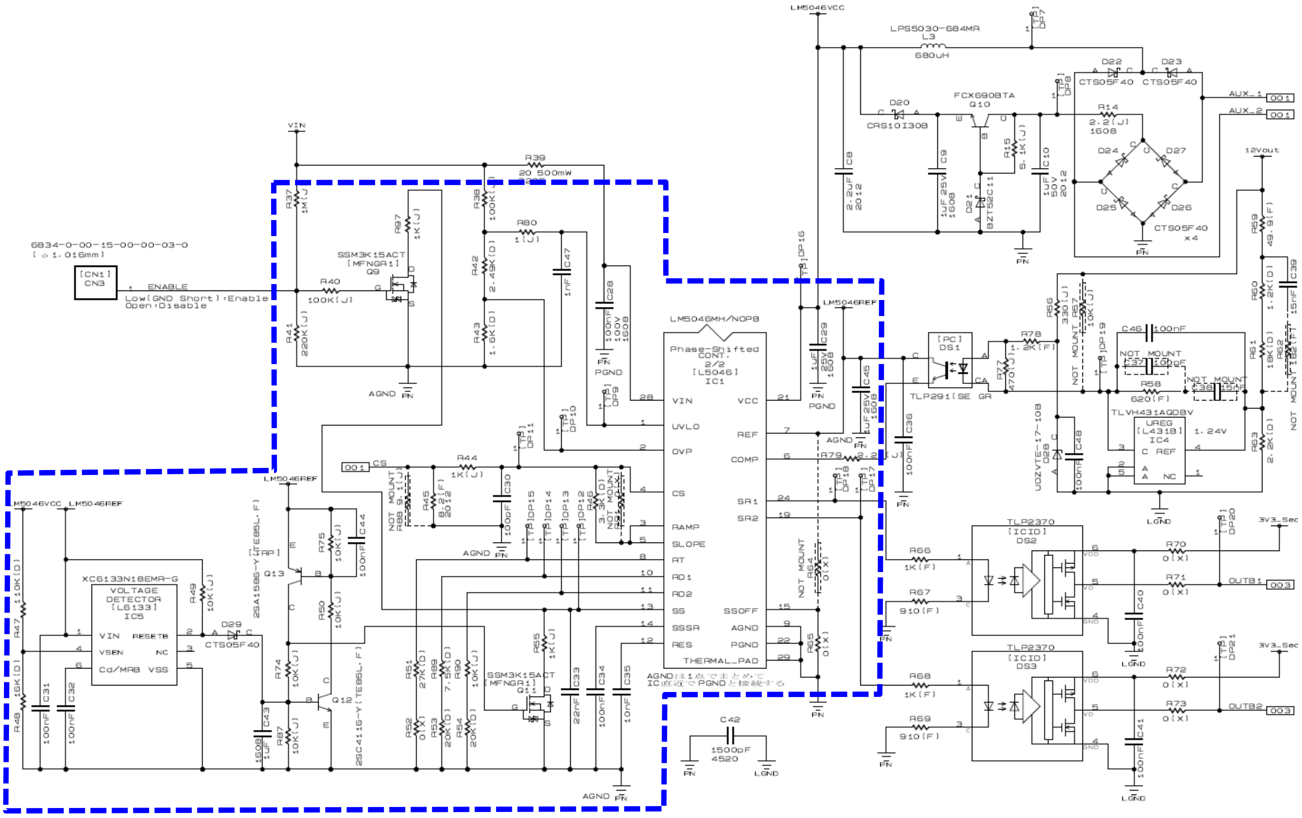

Figure 3.1 PSFB circuit (around the controller)

1. Place the PSFB PWM controller (IC1) away from the high-current switching circuit on the secondary side, the transformer, and the reactor.
2. Place the components surrounded by the blue dotted box in the vicinity of the PSFB PWM controller.
3. Connect the ground plane (PN in Figure 3.1) to the AGND pin of the PSFB controller through a path that does not have common impedance of a high current path..

Figure 3.2 shows the PCB top surface layout and Figure 3.3 shows the PCB bottom surface layout. Around the PSFB controller areas highlighted with dashed line boxes can be seen to suit the considerations above.

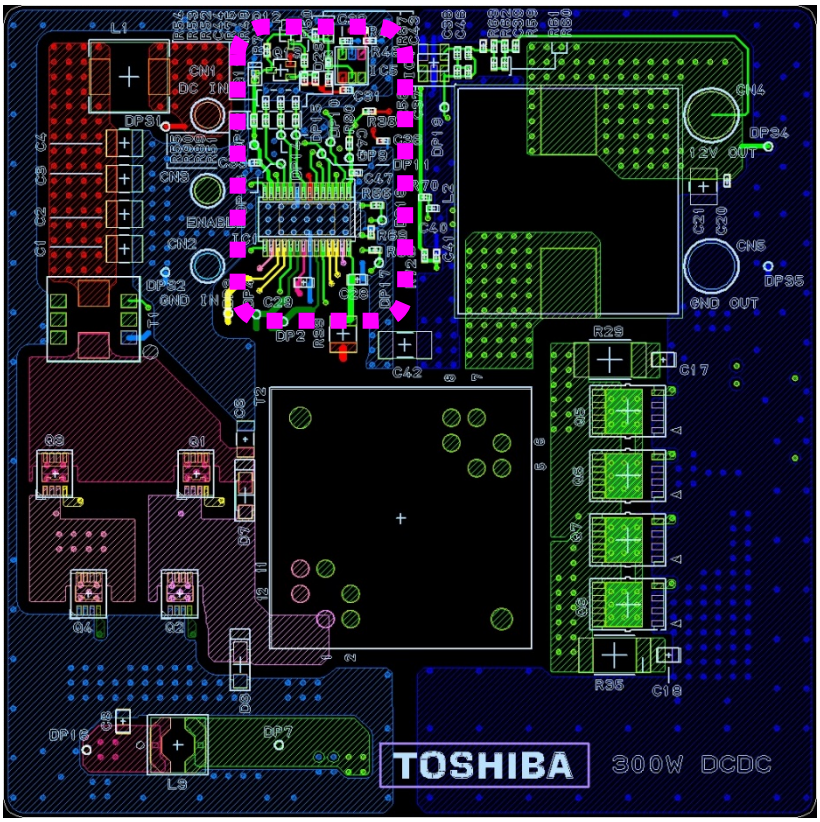

Figure 3.2 PCB top surface layout (around the controller)

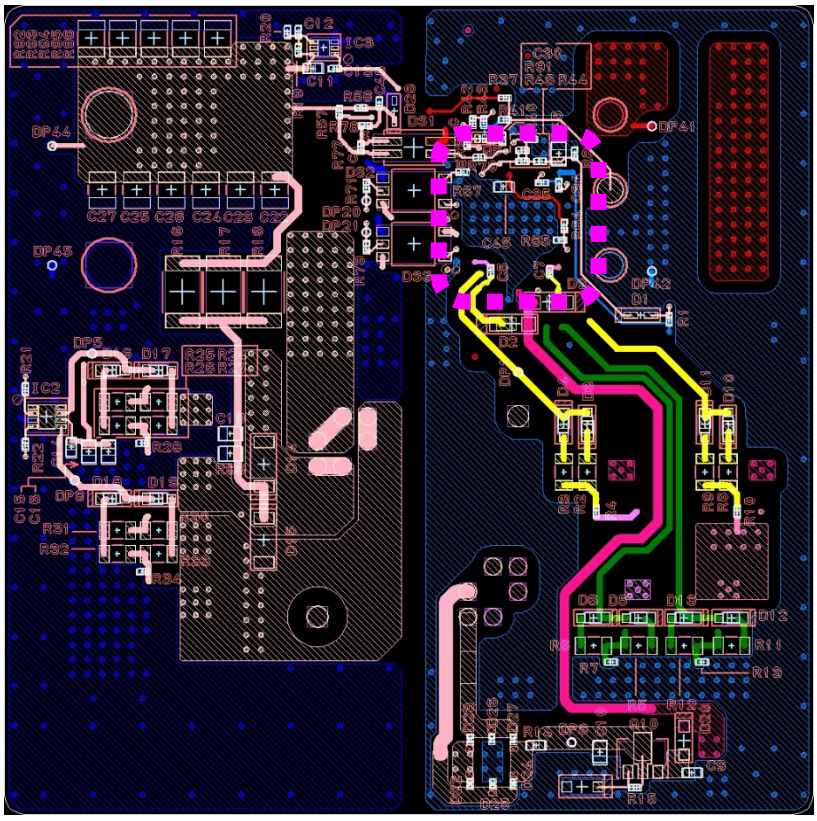

Figure 3.3 PCB bottom surface layout (around the controller)

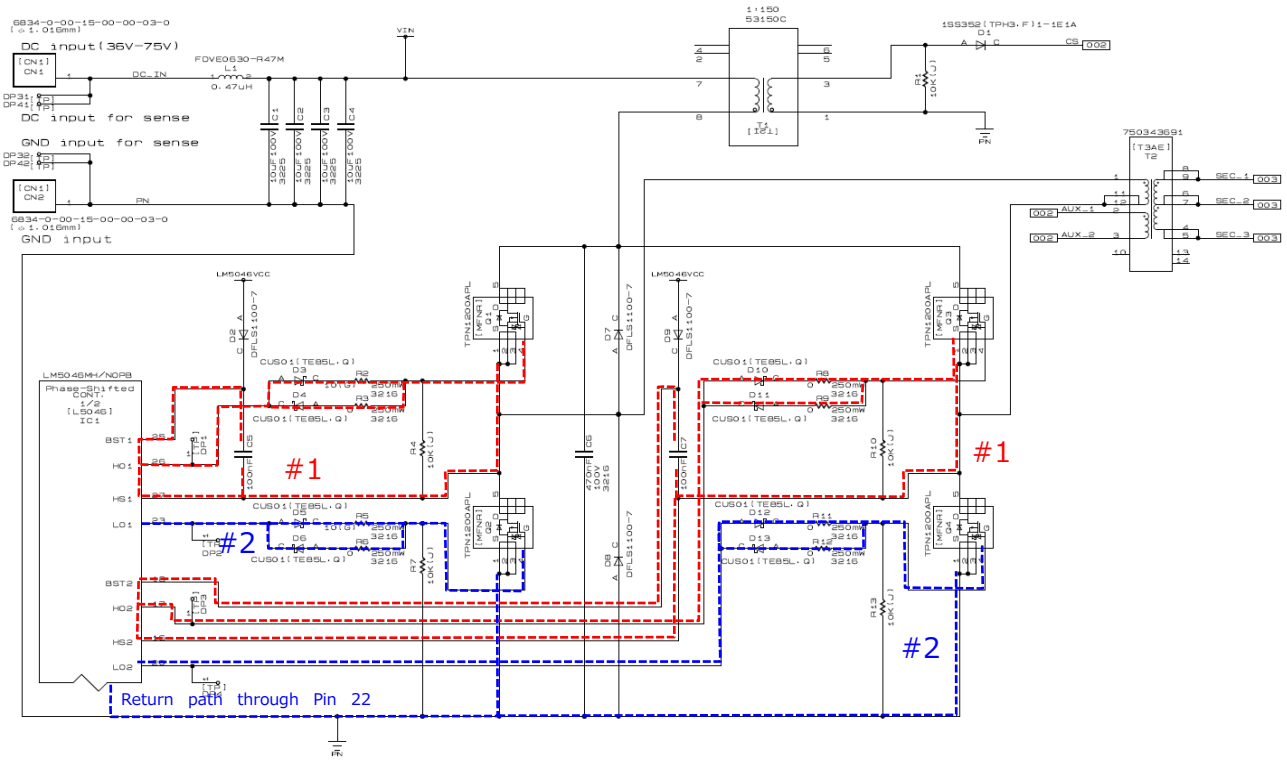

Figure 3.4 PCB traces of the PSFB circuit requiring special attention-1

1. Place components to minimize the area surroundding the switching nodes with considerable voltage changes (Line #1 and lines with a voltage fluctuation of the same potential as that of Line #1 in Figure 3.4).
2. Place Q1, Q2, Q3, and Q4 close to IC1 to minimize the lengths of the driver output lines (#1 and #2 in Figure 3.4) to ensure enough line widths and to be able to apply the maximum drive current.
3. Separate the return paths of the drive currents of Q1 and Q3 at positions close to their source pins.
4. Separte the return paths of the drive currents of Q2 and Q4 at portions close to the sourse pins of Q1 and Q3, when the return paths of the drive currents of Q2 and Q4 separates from the GND (PN) plane.
5. Kelvin connect the current-sensing line (CS) to the GND (PN) and the CS feedbacks to the PSFB PWM controller via the area with less currnet and/or voltage fluctuation.

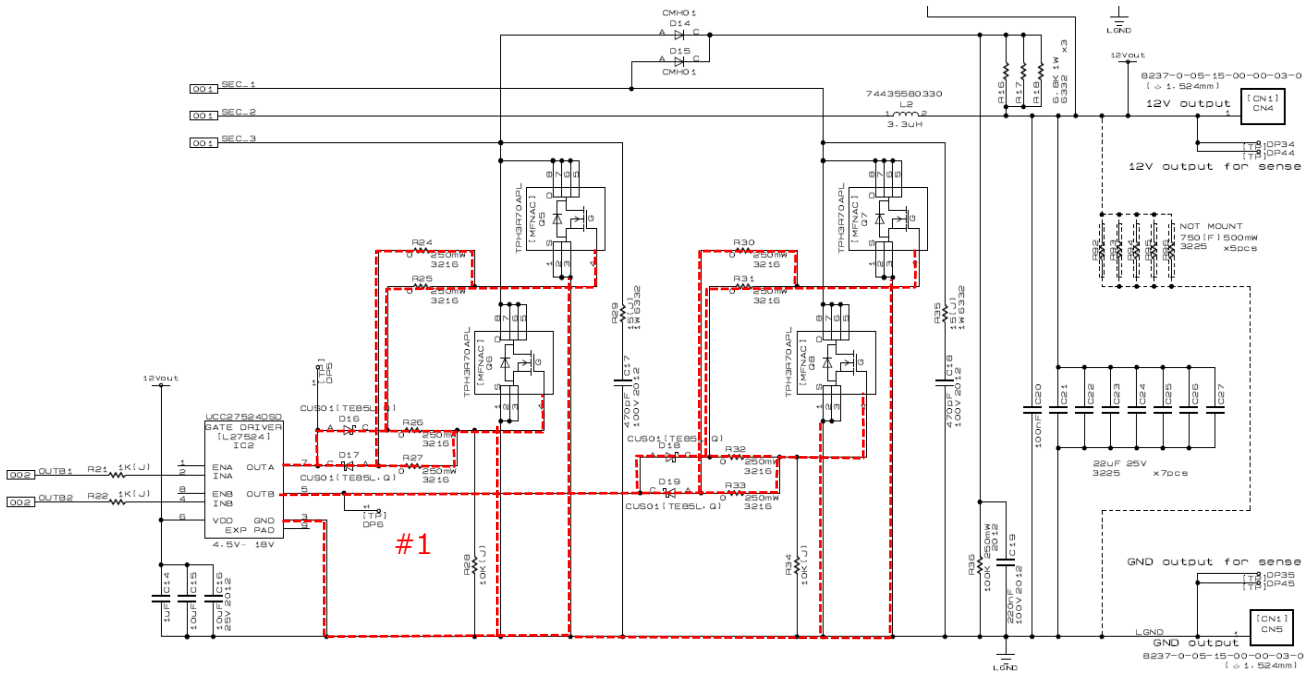

Figure 3.5 PCB traces of the PSFB circuit requiring special attention-2

1. Place Q5, Q6, Q7, and Q8 close to IC2 to minimize the length of the driver output line (#1 in Figure 3.5) to ensure enough line width and to be able to apply the maximum drive current.
2. When the GND (LGND) plane is not used as a return path of the drive current, separte the return path from a position close to the source pins of Q5-Q8.
3. Place the RC snubber C17-R29 close to the drain and the source pins of Q5 and Q6. Place the RC snubber C18-R35 close to the drain and source pins of Q7 and Q8.
4. Place D14, D15, C19, and R36 that constitute a regenerative circuit close to the drain and source pins of Q5, Q6, Q7, and Q8.
5. Place Q5, Q6, Q7, and Q8 close to T1 to minimize the loop of the transformer and the synchronous rectification MOSFETs.

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