1.6 kW T-Type 3-Level PFC Power Supply

Design Guide

RD172-DGUIDE-01

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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1. Introduction

This Design Guide (hereinafter referred to as "this Guide") describes how to design various circuits of 1.6 kW T-Type 3-Level PFC Power Supply (hereinafter referred to as "this power supply"). For detailed specifications, usage, and efficiency characteristic data of this reference, refer to the reference guide.

2. Circuit Specifications

The block diagram of this reference is shown in Fig. 2.1.

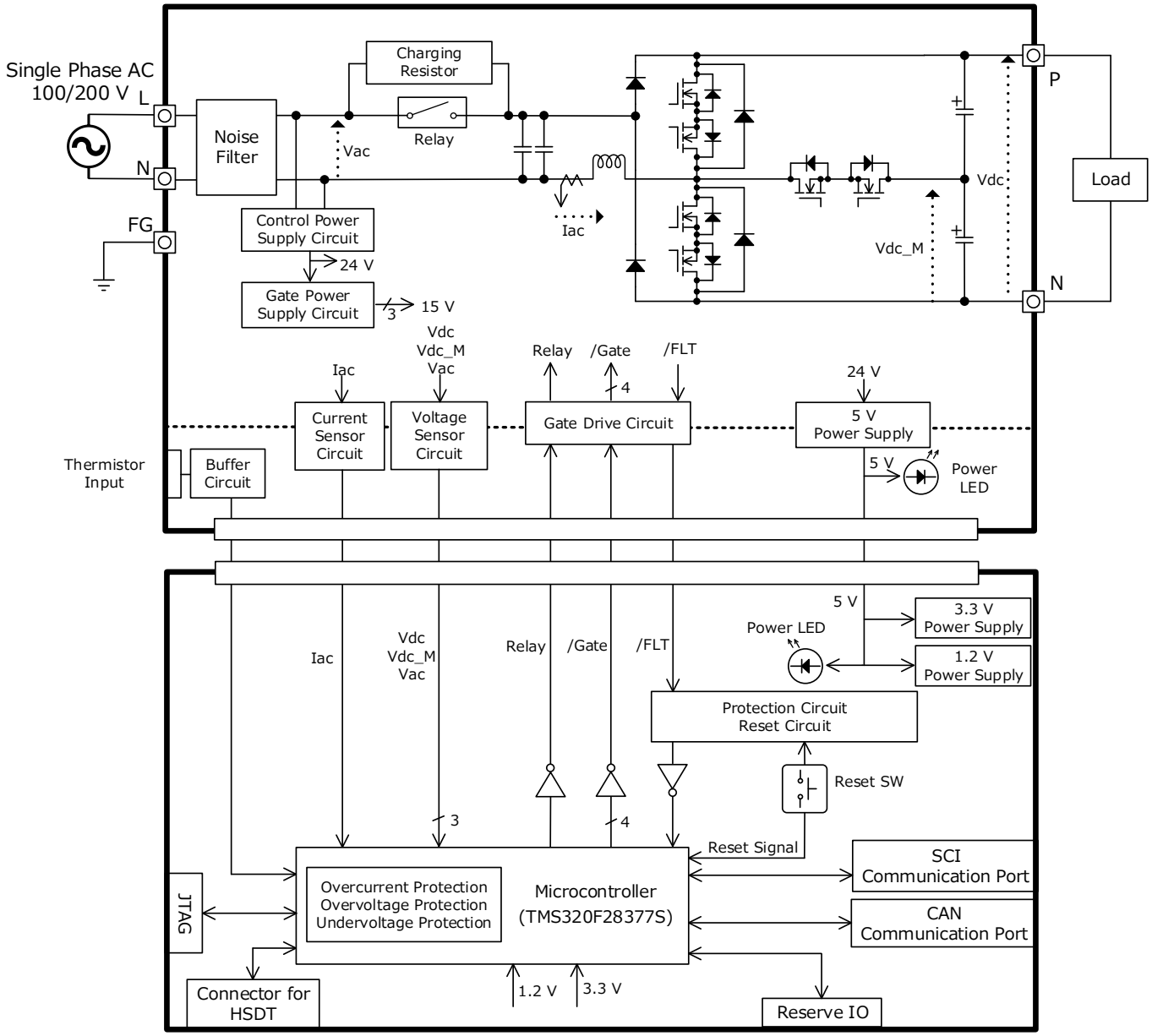


Fig. 2.1 Block Diagram

2.1. Electrical Specifications

The electrical specifications for this reference are shown in Table 2.1.

Table 2.1 Electrical Specifications

Item	Specification	Remark
AC Input Voltage Range	90 to 264 V	
AC Input Frequency Range	47 to 53 Hz, 57 to 63 Hz	Considering the fundamental frequency is 50 Hz / 60 Hz.
DC Output Rated Voltage	380 V	
Control Power Supply Voltage	DC 24 V	
Gate Voltage	DC 15 V	
DC Output Maximum Current	4.2 A	
Power Rating	1.6 kW @ AC 180 to 264 V 800 W @ AC 90 to 115 V	Between AC 115 V and 180 V with fixed DC output voltage of 380 V the outputs power changes according to the input AC voltage.
Switching Frequency	100 kHz	
Sensor Input	・AC input voltage ・AC input current ・DC output voltage ・DC midpoint voltage	The DC midpoint voltage is the voltage between two series capacitors and the DC output N terminal.

2.2. Devices Used

Fig. 2.2 shows the circuit of the power control part in this reference. Table 2.2 lists the devices used in this circuit. MOSFET Q4 disables the body diode operation of MOSFET Q3 and connects an external, high-performance diode for more efficient power supply. The same applies to MOSFET Q6 and MOSFET Q5. Table 2.2 lists the device characteristics selected this time.

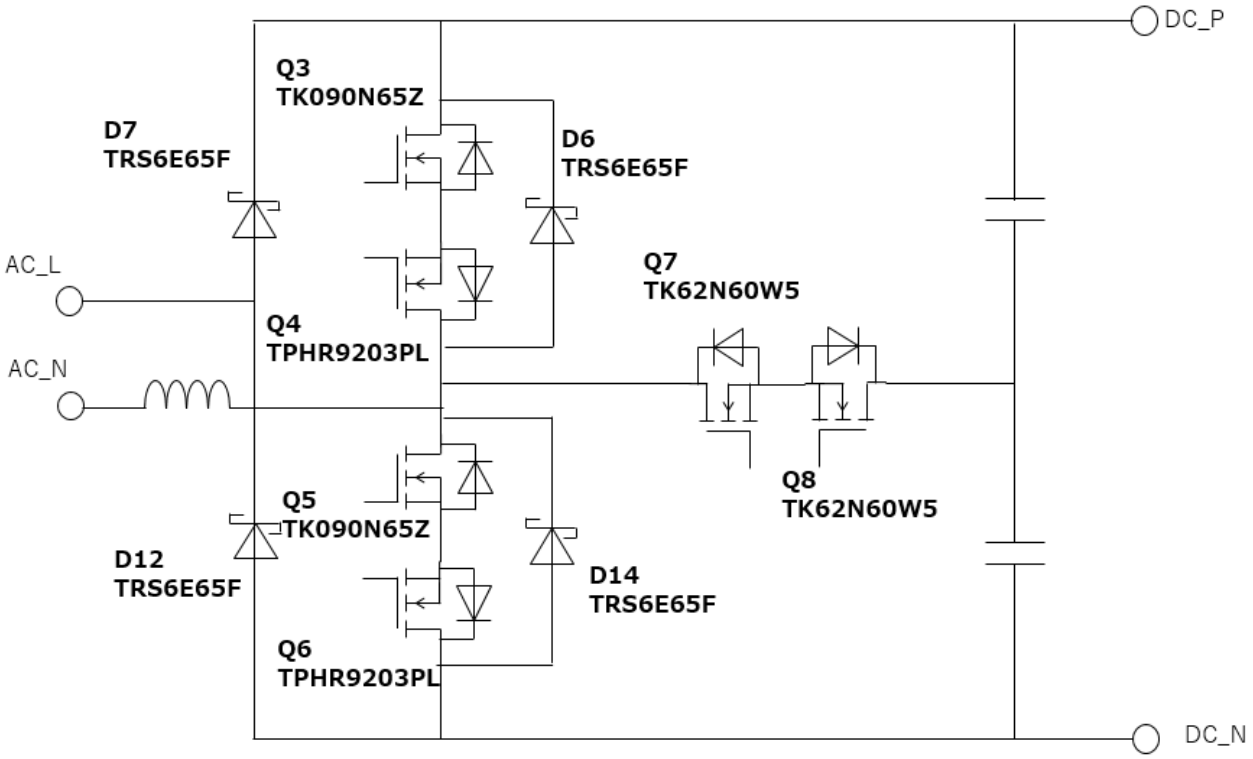


Fig. 2.2 Main Circuit Components

Table 2.2 Main Circuit Components

MOSFET	TK090N65Z	650 V
	TK62N60W5	600 V Integrated High Speed Diode
	TPHR9203PL	30 V
Diode	TRS6E65F	SiC Schottky Barrier Diode 650 V / 6 A

3. Operation of T-Type 3-Level PFC

The operation outline of the T-type 3-level PFC used in this reference is shown below.

3.1. Configuration of T-Type 3-Level PFC

Fig. 3.1 shows a basic circuit example of a T-type 3-level PFC. The AC input side of the T-type 3-level PFC circuit is the same circuit as the 2-level totem pole type PFC, which consists of an inductor L, Diode1, Diode2, MOSFET1, and MOSFET2, but a 3-level circuit is realized by connecting the two output capacitors in series and connecting their midpoint to the midpoint of MOSFET1 and MOSFET2 on the input side with a bidirectional element consisting of MOSFET3 and MOSFET4.

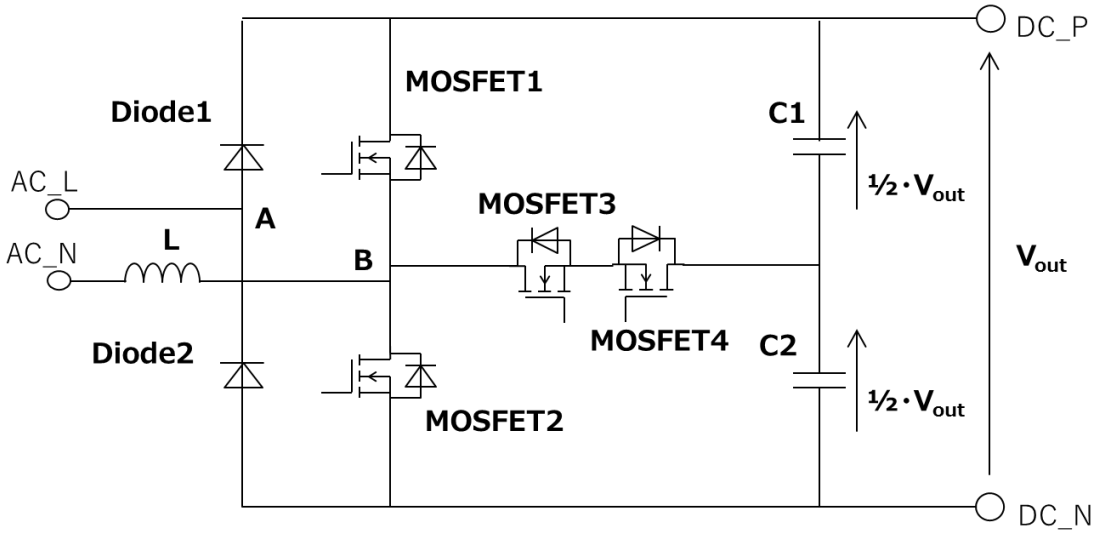


Fig. 3.1 Example of T-Type 3-Level PFC Basic Circuit

MOSFET used

MOSFET1, MOSFET2 shown in Fig. 3.1 must have withstand voltage that can handle the DC output voltage V_{out}. On the other hand, MOSFET3, MOSFET4 forming the bi-directional switch must have withstand voltage that can handle the voltage of C1 or C2, i.e. 1/2 x V_{out}.

Downsizing of Power Supply

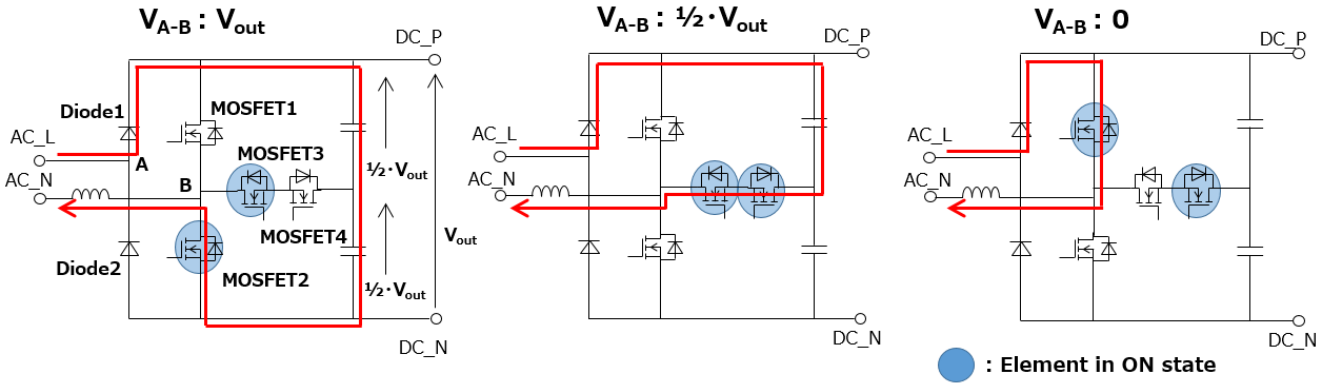
The voltage across the inductor of the T-type 3-level PFC circuit is less compared to a two-level totem-pole PFC. Assuming L as inductance, ΔI_L as inductor current ripple, V_L as voltage across the inductor, and Δt as voltage application time, the following relational expression is established.

$$\Delta I_L = V_L \times \Delta t / L$$

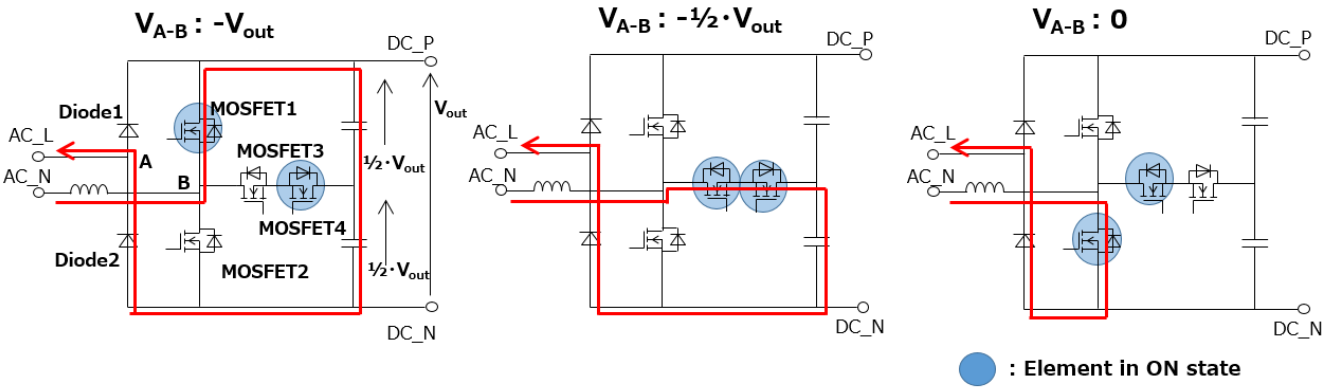
The three-level design can reduce the voltage V_L across the inductor, making it possible to reduce the inductor L while keeping the inductor ripple current ΔI_L constant. Reducing Δt, i.e. increasing the frequency, can also reduce the size of the inductor L. The miniaturization of inductors greatly contributes to the miniaturization of the power supply itself.

3.2. Voltage Control of T-Type 3-level PFC

The T-type 3-level PFC circuit (Fig. 3.1) improves the power factor. This is done by using the on/off states of each MOSFET to create 3 levels of voltage between A and B from input voltage, and then this voltage is controlled by using PWM to create a sinusoidal input current with no phase difference from the AC input voltage. Fig. 3.2 shows the MOSFET on/off states for each of the three levels of voltage during a positive half sine wave and a negative half sine wave.



(a) 3-level voltage during positive half sine wave input



(b) 3-level voltage during negative half sine wave input

Fig. 3.2 MOSFET On/Off Status for Each 3-Level Voltage

3.3. Circuit Operation of T-Type 3-Level PFC

Fig. 3.3 shows the operation image of the switching signals of the respective MOSFET of the T type 3-level PFC circuit (Fig. 3.1) and the periods a. to f. of the input voltage (between A and B). The operation during each period is described below.

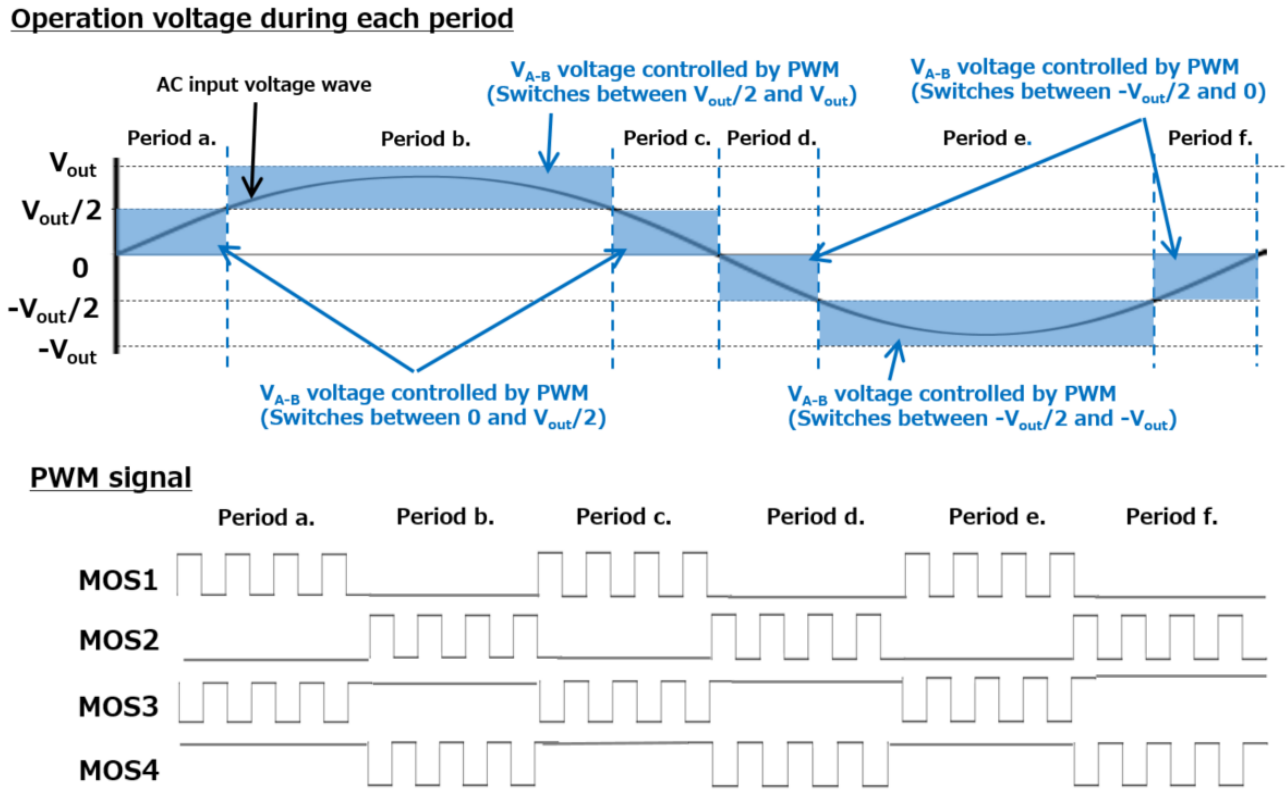


Fig. 3.3 MOSFET Switching Signals and Circuit Voltage Operation Waveform of T-Type 3-Level PFC

Fig. 3.4 shows the operation during the positive half sine wave input period. PWM control is performed so that when the AC input voltage is between 0 and 1/2 V_{out}, the voltage V_{A-B} between A and B is 0 or 1/2 V_{out}, and when the AC input voltage is more than 1/2 V_{out}, V_{A-B} is 1/2 V_{out} or V_{out}.

Period a.

In Fig. 3.3, the AC input voltage is between 0 and 1/2 V_{out}. Voltage V_{A-B} of 0 and 1/2 V_{out} are alternately generated by PWM signal to create an input sine wave current whose phase is matched to the input voltage. (Fig. 3.4 Period a. Operation)

Period b.

In Fig. 3.3, the AC input voltage is more than 1/2 V_{out}. Voltage V_{A-B} of 1/2 V_{out} and V_{out} are alternately generated by PWM signal to create an input sine wave current whose phase is matched to the input voltage. (Fig. 3.4 Period b. Operation)

Period c.

In Fig. 3.3, the AC input voltage is between 0 and 1/2 V_{out}. Voltage V_{A-B} of 0 and 1/2 V_{out} are alternately generated by PWM signals to create an input sine wave current whose phase is matched to the input voltage. (Fig. 3.4 Period c. Operation)

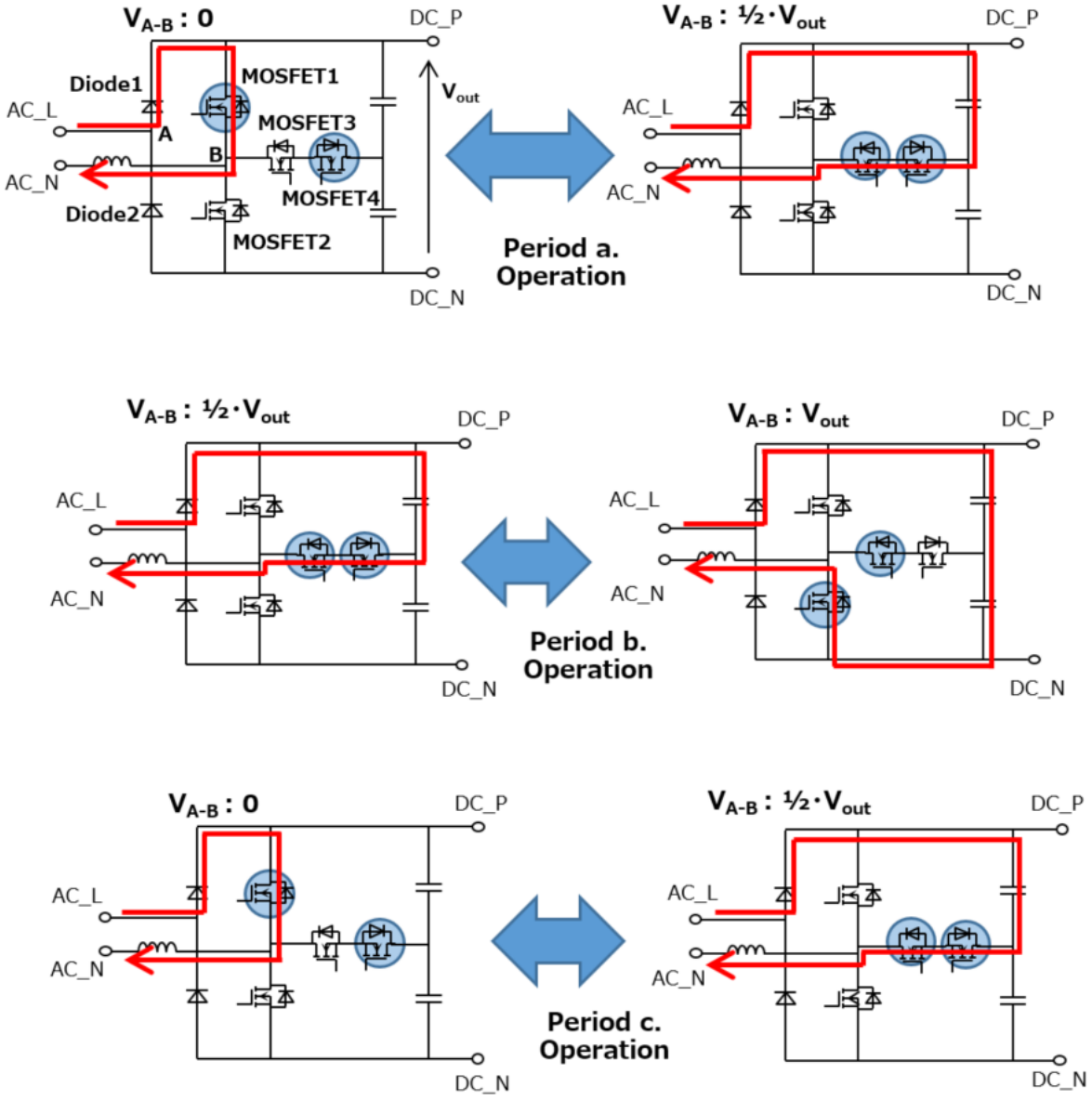


Fig. 3.4 Operation during Positive Sine Half Wave Input Period

Fig. 3.5 shows the operation during the negative half sine wave input period. PWM control is performed so that when the AC input voltage is between 0 and -1/2 V_{out}, the voltage V_{A-B} between A and B is 0 or -1/2 V_{out}, and when the AC input voltage is between -1/2 V_{out} and -V_{out}, V_{A-B} is -1/2 V_{out} or -V_{out}.

Period d.

In Fig. 3.3, the AC input voltage is between 0 and -1/2 V_{out}. Voltage V_{AB} of 0 and -1/2 V_{out} are alternately generated by PWM signal to create an input sine wave current whose phase is matched to the input voltage. (Fig. 3.5 Period d. Operation)

Period e.

In Fig. 3.3, the AC input voltage is less than -1/2 V_{out}. Voltage V_{AB} of -1/2 V_{out} and -V_{out} are alternately generated by PWM signal to create an input sine wave current whose phase is matched to the input voltage. (Fig. 3.5 Period e. Operation)

Period f.

In Fig. 3.3, the AC input voltage is between 0 and -1/2 V_{out}. Voltage V_{AB} is 0 and -1/2 V_{out} are alternately generated by PWM signal to create an input sine wave current whose phase is matched to the input voltage. (Fig. 3.5 Period f. Operation)

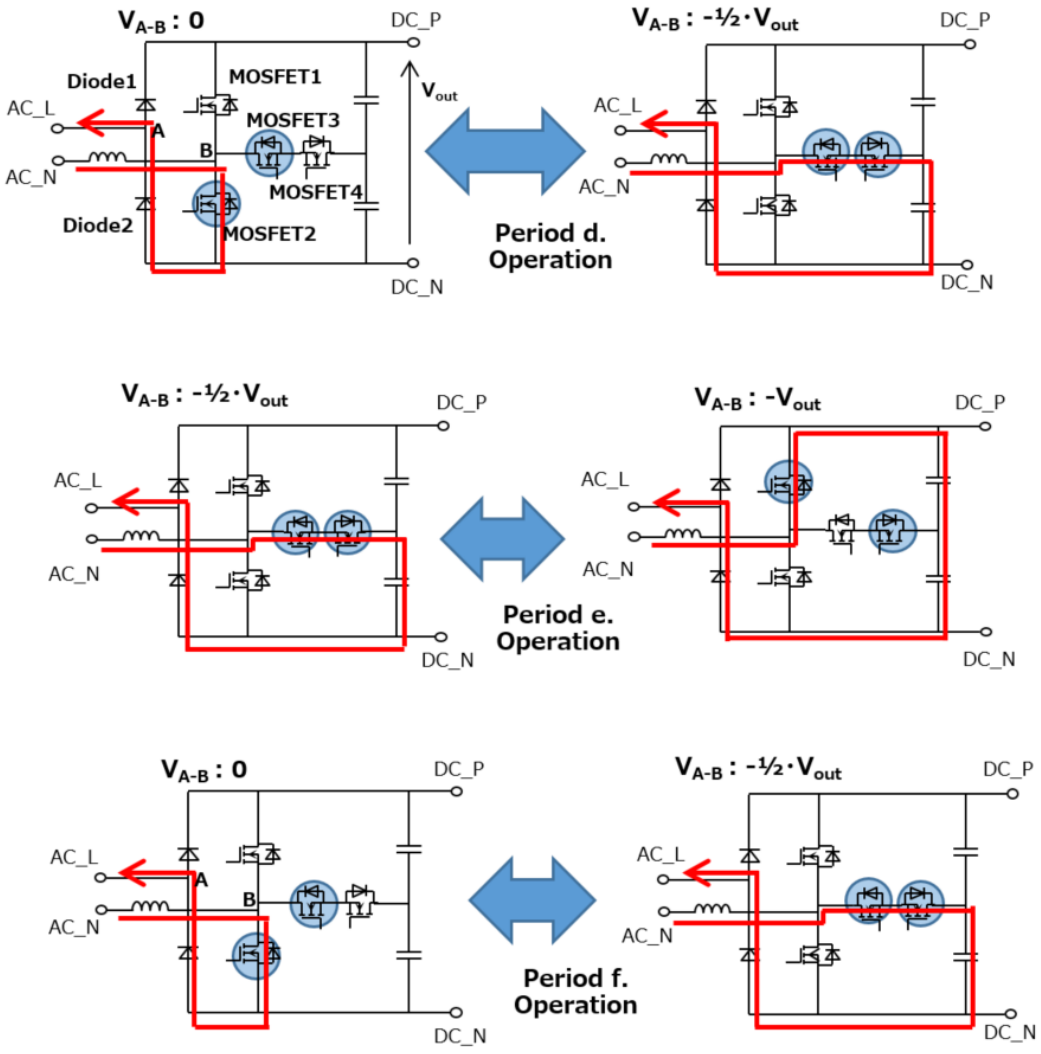
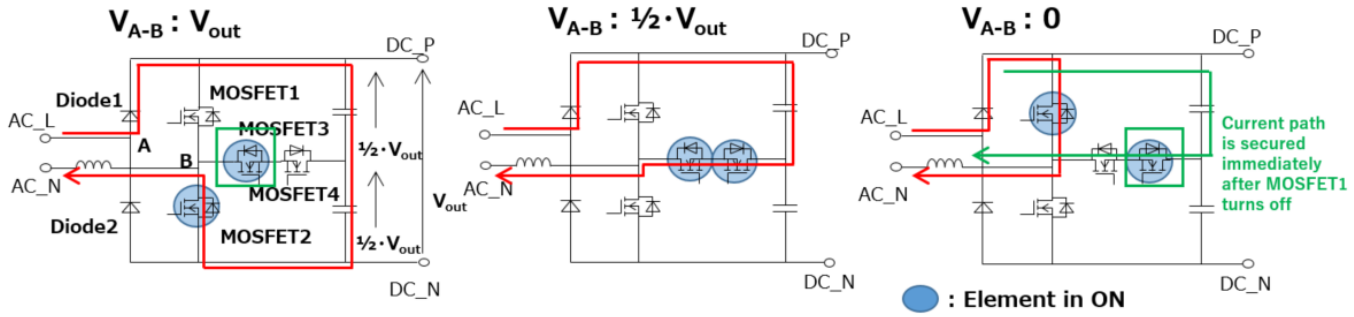


Fig. 3.5 Operation during Negative Half Sine Wave Input Period Supplement (MOSFET3, MOSFET4 Operation)

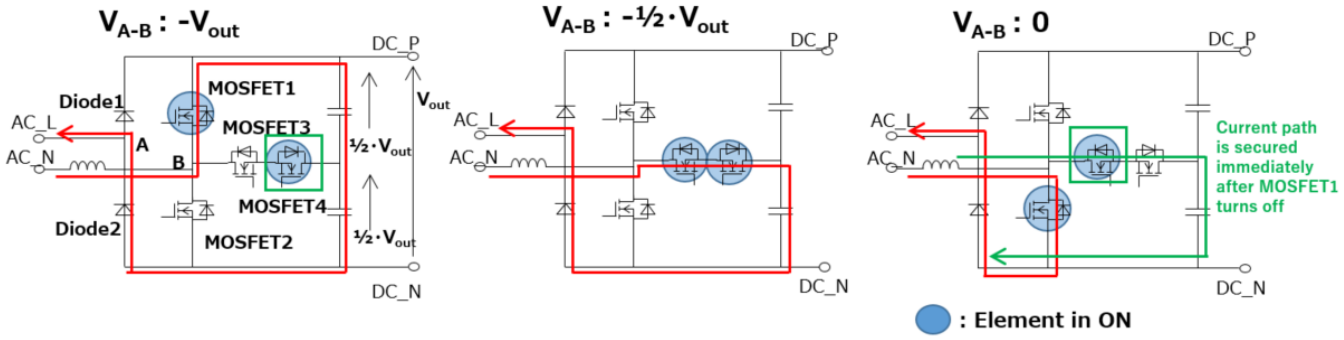
Fig. 3.6 (a) shows that during the positive half sine wave input, when the 3-level voltage (V_{A-B} voltage between A and B) is 0, MOSFET4 is turned on even though no current flows. This is to secure the current path from when MOSFET1 is turned off until MOSFET3 is turned on.

In addition, when the A-B voltage V_{A-B} is V_{out}, MOSFET3 is turned on even though no current flows, therefore MOSFET3 is always turned on in the period b. of Fig. 3.4, during which V_{A-B} alternately changes between 1/2 V_{out} and V_{out}, thus reducing the drive loss of MOSFET3.

Fig. 3.6 (b) Operation of MOSFET3, MOSFET4 for 3-level voltages during a negative half sine wave input is also similar.



(a) 3-Level Voltages during Positive Half Sine Wave Input



(b) 3-Level Voltages during Negative Half Sine Wave Input

Fig. 3.6 MOSFET Energization at Every Voltage Level

4. Circuit Design

4.1. AC Line Section

This section describes the AC line design of this reference. The AC line circuit is shown in Fig. 4.1.

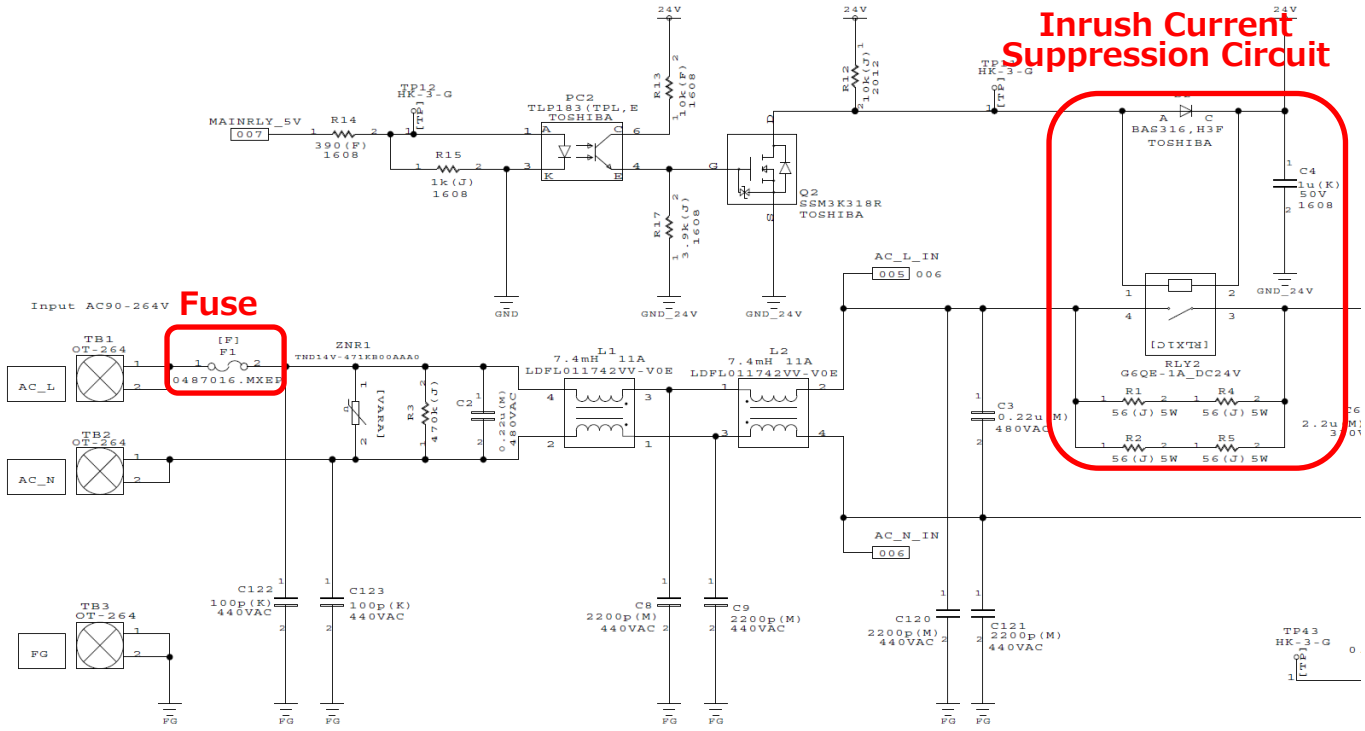


Fig. 4.1 AC Line Circuit

Fuse

A fuse (F1) is installed to cut off the AC line when abnormal current flows through the AC line. For the fuse, select the fuse according to the maximum current value of the AC line. The effective value of the maximum value of AC current is calculated using the following formula.

AC current maximum value = maximum power/power supply efficiency/input voltage effective value (min)

Table 4.1 AC Current Values

	AC 100 V System			AC 200 System			
Input Voltage	90	100	115	180	200	240	V
Output Power	800			1600			W
Efficiency	95						%
AC Current Value	9.36	8.42	7.32	9.36	8.42	7.01	A

The maximum AC current is 9.36 A when the efficiency is 95%. A fuse rated 16 A is selected for this reference, considering a margin of about 2 times.

Inrush Current Suppressing Components

A resistor configuration ((R1+R4) // (R2+R5)) is implemented to suppress inrush current when the AC power is turned on. The resistance value should be set according to the maximum input voltage and maximum input current of the AC line. The resistance value is calculated using the following equation.

Resistance > Maximum Input Voltage / Maximum Input Current

From the above equation, the largest resistor is required when using 1.6 kW power rating of this reference and AC 264 V input. The maximum input current at the maximum input voltage AC 264 V (peak voltage is 373 V) is 6.06 Arms (peak current 8.57 A), and thus the resistance value is approximately 43.6 Ω or more from the above equation. This reference uses a 56 Ω resistor with margin considerations. The resistance peak current under this condition is 6.66 A.

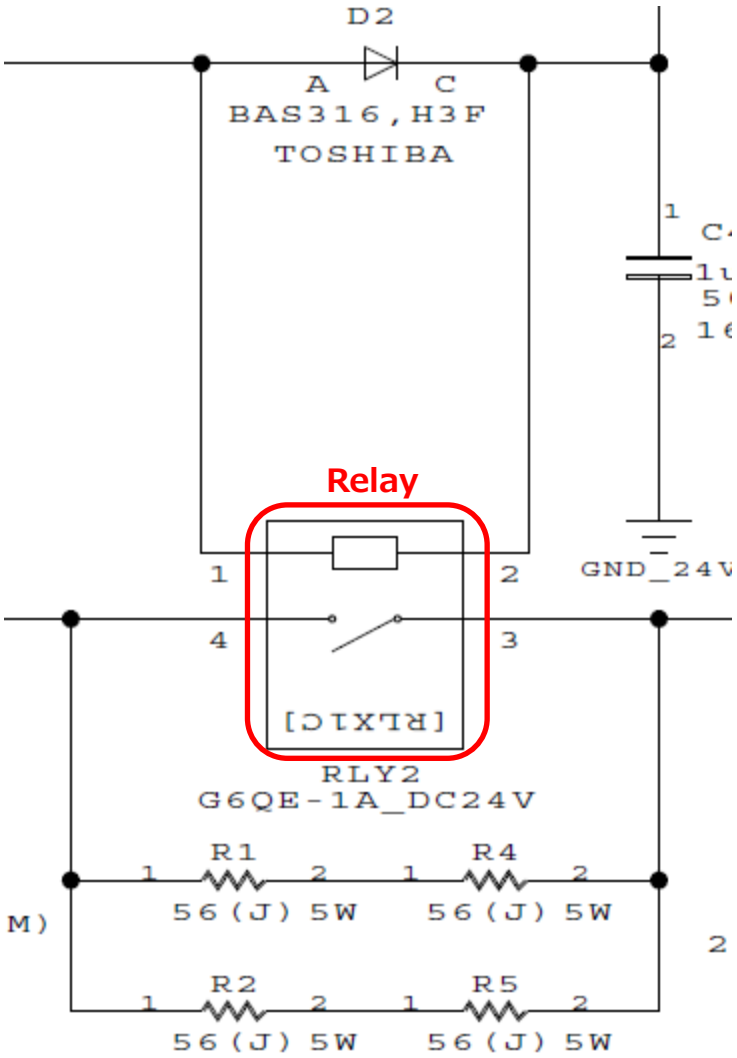


Fig. 4.2 Inrush Current Suppression Circuit

4.2. PFC Section

Gate Drive Circuit

For reference the gate drive circuit of MOSFET Q3 on the upper arm section in Fig. 2.2 is shown in Fig. 4.3. The design of the gate drive circuit affects power supply efficiency and EMI noise. Generally, power supply efficiency and EMI noise have a trade-off relationship, so it is necessary to design both in a balanced manner.

The gate drive circuit of this reference has a circuit configuration which can be used to adjust the switching speed of MOSFET. If the noise at turn-on of MOSFET needs to be reduced, changing the gated series resistor (R21) to a large value may reduce EMI noise. However, note that the gate resistance during turn-off is a parallel equivalent resistance of R21 and R23, so changing R21 not only changes the turn-on speed but also the turn-off speed.

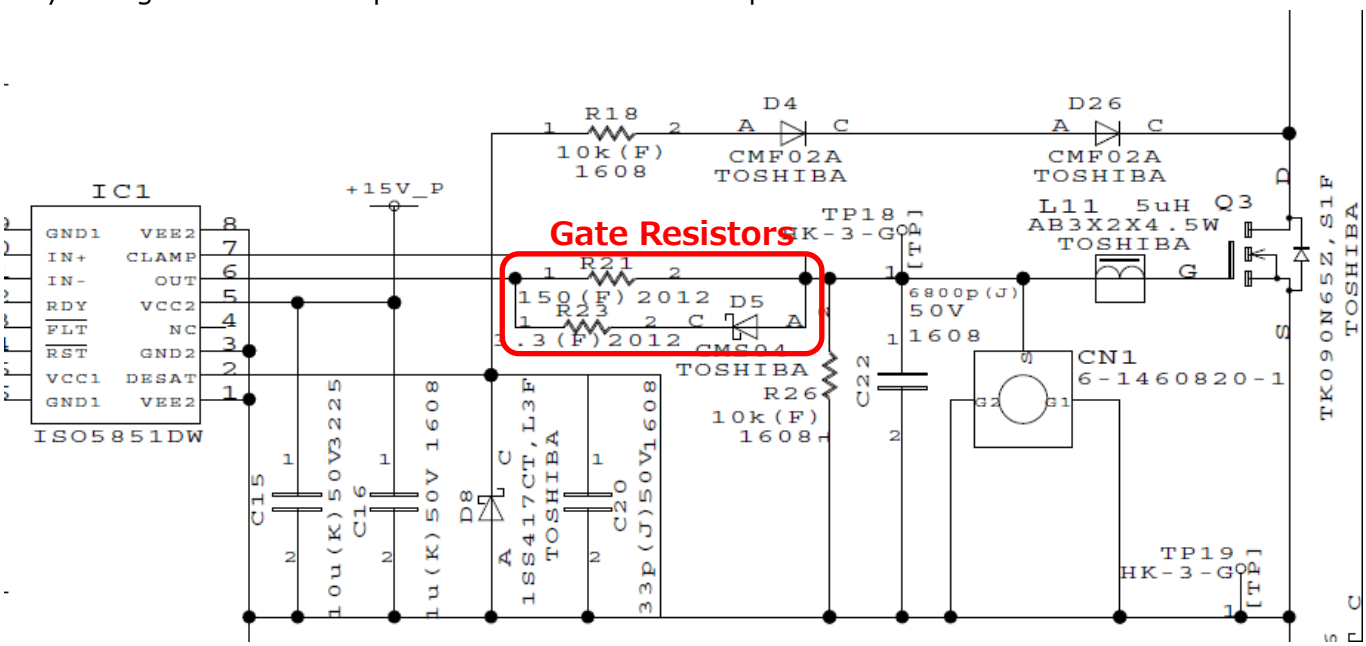


Fig. 4.3 Gate Drive Circuit

Current Detector

The maximum input current is 8.89 Arms (voltage AC 180 V at rated 1.6 kW and current at voltage AC 90 V at 800 W) with a peak value of 12.57 A, thus after taking margin the measurement range is set to be ±20 A. Fig. 3.4 shows the circuit. The critical properties of the current sensors (F02P015S05L) used are:

Reference Voltage (output) (at IP=0): 2.5 V

(Reference voltage: Typical value of the sensor-output (V_{out} terminal) voltage when the current under test is 0 A)

Theoretical sensitivity: 41.67 mV/A

For ±20 A detection, the output voltage of the current sensor is reference voltage 2.5 V ± (41.47 mV/A×20 A), which is 2.5 V±0.8334 V (-20 to 20 A). The current sensor voltage is amplified three times by the differential amplifier circuit (multiplying ±0.8334 V by three) so that the detection voltage is in the range of 0 to 5 V, and thus the output becomes 2.5 V±2.5002 V (-20 to 20 A).

The resolution is the following when using a 12-bit converter (4096 levels).

(5 V/4096) × (20 A/2.5002 V) = 9.765 mA

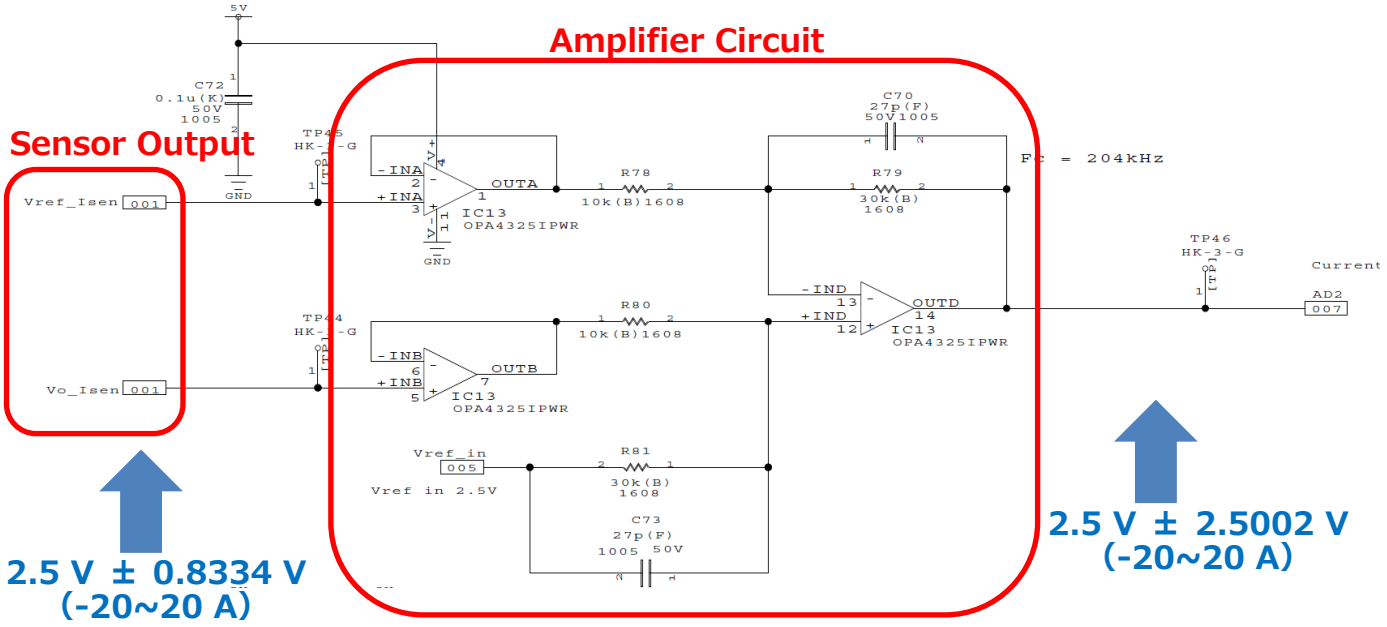


Fig. 4.4 Current Detection Circuit

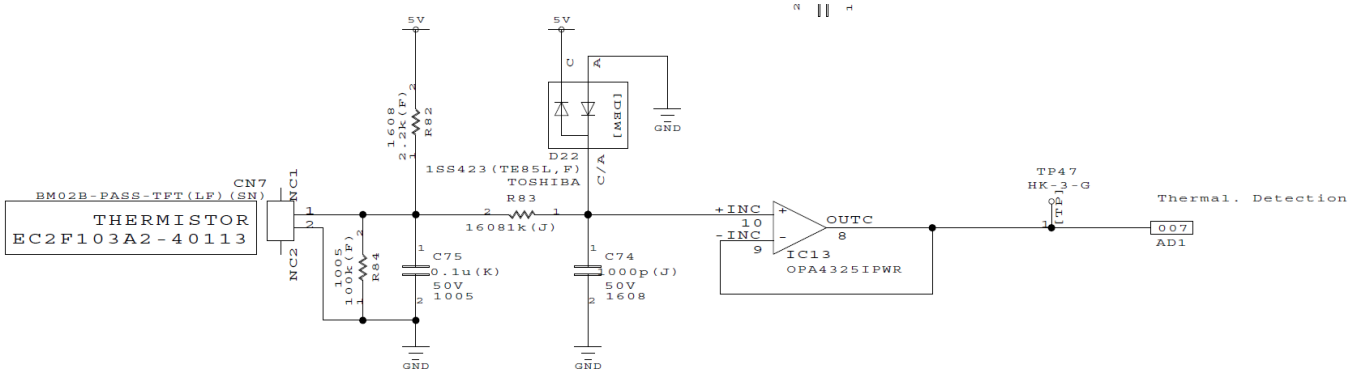


Fig. 4.5 Temperature Detection Circuit

Temperature Detection Circuit

The temperature detection circuit is shown in Fig. 4.5 and Fig. 4.6. The characteristics of the thermistor used this time are as follows.

Resistance value (25 ℃): 10 (kΩ) ±1 %

B constant: 3435 (K) ±1 %

It is a physical property value representing the sensitivity of the thermistor to temperature change (ratio of change in resistance value). Indicates that the logarithm of the resistance value is linearly related to the reciprocal of the absolute temperature.

$$B = \frac{log_e R - log_e R_0}{\frac{1}{T} - \frac{1}{T_0}}$$

R: Resistance at absolute temperature T (K) (Ω)

R_0: Resistance at absolute temperature T_0 (K) (Ω)

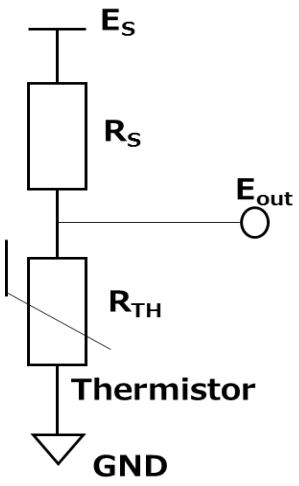


Fig. 4.6 Temperature Detection Circuit (Thermistor portion)

The circuit shown in Fig. 4.6 uses a thermistor to convert temperature changes to voltage changes.

Consider three points (T_1, T_2, T_3) with equal temperature intervals. Let the detected voltage E_{out} at these points be (E_1, E_2, E_3). R_S is set so that the temperature and E_{out} are linearly aligned (E_{out} is proportional to the temperature). Thus, the relation between E_{out} and temperature is expressed by a straight line approximation and the temperature can be determined by detecting E_{out}.

[R_S Settings]

As $T_1<T_2<T_3$

Obtain R_S for which $(E_2-E_1) = (E_3-E_2)$ when $\Delta T_{32} = (T_3-T_2) = \Delta T_{21} = (T_2-T_1)$.

If R_{TH} (thermistor resistance) is R_1, R_2, R_3 for T_1, T_2, T_3, then E_{out} (E_1, E_2, E_3) shown in Fig. 4.6 has the following relation.

$$E_1 = \frac{E_S \times R_1}{(R_1 + R_S)}$$

$$E_2 = \frac{E_S \times R_2}{(R_2 + R_S)}$$

$$E_3 = \frac{E_S \times R_3}{(R_3 + R_S)}$$

When three equally spaced points are linearly arranged, the difference between the detected voltage E_{out} (E_1, E_2, E_3) is also equal, so the following equation holds.

$$\frac{E_S \times R_1}{(R_1 + R_S)} - \frac{E_S \times R_2}{(R_2 + R_S)} = \frac{E_S \times R_2}{(R_2 + R_S)} - \frac{E_S \times R_3}{(R_3 + R_S)}$$

Solving the above for R_S yields the following equation:

$$R_S = \frac{R_2(R_1 + R_3) - 2R_1R_3}{R_1 + R_3 - 2R_2}$$

Next, thermistor resistance R_{30}, R_{60}, R_{90} is calculate when T is 30 °C, 60 °C, 90 °C (303 K, 333 K, 363 K).

When T is 30 °C, 60 °C or 90 °C, the thermistor resistance R_{30}, R_{60}, R_{90} is obtained by substituting the thermistor resistance of T_0 (298 K, 25 °C) with 10 kΩ and the thermistor B-constant of 3435 (K).

$$R_{TH} = R_0 \times e^{\left(B\left(\frac{1}{T}-\frac{1}{T_0}\right)\right)}$$

T, and T_0 are in Kelvin (K).

$R_1=R_{30}$ = 8.27 kΩ (R_{TH} at 30 °C), $R_2=R_{60}$ = 2.98 kΩ (R_{TH} at 60 °C), $R_3=R_{90}$ = 1.27 kΩ (R_{TH} at 90 °C)

By using these in the R_S expression

R_S = 2.1 kΩ is obtained.

E_{out} is expressed by the following equation.

$$E_{out} = E_s \times \frac{R_{TH}}{R_s + R_{TH}}$$

Thermistor resistance R_{TH} at each temperature can be substituted into the above equation to derive the relation between temperature and E_{out}.

Voltage Detection Circuit

The circuit shown in Fig. 4.7 detects AC voltage, DC midpoint voltage, and DC voltage. Each voltage divided by a resistor voltage divider circuit and is amplified by an amplifier circuit after passing through an isolation amplifier. The overall amplification factor is set so that each voltage falls within the detection circuit output voltage range of 0 to 5 V. By dividing the detection circuit output voltage 0 to 5 V by the overall amplification factor, it is possible to know the input voltage corresponding to the detection circuit output voltage 0 to 5 V. Table 3.2 shows the amplification factor, measurement range, and resolution of the circuit.

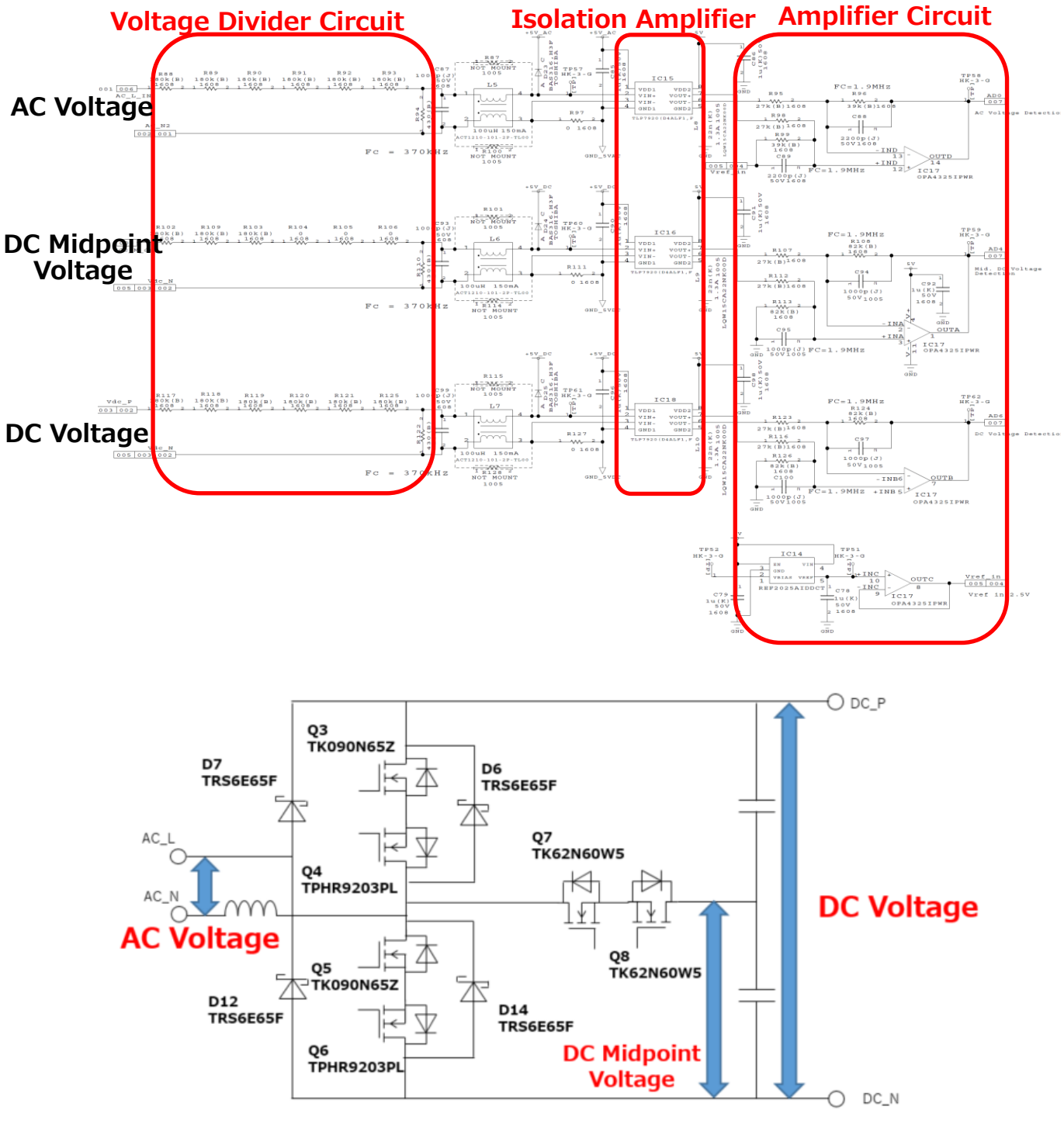


Fig. 4.7 Voltage Detection Circuit

Table 4.2 Voltage Detection Numeric Values

	A: Division Ratio	B: Isolation Amp. Gain	C: Amplifier Circuit Gain	D: Total Gain (AxBxC)	E: Measurement Range (5 V/D)NOTE1	Resolution V/bit (E/4096)NOTE2
AC voltage	3.98E-04	8.2	1.44	4.72E-03	±530	0.26
DC midpoint voltage	7.96E-04	8.2	3.04	1.98E-02	252	0.06
DC voltage	3.98E-04	8.2	3.04	9.92E-03	504	0.12

NOTE1: Input voltage range for which detection circuit output voltage is within 0 to 5 V range
NOTE2: 12 bit converter is used (12 bit means 4096 levels)

Output Capacitor

The capacitance values for the output capacitors (C110 to C115, C48, C49, C54, and C55) are calculated based on the holdup time (T_{hold}) NOTE1 requirements. The holdup time T_{hold} is expressed by the following equation, where C_{out} is the capacitance of the output capacitors, V_{out} is the output voltage, V_{out_min} is the output lower limit voltage, and P_{out} is the maximum output power. The energy output when the capacitor voltage changes from V_{out} to lower limit voltage V_{out_min}, is equal to the energy of output power P_{out} during the holdup time (T_{hold}), and is described by the following equation.

$$\frac{1}{2}C_{out}{V_{out}}^2 - \frac{1}{2}C_{out}{V_{out-min}}^2 = P_{out} \times T_{hold}$$

$$T_{hold} = C_{out} \times \frac{({V_{out}}^2 - {V_{out\_min}}^2)}{2 \times P_{out}}$$

With V_{out} = 380 V, V_{out}_min = 280 V, P_{out} = 1600 W, the capacitance of the output capacitors is calculated to satisfy the holdup time of 0.02 s.

$$C_{out} = T_{hold} \times \frac{2 \times P_{out}}{({V_{out}}^2 - {V_{out\_min}}^2)}$$

In addition, when the output ripple specification is defined, the capacitance required to satisfy the output ripple specification must be calculated and compared with the capacitance that satisfies the hold-up time, and the large capacitance value must be used. In addition, tolerances and aging degradation must be considered when selecting a capacitor.

NOTE1: Hold-up time (T_{hold}):
It is from the time when input got cut off until the time when output voltage falls outside the operating range.

DESAT Circuit

DESAT detector protects the power semiconductor switch elements from load short-circuit current that can cause damage. When MOSFET's V_{DS} rises due to overcurrent caused by a load short circuit, etc., as shown in Fig. 4.8, DESAT current cannot flow into the MOSFET and the capacitor starts to get charged. When DESAT terminal exceeds DESAT threshold voltage, it is judged that an excessive current is flowing through the MOSFET, and the MOSFET is turned off.

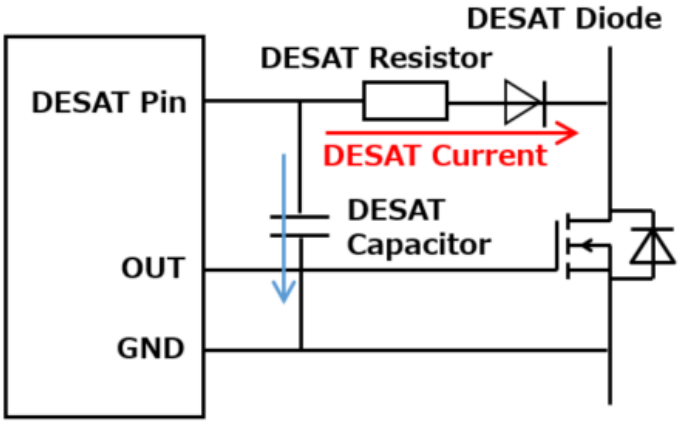


Fig. 4.8 DESAT Circuit

V_{DS} voltage used in DESAT protection function can be adjusted with DESAT diode (V_F) and DESAT resistor.

Detected V_{DS} voltage = DESAT voltage - (V_F+DESAT resistor × DESAT current)

Fig. 4.9 shows TK090N65Z's DESAT detection circuit and Fig. 4.10 shows TK62N60W5's DESAT detection circuit.

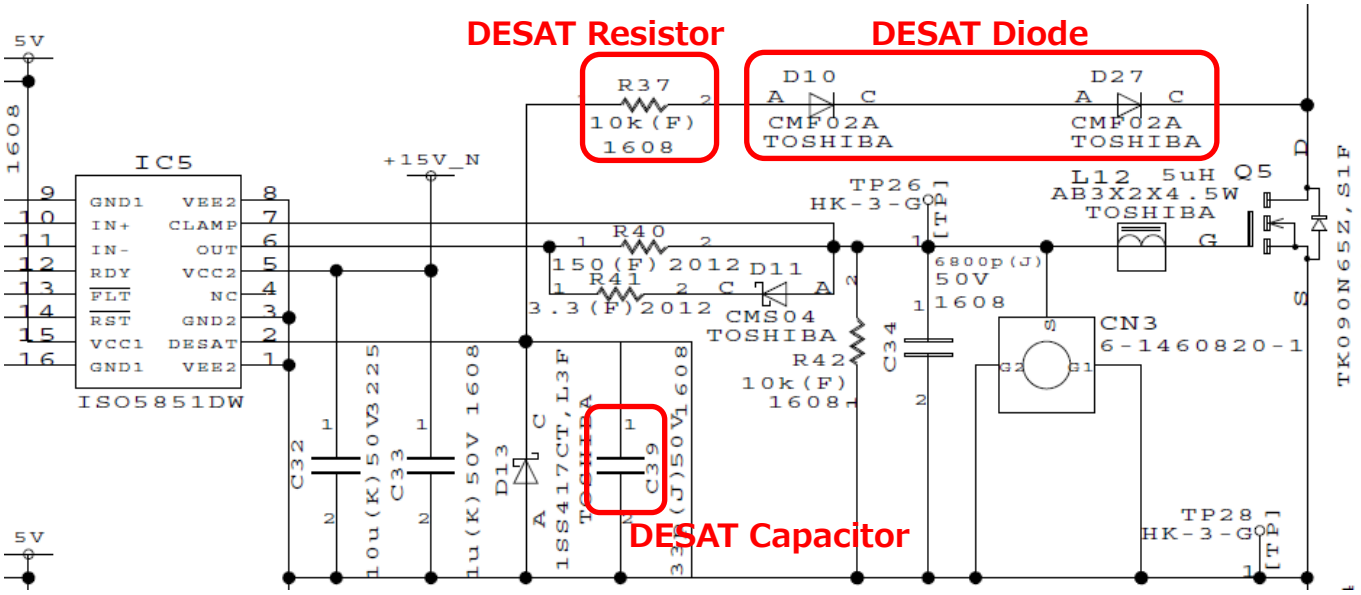


Fig. 4.9 TK090N65Z DESAT Detection Circuit

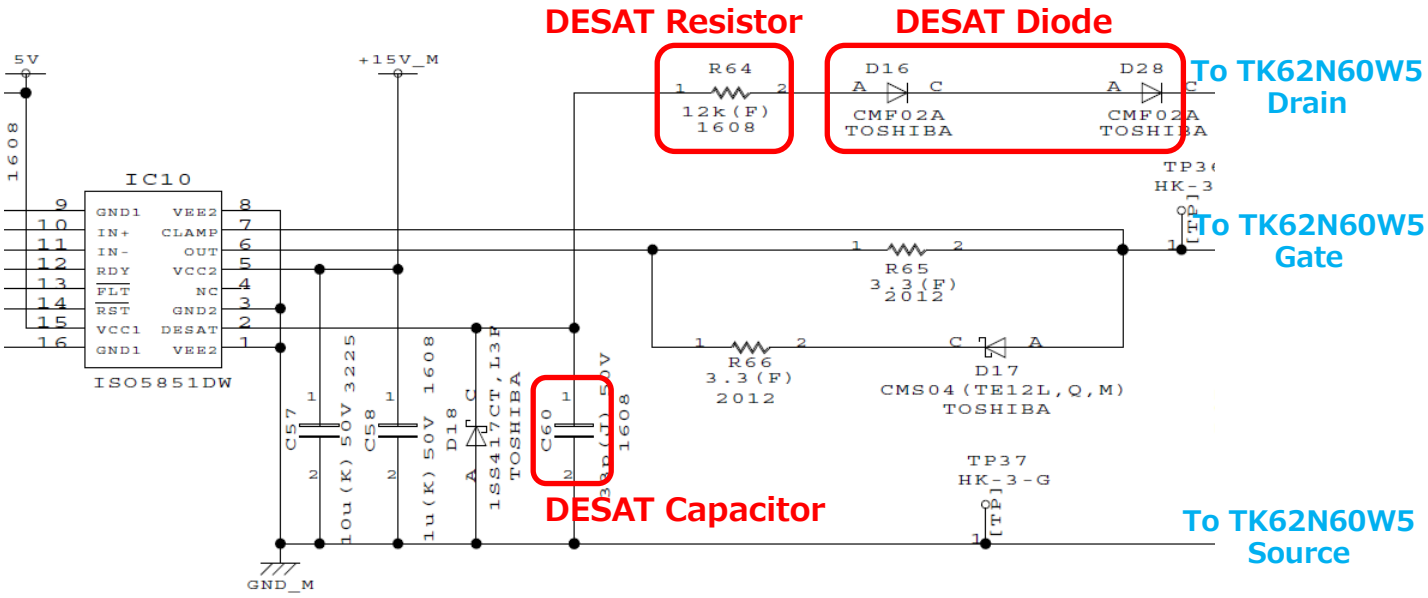


Fig. 4.10 TK62N60W5 DESAT Detection Circuit

Inductor Selection

This section explains how to select inductor (L3). The inductance value in this circuit can be calculated using the following items, which are power supply specifications.

- AC 200 V system input minimum voltage: V_{in_min} (V)
- DC output voltage: V_{out} (V)
- Switching frequency: F_c (Hz)
- Allowable ripple current width: ΔI_{ripple} (A)

Calculate the inductance value using the following formula.

$$L = \frac{\left(V_{out} - \sqrt{2} \times V_{in\_min}\right) \times V_{in\_min}}{F_c \times \Delta I_{ripple} \times V_{out}}$$

Here, assuming that the input voltage (V_{in_min}) of the AC line is 180 V, the output voltage (V_{out}) is 380 V, the switching frequency (F_c) is 100 kHz, and the allowable ripple current width is 5 A, the above equation shows that the calculated inductance value (L) is 119 μH. Therefore, the setting value of this power supply is 222 μH considering the margin.

In the actual design, the inductance value of the inductor varies depending on the DC bias characteristics. Select a component that can secure the above calculated value with the inductance value decreased due to DC bias characteristics.

Varistor

A varistor is installed to protect the system from surge voltage for example when an induced lightning surge, etc. occurs on the AC line. The maximum AC voltage is 264 V and considering margin a varistor with voltage of 470 V (423 to 517 V) is used. The varistor is used between the lines of the circuit, and a current fuse is placed in series before the varistor.

5. Product Overview

This section describes the products used in this circuit. Toshiba has prepared an extensive product lineups including MOSFET and SBD as shown below.

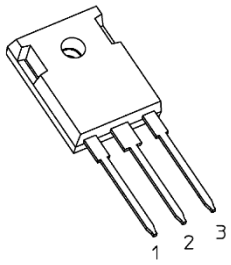
5.1. Power MOSFET TK090N65Z

Please click here for more information.

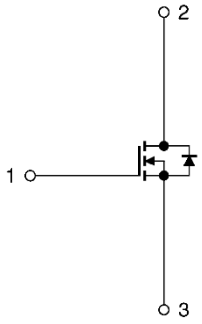
Features

- V_{DSS} = 650 V (max), I_D = 30 A (max)
- Low drain-source on-resistance: $R_{DS(ON)}$ = 0.075 Ω (typ.)
- High-speed switching properties with lower capacitance.
- Enhancement mode: V_{th} = 3 to 4 V (V_{DS} = 10 V, I_D = 1.27 mA)

Appearance and Terminal Arrangement



TO-247



1: Gate
2: Drain (Heatsink)
3: Source

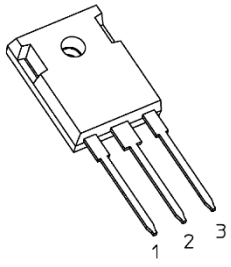
5.2. Power MOSFET TK62N60W5

Please click here for more information.

Features

- V_{DSS} = 600 V (max), I_D = 61.8 A (max)
- Fast reverse recovery time: t_{rr} = 170 ns (typ.)
- Low drain-source on-resistance: $R_{DS(ON)}$ = 0.036 Ω (typ.)
  by using Super Junction Structure : DTMOS
- Easy to control Gate switching
- Enhancement mode: V_{th} = 3 to 4.5 V (V_{DS} = 10 V, I_D = 3.1 mA)

Appearance and Terminal Arrangement



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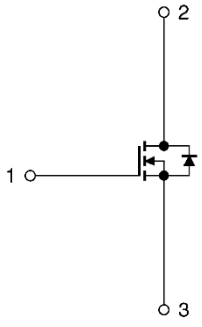


1: Gate
2: Drain (Heatsink)
3: Source

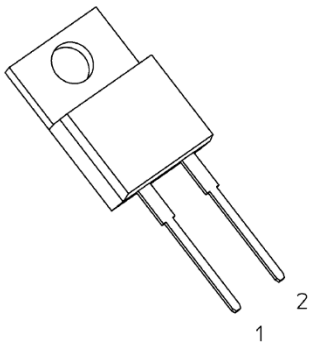
5.3. SiC Schottky Barrier Diode TRS6E65F

Please click here for more information.

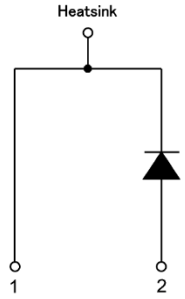
Features

- V_{RRM} = 650 V (max), $I_{F(DC)}$ = 6 A (max)
- High surge current capability: I_{FSM} = 55A (max)
- Low junction capacitance: C_j = 22 pF (typ.)
- Low reverse current: I_R = 0.3 μA (typ.)

Appearance and Terminal Arrangement



TO-220-2L



1: Cathode
2: Anode

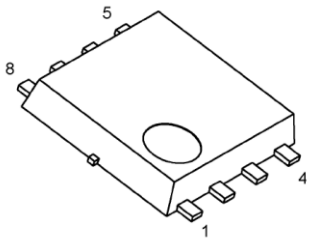
5.4. Power MOSFET TPHR9203PL

Please click here for more information.

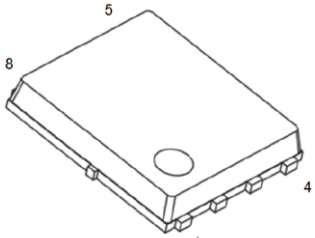
Features

- V_{DSS} = 30 V (max), I_D = 280 A (max)
- High-speed switching
- Small gate charge: Q_{SW} = 19 nC (typ.)
- Small output charge: Q_{oss} = 51 nC (typ.)
- Low drain-source on-resistance: $R_{DS(ON)}$ = 0.61 mΩ (typ.) (V_{GS} = 10 V)
- Low leakage current: I_{DSS} = 10 μA (max) (V_{DS} = 30 V)
- Enhancement mode: V_{th} = 1.1 to 2.1 V (V_{DS} = 10 V, I_D = 0.5 mA)

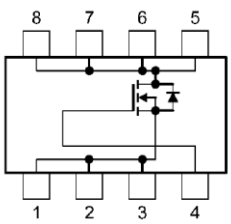
Appearance and Terminal Arrangement



SOP Advance



SOP Advance(N)



1, 2, 3: Source
4: Gate
5, 6, 7, 8: Drain

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