Non-Isolated Buck DC-DC Converter

Design Guide

RD205-DGUIDE-01

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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1. Introduction

This design guide describes how to design various circuitry for Non-Isolated Buck DC-DC Converter (hereafter referred to as this power supply). Refer to the reference guide for the specifications, use, and characteristic data of this power supply.

If a component is indicated as "Not Mounted" in the bill of materials, then it is not mounted on the PCB even if its part number is indicated in the circuit diagram. Mounting locations are provided on the PCB for constant value adjustment at the time of circuit design.

2. Non-Isolated Buck DC-DC Converter

A DC-DC converter converts DC (direct current) to DC (direct current). The step-down converter produces a voltage lower than the input voltage. Non-Isolated Buck DC-DC Converter share the GNDs on the input power side and the output side, and thus its input side and output side are electrically connected. In addition, it uses asynchronous rectification and synchronous rectification methods.

2.1. Asynchronous Rectification Method

Fig. 2.1 shows the circuit outline and operation of the asynchronous rectification method. In the asynchronous rectification method, when the high-side switch (Q1) is turned on, current flows through the inductor (L) to the output side as shown in Fig. 2.1 (a). At the same time, the energy determined by the current value and the inductance value of the Inductor (L) is stored in the inductor. While Q1 is on, the low-side switch (D1) is energized in the opposite direction, thus D1 does not conduct. When Q1 is turned off, L continues to carry current, and the stored energy is supplied to the output side as shown in Fig. 2.1 (b).

By repeating the operations in Fig. 2.1 (a) and (b), the voltage supplied from the input power supply is converted to the switching pulse voltage. When viewed from the input power side, power is supplied from the input only during the period shown in Fig. 2.1 (a), and power is not supplied from the input during the period shown in Fig. 2.1 (b). The supplied switching pulse output voltage is smoothed by L and the output capacitor (C_{out}) to produce a constant voltage. This is illustrated in Fig. 2.2.

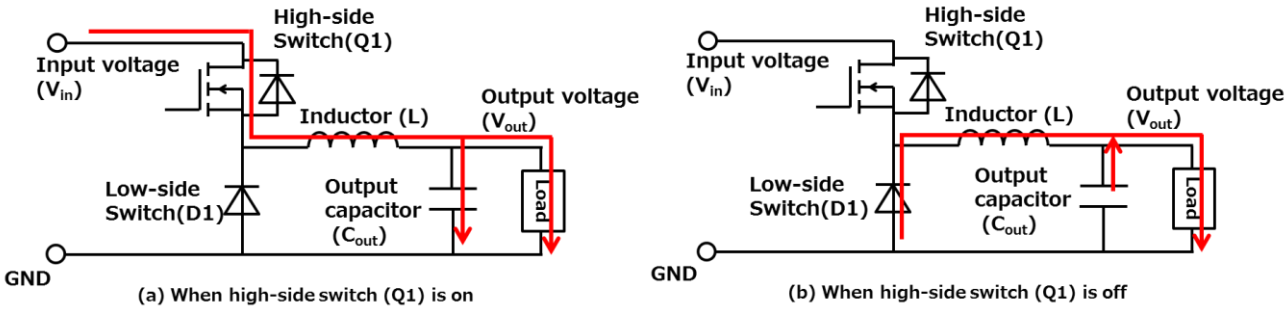

Fig. 2.1 Outline of Circuit of Asynchronous Rectification Method

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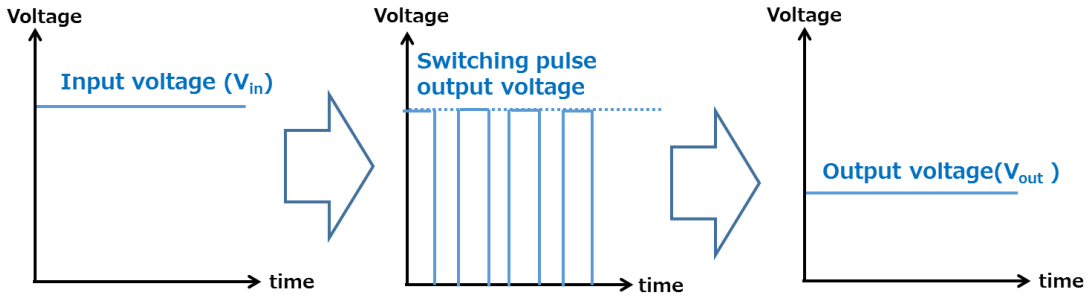

Fig. 2.2 Buck Converter Voltage

2.2. Synchronous Rectification Method

The synchronous rectification method has the same basic operation as the asynchronous rectification method, although a MOSFET rather than a diode is used for the low-side switch.

Fig. 2.3 shows the circuit outline and operation of the synchronous rectification method. In the synchronous rectification method, when the high-side switch (Q1) is turned on, current flows through the inductor (L) to the output side as shown in Fig. 2.3 (a). At the same time, the energy determined by the current value and the inductance value of L is stored in L. The low-side switch (Q2) is turned off while Q1 is on, thus becoming non-conductive. When Q1 is turned off, the energy stored in L is fed to the output side in the path shown in Fig. 2.3 (b), and Q2 is controlled so that it turns on at the same time Q1 turns off. A MOSFET is used instead of a diode in asynchronous rectification for the low-side switch, because it greatly improves the loss generated by the diode.

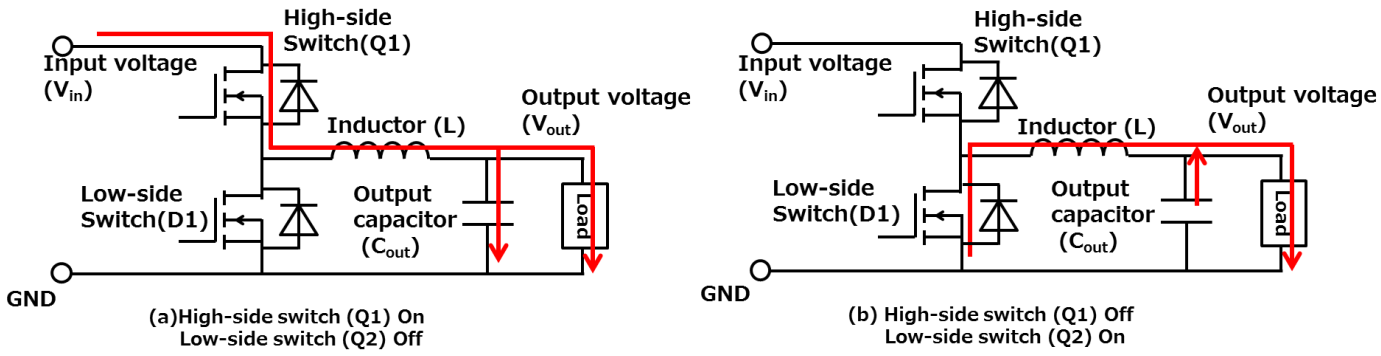

Fig. 2.3 Outline of Circuit of Synchronous Rectification Method

Comparing the loss of asynchronous and synchronous rectification, both asynchronous and synchronous rectification are equivalent in the on-period T_{on} of the high-side switch (Q1), but in the off-period T_{off}, current flows through the low-side switch (D1: diode) for asynchronous rectification and through the low-side switch (Q2: MOSFET) for synchronous rectification. The power consumed during T_{off} is shown below.

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Asynchronous rectification W (power) = $I \times V_F$ (diode forward voltage)

Synchronous rectification W (power) = $I^2 \times R$ (MOSFET on-resistance)

Generally, the power loss of asynchronous rectification is considerably larger than that of synchronous rectification. Although asynchronous rectification has the advantage of being easy to design because control of diodes (low-side switches) is unnecessary, in recent years, synchronous rectification is becoming mainstream because loss reduction has been emphasized.

2.3. Control of the Buck DC-DC Converter

The PWM (Pulse Width Modulation) control method is used as a control method to generate a constant voltage. The frequency is constant and controls the on-time (T_{on}) of the high-side switches (see Fig. 2.1 and Fig. 2.3) within the period. (The percentage of on-time per cycle is called Duty.) The control circuit monitors the output voltage, and controls the output voltage so that when the output voltage drops relative to the set voltage, Duty increases, and when the output voltage rises relative to the set voltage, Duty decreases, keeping the output voltage constant.

Output Voltage

For the circuit shown in Fig. 2.1 and Fig. 2.3, the period during which the high-side switch (Q1) is turned on is T_{on} and the period during which the high-side switch is turned off is T_{off}. Fig. 2.4 (a) shows the voltage and current waveforms of Q1 and inductor (L) at this time. When Q1 is on, (V_{in}-V_{out}) is applied at both ends of the inductor (L). When Q1 is off, V_{out} is applied. Therefore, the current ΔI_{on} of L that increases during T_{on} period shown in Fig. 2.4(b) and the current-ΔI_{off} of L that decreases during T_{off} period are expressed as follows.

Inductor current increase

$$\Delta I_{on} = \frac{1}{L} \times (V_{in} - V_{out}) \times T_{on}$$

Inductor current reduction

$$-\Delta I_{off} = \frac{1}{L} \times (V_{out}) \times T_{off}$$

When DC-DC converter operation is in the steady state, ΔI_{on} of the increase in the inductor current during T_{on} and -ΔI_{off} of the decrease in T_{off} period are equal, and the output voltage V_{out} from ΔI_{on} = -ΔI_{off} is expressed by the following equation.

$$V_{out} = V_{in} \times \frac{T_{on}}{T_{on}+T_{off}} \qquad \text{Equation(1)}$$

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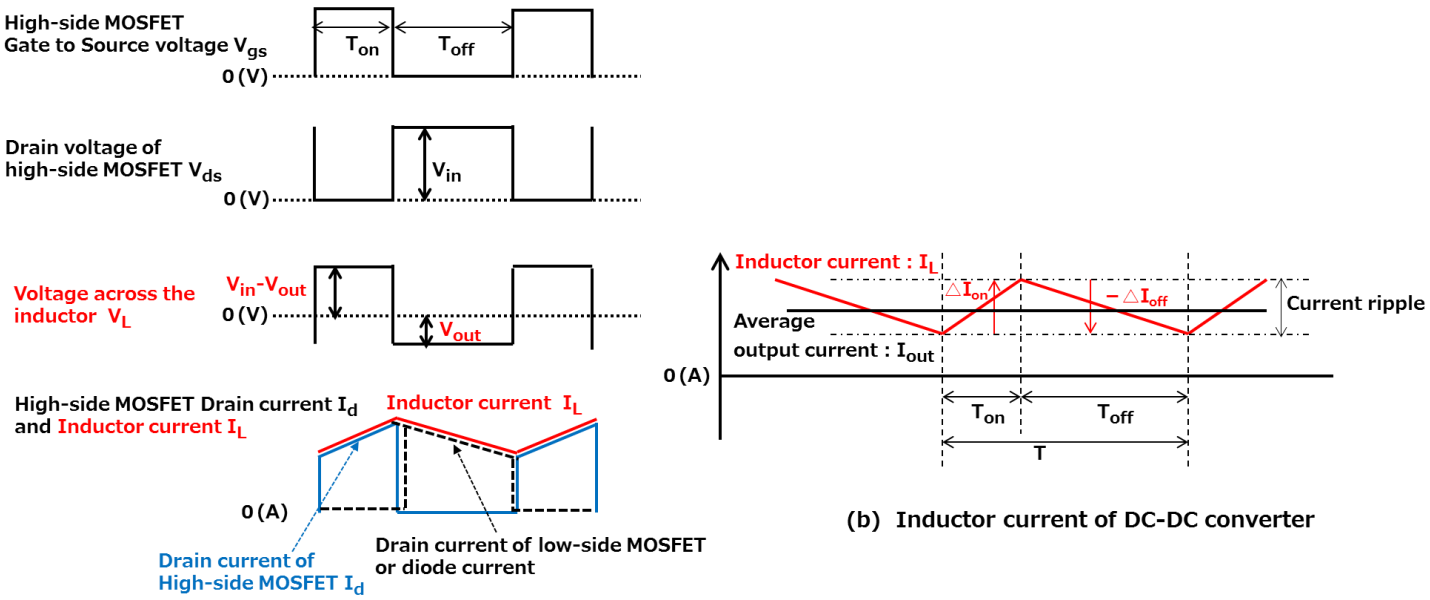

Fig. 2.4 DC-DC Converter Voltage/Current Waveforms

2.4. Continuous Current Mode and Discontinuous Current Mode

There are continuous current mode and discontinuous current mode for switching operation. The continuous current mode is a mode in which the inductor current flows continuously in the circuit shown in Fig. 2.1 and Fig. 2.3. If the output current I_{out} is greater than 1/2 of the increase/decrease (ripple current) ΔI of the inductor current I_L the continuous current mode is set, and if it is smaller the operation will be different between asynchronous rectification and synchronous rectification.

When the output current I_{out} is greater than 1/2 of the increment/decrement (ripple current) of the inductor current I_L

In the area where $I_{out} \geqq 1/2 \times \Delta I$ is satisfied, both asynchronous rectification and synchronous rectification are in continuous current mode. In particular, when $I_{out} = 1/2 \times \Delta I$, it is called boundary current mode. Fig. 2.5 shows the current I_L and current I_{out} waveforms. Ideally, the output voltage is independent of the output current and depends only on V_{in}, T_{on}, T_{off}, as shown in Equation (1) above.

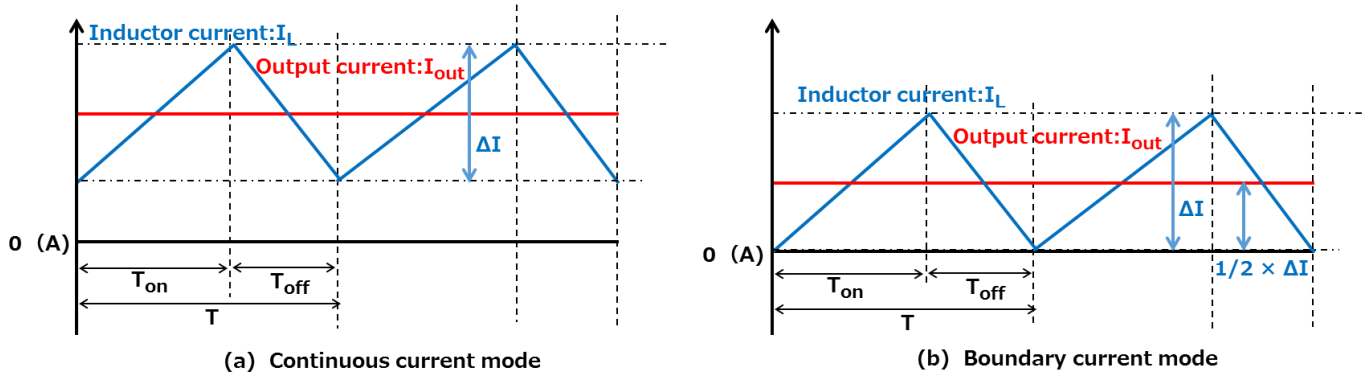

Fig. 2.5 Continuous Current Mode Waveform

When the output current I_{out} is less than 1/2 of the increment/decrement range (ripple current) of the inductor current I_L (ΔI)

The operation differs between asynchronous and synchronous rectification. In asynchronous rectification, as shown in Fig. 2.6 (a), there is a period in which the output current becomes zero because reverse flow of the inductor current cannot be performed by the diode (low-side switch). This is called discontinuous current mode. The output voltage equation (1) does not hold in the discontinuous current mode.

In synchronous rectification without reverse current prevention function, as shown in Fig. 2.6 (b), if the load current falls below half of the ripple current, a period in which the inductor current becomes negative occurs. That is, a current flows from V_{out} to the inductor. At this time, energy is stored in the inductor in the opposite direction. Even if the low-side switch is turned off and the high-side switch is turned on, current flows backwards from V_{out} to V_{in} through the inductor until the energy stored in the inductor reaches zero. In synchronous rectification with reverse current, the output voltage equation (1) is true because the system operates in the continuous current mode over the entire range of the output current.

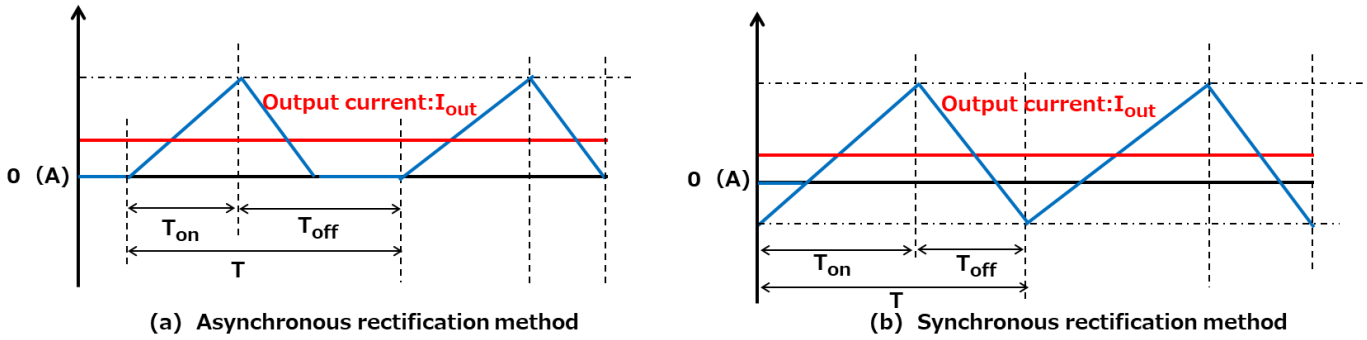

Fig. 2.6 Inductor Current at Light Load

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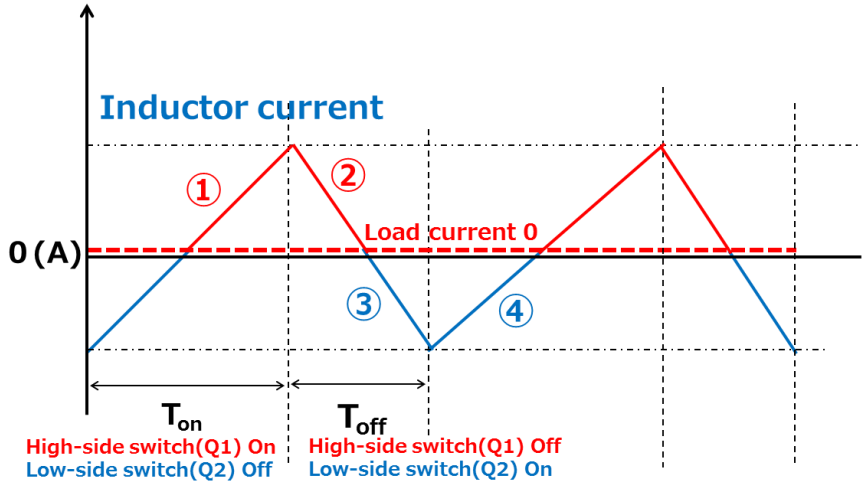
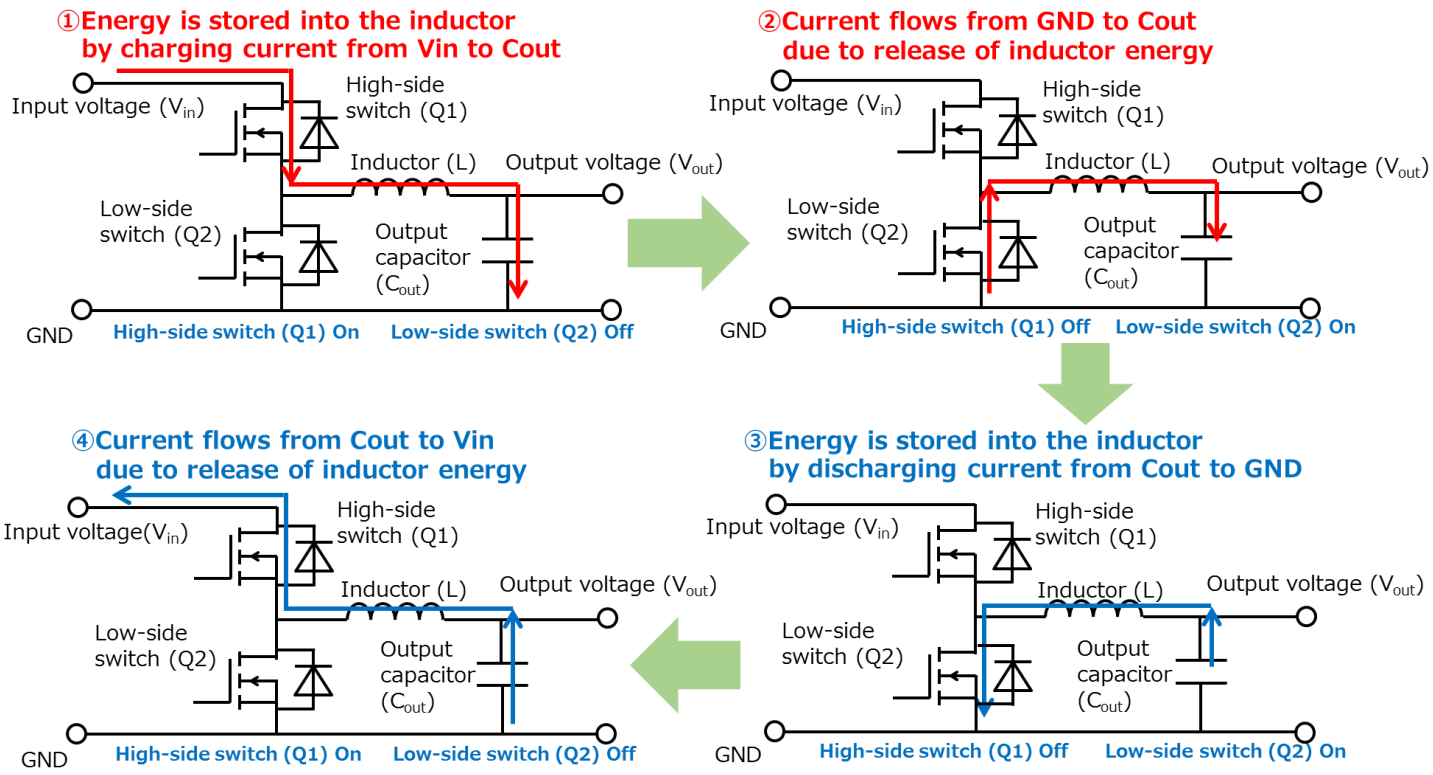
Fig. 2.7 (a) shows the inductor current waveform of the synchronous rectification method when the load current is zero. Fig. 2.7 (b) shows the reverse flow operation in the circuit that produces the waveform shown in Fig. 2.7 (a).



(a) Inductor Current Waveform of the Synchronous Rectification Method at No Load



(b) Synchronous Rectification Reverse Flow Operation at No Load

Fig. 2.7 Operation and Inductor Current of Synchronous Rectification Method at No Load

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2.5. Improving the Efficiency of the Synchronous Rectification Method under Light Load Conditions

In the synchronous rectification method, when the load current becomes half or less of the ripple current, a period in which the inductor current flows backward occurs as described in Fig. 2.6. This inductor reverse current flows through the high-side switch (Q1) and low-side switch (Q2), causing a loss due to the on-resistance of MOSFET and reducing the efficiency under light loads.

To eliminate this loss, a function is added to detect reverse inductor current and turn off the low-side switch (Q2). When the low-side switch (Q2) is turned off, the reverse current period of the inductor current is zero. If the inductor reverse current is prevented, the reverse current does not cause energy to accumulate in the inductor, and the inductor reverse current to the high-side switch (Q1) is not generated. The operation at this time is the same as the discontinuous current mode of asynchronous rectification.

Further Improvement of Efficiency at Light Load

DC-DC converter has been improved by the synchronous rectification method, while for light loads it has been improved by adding the anti-reverse flow function to the synchronous rectification method. PFM control further improves the efficiency during light loads.

PFM-Control (Pulse Frequency Modulation)

The PWM control of DC-DC converter keeps the switching period of the high-side MOSFET constant and changes the duty cycle. In contrast, the PFM keeps the on-time (T_{on}) of the switching pulse constant and vary the period depending on the loading.

Fig. 2.8 shows the operation waveforms of the PFM. When the load current is small, the frequency decreases (period increase) (a). And as the load current increases, the frequency increase (period decreases) (b). At light loads, the power consumed by DC-DC converter is not negligible for the power consumed by the load, resulting in a reduction in efficiency. For light loads, switching from PWM control to PFM control reduces switching losses by reducing the number of switching operations in response to a decrease in load current, thus improving efficiency.

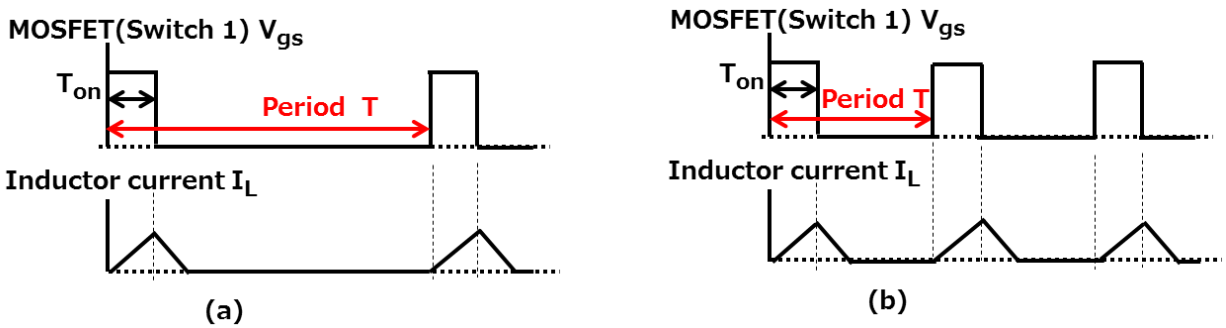

Fig. 2.8 PFM Control

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3. Circuit Design

This section describes the circuit design of this power supply.

3.1. Overview

In this power supply Analog Devices's LTC7803 (hereafter referred to as the controller) is used to configure the circuitry for the controller ICs.

Input is DC 12 V (±10 %), and 8 outputs are shown below. In addition, each output is further optimized in 3 ways, ① emphasis on efficiency at 100 % load, ② emphasis on efficiency at 50 % load, and ③ emphasis on compactness, leading to 24 design patterns. These optimizations are achieved by changing the switching frequency, inductor, and MOSFET.

Table 3.1 Power Supply Circuit Types

Input Voltage (V)	Output Voltage (V)	Max. Output Current (A)	Optimization
12	5	5	①efficiency at 100 % load
			②efficiency at 50 % load
			③compactness
		8	①efficiency at 100 % load
			②efficiency at 50 % load
			③compactness
		12	①efficiency at 100 % load
			②efficiency at 50 % load
			③compactness
	3.3	10	①efficiency at 100 % load
			②efficiency at 50 % load
			③compactness
		13.3	①efficiency at 100 % load
			②efficiency at 50 % load
			③compactness
		18.2	①efficiency at 100 % load
			②efficiency at 50 % load
			③compactness
	1.5	10	①efficiency at 100 % load
			②efficiency at 50 % load
			③compactness
	1.05	10	①efficiency at 100 % load
			②efficiency at 50 % load
			③compactness

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3.2. Circuit Design Explanation

This section describes the basic design points of this power supply. There are 24 design patterns, but since the same controller is used in all patterns, the explanation is based on one pattern i.e. 5 V/5 A optimized for ① efficiency at 100 % load. Fig. 3.1 shows the circuit. For detailed designs around the controller, refer to the datasheet of LTC7803 manufactured by Analog Devices and related documents.

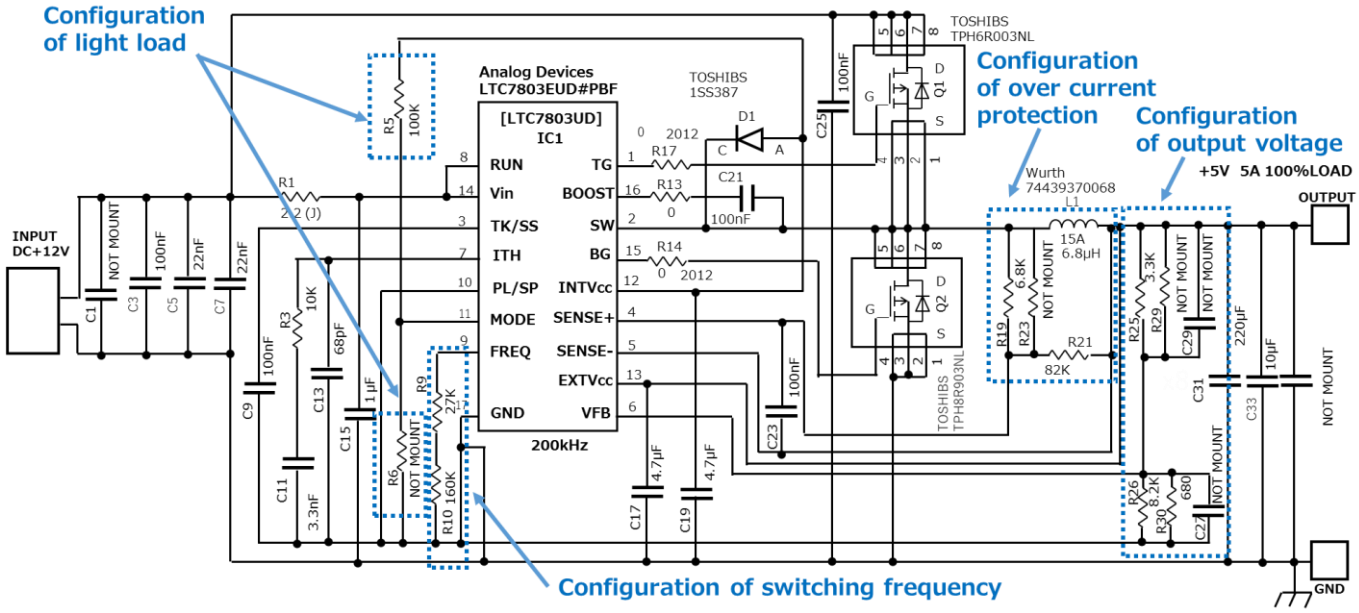

Fig. 3.1 Circuit of 5 V/5 A Optimized for ① Efficiency at 100% Load

Setting the Switching Frequency

The switching frequency is set using FREQ pin or PL/SP (PLLIN/SPREAD) pin. Set PL/SP pin to 0V and set the switching frequency (f_{osc}) using the resistance of the external resistors (R9, R10). Calculate the switching frequency (f_{osc}) using the following equation:

$$f_{osc}(kHz) = \frac{37MHz}{(R9 + R10)\Omega}$$

In this power supply, the switching frequency (f_{osc}) setting for the design optimized for ① efficiency at 100 % load and the design optimized for ② efficiency at 50% load is 197.9 kHz, and for the design optimized for ③ compactness is 596.8 kHz.

As shown in Fig. 3.2, 187 kΩ is selected as the resistance value (R9+R10) to set the frequency to approximately 200 kHz (197.9 kHz). To set to 600 kHz, select 62 kΩ for the resistance value (R9+R10). The frequency can be set from 100 kHz to 3 MHz.

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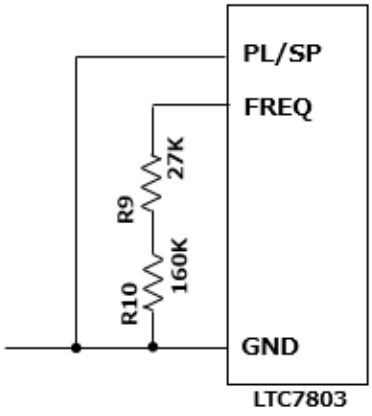

Fig. 3.2 Switching Frequency Setting

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Output Voltage Setting

Set the output voltage using the resistance value of the external resistors (R25, R29, R26, R30). Calculate the output voltage (V_{OUT}) using the following equation:

$$V_{OUT}(V) = 0.8 \times \left(1 + \frac{(R25//R29)}{(R26//R30)} \right)$$

For output voltage of 5 V, R25 is set as 3.3 kΩ, R29 is not mounted and to set R26//R30 as 628 Ω, R26 and R30 are selected as R26=8.2k Ω and R30=680 Ω as shown in Fig. 3.3.

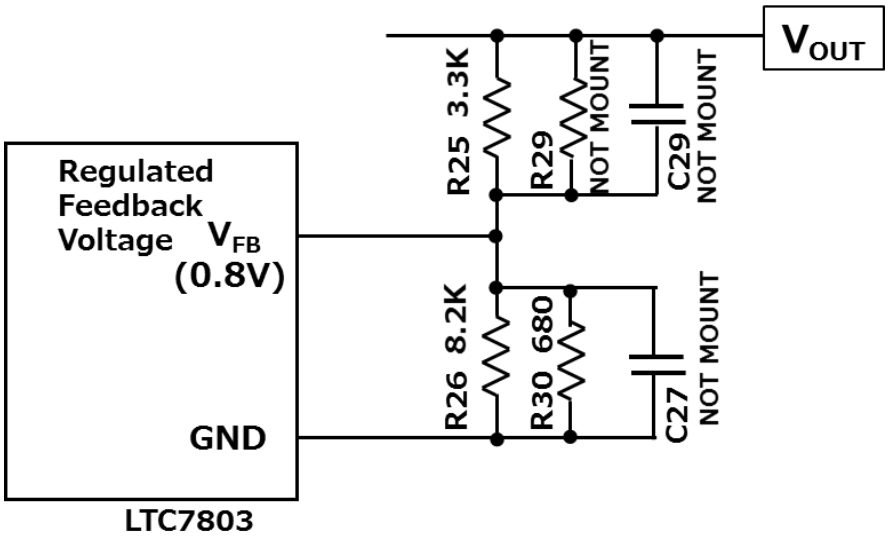

Fig. 3.3 Output Voltage Setting (Output Voltage 5V)

When the output voltage is set to +3.3 V, R25 = 3.3 kΩ, R29 is not mounted, R26 = 8.2 kΩ, and R30 = 1.2 kΩ.
When the output voltage is set to +1.0 V, R25 = 2.2 kΩ, R29 is not mounted, R26 = 10 kΩ, and R30 = 3.3 kΩ.
When the output voltage is set to +1.05 V, R25 = 3.3 kΩ, R29 is not mounted, R26 = 82 kΩ, and R30 = 12 kΩ.

Tolerance for the reference voltage 0.8 V (pin-4 FB terminal) is ±1.5 % for (-40 °C to 125 °C or 150 °C) and ±1.0 % for (0 ℃ to 85 ℃). It is necessary to consider both resistance tolerance and the reference voltage tolerance to set output voltages.

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Overcurrent Detection Setting

The controller can be configured to use either inductor resistance (DCR) sensing or sensing by adding a current sensing resistor. Either of the two current detection method can be selected. Inductor DCR sensing is selected when efficiency, mounting area, and cost are priorities. And, sensing by adding a current detection resistor is selected when overcurrent detection accuracy is priority.

In this power supply, detection by the DCR of the inductor is used. Thus the accuracy of overcurrent detection decreases, however output short protection is used as specification of this power supply without fixing the overcurrent detection range.

When detection by inductor DCR is used, adjustment using external resistor is required.

Calculate the overcurrent detection OC (A) and the external resistor R19 and R21 using the following equation.

$$OC\ \ (A) = \frac{V_{sense}}{R_{sense}} - \frac{\Delta I_L}{2}$$

V_{sense}: 50 mV

ΔI_L: Ripple current

(The peak value of the inductor-current is set, and the value obtained by subtracting half of the ripple current ΔI_L is the maximum average current.)

$$\Delta I_L(A) = \frac{1}{f_{osc} \times L} \times V_{out} \times (1 - \frac{V_{out}}{V_{in}})$$

In the above equation $(1 - \frac{V_{out}}{V_{in}})$ is low-side MOSFET Duty.

f_{osc} : switching frequency, 197.9 kHz

L : Inductance of the inductor, 6.8 μH

V_{out}: +5 V

V_{in} : +12 V

If the external (R19//R21) • C23 time constant is selected to be exactly equal to L1/DCR time constant, the voltage drop across the external voltage capacitor C23 is equal to the voltage drop across the DCR of the inductance multiplied by R21/(R19+R21).

$$R_{sense} = \frac{DCR_{at20\ ^\circ C} \times (R21)\ \ k\Omega}{(R19)\ \ k\Omega + (R21)\ \ k\Omega}$$

DCR at 20 °C : 4.1 mΩ

R19 : 6.8 kΩ, R21 : 82 kΩ

From the above equation, ΔI_L = 2.17 A, R_{sense} = 3.79, OC (MAX) (A) = 12.1 (A)

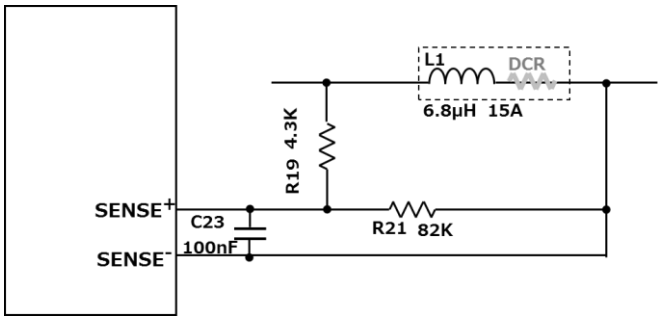

Fig. 3.4 Overcurrent Detection Setting

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Ripple Voltage Calculation

Set the output voltage ripple (V_{ripple}) to the requirement value by using the capacitance value (C_{out}) of the output capacitor. The resulting combined ripple voltage is the output voltage ripple (V_{ripple}).

1. Ripple voltage (V_{ripple_ESR}) generated by Ripple Current (ΔI_L) and Equivalent Serial Resistor Value (ESR) of Output Capacitor
2. Ripple voltage (V_{ripple_Cap}) generated by Ripple Current (ΔI_L), Capacitance of Output Capacitor (C_{out}), and Switching Frequency (f_{osc})
3. Ripple voltage (V_{ripple_ESL}) generated by switching voltage (V_{sw}), equivalent serial inductance (ESL) of output capacitor, and inductance (L)

Calculate each ripple voltage using the following equation.

$$V_{ripple\_ESR}(V) = \Delta I_L \times ESR$$

$$V_{ripple\_Cap}(V) = \frac{\Delta I_L}{8 \times C_{OUT} \times (f_{osc})}$$

$$V_{ripple\_ESL}(V) = \frac{V_{SW} \times ESL}{(L)}$$

ΔI_L is 2.17 A from last result, ESR is 0.82 mΩ (parallel of C31 : 3.1 mΩ and C33 : 1.11 mΩ).

V_{ripple_ESR} = 2.17 × 0.82 = 1.78 mV

C_{out} is, C31 : 220 µF, C33 : 10 µF, but considering DC bias characteristic, it is 58.2 µF + 4.5 µF = 62.7 µF.

F_{osc} = 197.9 kHz

V_{ripple_Cap} = 2.17 ÷ (8 × 62.7 µ × 197.9 k) = 21.9 mV

V_{sw} =12 V、L = 6.8 µH, ESL is 0.25 nH (parallel of C31 : 0.36 nH and C33 : 0.83 nH)

V_{ripple_ESL} =12 × 0.25 n ÷ 6.8 µ = 0.44 mV

V_{ripple_Cap} = 1.78 m + 21.9 m + 0.44 m ≒ 24.1 mV

Since the ripple voltage generated by V_{ripple_Cap} is out of phase with V_{ripple_ESR}, V_{ripple_ESL}, the simple sum is used as a guideline for the output voltage ripple.

Adjust COUT, ESR, and ESL of the output capacitor so that the output voltage ripple V_{ripple} satisfies the required specifications. Also check the following:

1. The output terminal undershoot and overshoot (that occur when the load changes suddenly) falls within the specified voltage range.
2. The allowable ripple current of the output capacitor is ensured.
3. Tolerance and aging of the output capacitors, tolerances including DC superimposition characteristics of the inductor (L), and tolerances of other components shall be considered.

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Inductor Selection

There is a correlation between switching frequency and inductor selection in the sense that the higher the switching frequency, the smaller inductor can be used. If efficiency is priority, then lower the switching frequency and select an inductor with a low DC resistance (higher rated current). If compactness is priority, increase the switching frequency and select an inductor with a small value. The switching frequency can be set between 100 kHz and 3 MHz for the controller, but 197.9 kHz is set for the both designs optimized for ① efficiency at 100 % and ② efficiency at 50% load, and 596.8 kHz is set for the design optimized for ③ compactness on this power supply.

Below is a list of the Wurth Elektlonik's inductors used this time.

Table 3.2 Inductor List

Output (V/A)	Optimization	Inductor P/N	Specification (μH/A)	Size (mm)
5/5	①efficiency at 100 % load	74439370068	6.8/15	16.4 x 15.4
	②efficiency at 50 % load	74439370068	6.8/15	16.4 x 15.4
	③compactness	744314200	2/11.5	6.9 x 6.9
5/8	①efficiency at 100 % load	74439369033	3.3/15	11.6 x 10.5
	②efficiency at 50 % load	74439369033	3.3/15	11.6 x 10.5
	③compactness	7443340150	1.5/16.5	8.4 x 7.9
5/12	①efficiency at 100 % load	74439369033	3.3/15	11.6 x 10.5
	②efficiency at 50 % load	74439369033	3.3/15	11.6 x 10.5
	③compactness	7443340100	1/17	8.4 x 7.9
3.3/10	①efficiency at 100 % load	7443630310	3.1/26	21.8 x 21.5
	②efficiency at 50 % load	7443630310	3.1/26	21.8 x 21.5
	③compactness	744311100	1/15	7.0 x 6.9
3.3/13.3	①efficiency at 100 % load	7443630310	3.1/26	21.8 x 21.5
	②efficiency at 50 % load	7443630310	3.1/26	21.8 x 21.5
	③compactness	7443340068	0.68/19	8.4 x 7.9
3.3/18.2	①efficiency at 100 % load	7443630310	3.1/26	21.8 x 21.5
	②efficiency at 50 % load	7443630310	3.1/26	21.8 x 21.5
	③compactness	7443320047	0.47/26	12.1 x 11.4
1.5/10	①efficiency at 100 % load	7443310150	1.5/18.5	12.1 x 11.4
	②efficiency at 50 % load	7443310150	1.5/18.5	12.1 x 11.4
	③compactness	744323033	0.33/18	10.6 x 10.6
1.05/10	①efficiency at 100 % load	74439369022	2.2/16	11.6 x 10.5
	②efficiency at 50 % load	74439369022	2.2/16	11.6 x 10.5
	③compactness	744316047	0.47/15	5.3 x 5.6

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Operation Setting at Light Load

High-efficiency Burst Mode operation, pulse skip mode, or forced continuous conduction mode can be selected in this power supply at light load current. This power supply is set to pulse skip mode.

Selection Method

Burst Mode Operation

R5 : Mounting is Not required,

R6 : 0 Ω (i.e. MODE pin. and GND are connected)

Pulse Skip Mode

R5 : 100 kΩ (MODE pin and $INTV_{CC}$ pin are connected through a 100 kΩ resistor),

R6 : Mounting is not required.

Forced Continuous Conduction Mode

R5 : 0 Ω (i.e. MODE pin and $INTV_{CC}$ pin are connected,

R6 : Mounting is not required.

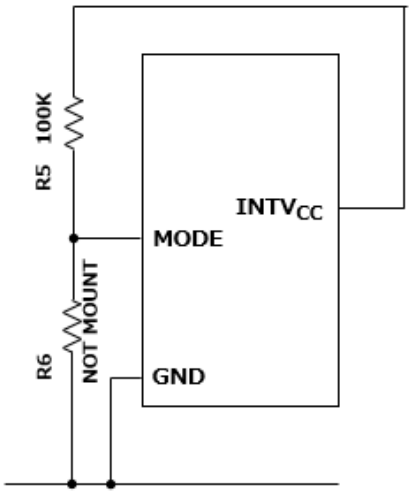

Fig. 3.5 Operation Setting at Light Load

Pin 13 : EXTVcc

Supplying a voltage of 4.7 V or more to this terminal will increase efficiency because the linear voltage regulator built into the controller is turned off. With this power supply, the output voltage is connected to the pin 13 (EXTVcc) only for +5 V output design.

Precautions

The pin assignment of the controller LTC7803 vary according to its package. This power supply design shows the pin assignment of the QFN package.

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4. MOSFET Selection

The two N-channel MOSFET (high-side and low-side) used for this power supply are selected considering the following:

① Since this power supply is a 12 V step-down converter, V_{DSS} is chosen to be 30 V.

② The high-side and low-side MOSFET driving voltages are set by the controller's $INTV_{CC}$ voltage and are typically 5.15 V at startup. Therefore, the logic-level drive MOSFET is selected.

③ MOSFET requires different properties between the high-side MOSFET and the low-side MOSFET.

The high-side MOSFET performs the switching operation, and the low-side MOSFET performs the synchronous rectification operation.

High-side MOSFET

In the high-side MOSFET, switching loss is the most critical feature, and high-speed performance is required. Because the switching frequency is as high as several hundred kHz, the switching loss accounts for a large percentage of the total loss.

The conduction loss varies greatly depending on the I/O voltage ratio and load conditions. However, since the I/O voltage ratio is the on-duty ratio of MOSFET, it increases as the I/O voltage ratio increases. The conduction loss increases in proportion to the square of the current (the switching loss increases in proportion to the approximate current), so it increases as the load current increases.

In light loads, since the loss at output capacitance and gate capacitance due to switching affects the efficiency, it is also important.

Low-side MOSFET

The low-side MOSFET has almost no switching loss because of zero-volt switching due to synchronous rectification operation. Consequently, continuity loss is the majority of the total loss, and thus the low $R_{ds(on)}$ property is the most critical.

When the high-side MOSFET is turned on, the loss occurs due to the reverse-recovery current of the low-side MOSFET body diode, therefore the body diode properties are also crucial.

In light loads, the current is small, so there is almost no conduction loss, and most of the loss occurs due to the capacitance of the MOSFET (including the body diode) and is caused by switching.

④ Emphasis on Compactness

By increasing the switching frequency, components such as inductor are made smaller, and by selecting MOSFET of small packages, the power supply is made smaller. The switching performance of the high-side MOSFET becomes more significant because the switching loss of the high-side MOSFET increases as the switching frequency increases.

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Table 4.1 lists MOSFET products selected for each design pattern. And, Fig. 4.1 shows the efficiency curve for three optimizations, which are ① efficiency at 100% load, ② efficiency at 50% load, and ③ compactness for the design pattern with output of 3.3 V, 10 A and with MOSFETs selected this time as a reference.

Table 4.1 List of MOSFETs Used

Output (V/A)	Optimization	Fc (kHz)	MOSFETs used			
			High-side	$R_{ds(on)}$@4.5 V (mΩ)(max) /C_{iss} (pF)(typ) /Package	Low-side	$R_{ds(on)}$@4.5 V (mΩ)(max) /C_{iss} (pF)(typ) /Package
5/5	①efficiency at 100 % load	197.9	TPH11003NL	16/510/SOP Advance	TPH8R903NL	12.7/630/SOP Advance
	②efficiency at 50 % load	197.9	TPH11003NL	16/510/SOP Advance	TPH11003NL	16/510/SOP Advance
	③compactness	596.8	TPN11003NL	16/510/TSON Advance	TPN8R903NL	12.7/630/TSON Advance
5/8	①efficiency at 100 % load	197.9	TPH4R003NL	6.2/1110/SOP Advance	TPH2R903PL	4.1/1780/SOP Advance
	②efficiency at 50 % load	197.9	TPH8R903NL	12.7/630/SOP Advance	TPH4R803PL	6.2/1520/SOP Advance
	③compactness	596.8	TPN8R903NL	12.7/630/TSON Advance	TPN5R203PL	6.4/1520/TSON Advance
5/12	①efficiency at 100 % load	197.9	TPH4R003NL	6.2/1110/SOP Advance	TPH2R003PL	2.6/4930/SOP Advance
	②efficiency at 50 % load	197.9	TPH4R003NL	6.2/1110/SOP Advance	TPH4R803PL	6.2/1520/SOP Advance
	③compactness	596.8	TPN4R303NL	6.3/1110/TSON Advance	TPN2R903PL	4.1/1730/TSON Advance
3.3/10	①efficiency at 100 % load	197.9	TPH4R003NL	6.2/1110/SOP Advance	TPH2R003PL	2.6/4930/SOP Advance
	②efficiency at 50 % load	197.9	TPH4R003NL	6.2/1110/SOP Advance	TPH4R803PL	6.2/1520/SOP Advance
	③compactness	596.8	TPN4R303NL	6.3/1110/TSON Advance	TPN2R903PL	4.1/1730/TSON Advance
3.3/13.3	①efficiency at 100 % load	197.9	TPH4R003NL	6.2/1110/SOP Advance	TPHR9203PL1	1.29/5800/SOP Advance
	②efficiency at 50 % load	197.9	TPH4R003NL	6.2/1110/SOP Advance	TPH2R903PL	4.1/1780/SOP Advance
	③compactness	596.8	TPN4R303NL	6.3/1110/TSON Advance	TPN2R903PL	4.1/1730/TSON Advance
3.3/18.2	①efficiency at 100 % load	197.9	TPH3R203NL	4.7/1600/SOP Advance	TPHR6503PL1	0.89/7700/SOP Advance
	②efficiency at 50 % load	197.9	TPH4R003NL	6.2/1110/SOP Advance	TPH2R003PL	2.6/4930/SOP Advance
	③compactness	596.8	TPN4R303NL	6.3/1110/TSON Advance	TPN1R603PL	2.5/2970/TSON Advance
1.5/10	①efficiency at 100 % load	197.9	TPH8R903NL	12.7/630/SOP Advance	TPH2R003PL	2.6/4930/SOP Advance
	②efficiency at 50 % load	197.9	TPH8R903NL	12.7/630/SOP Advance	TPH4R803PL	6.2/1520/SOP Advance
	③compactness	596.8	TPN8R903NL	12.7/630/TSON Advance	TPN2R903PL	4.1/1730/TSON Advance
1.05/10	①efficiency at 100 % load	197.9	TPH8R903NL	12.7/630/SOP Advance	TPH2R003PL	2.6/4930/SOP Advance
	②efficiency at 50 % load	197.9	TPH8R903NL	12.7/630/SOP Advance	TPH4R803PL	6.2/1520/SOP Advance
	③compactness	596.8	TPN8R903NL	12.7/630/TSON Advance	TPN2R903PL	4.1/1730/TSON Advance

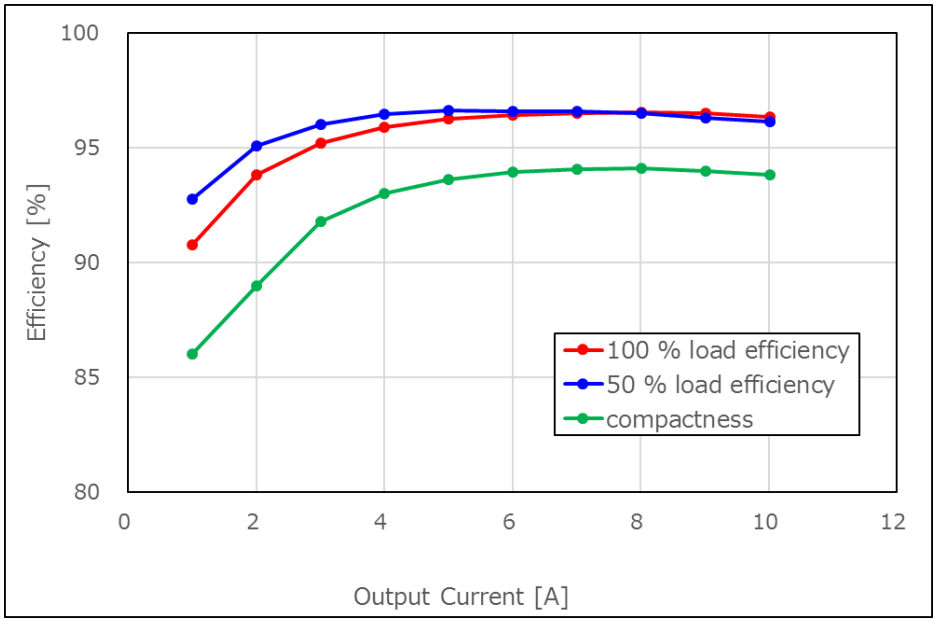

Fig. 4.1 Output 3.3 V/10A designs Efficiency

Appendix

The calculated values for all 24-design patterns of the power supply in this design are as follows.

5 V Output, total 9 circuits

	Optimization		5 V/5 A			5 V/8 A			5 V/12 A		
			①Optimized for 100% load	②Optimized for 50% load	③Optimized for compactness	①Optimized for 100% load	②Optimized for 50% load	③Optimized for compactness	①Optimized for 100% load	②Optimized for 50% load	③Optimized for compactness
Switching Frequency	Rfreq	[kΩ]	187	187	62	187	187	62	187	187	62
	fosc=	[kHz]	197.9	197.9	596.8	197.9	197.9	596.8	197.9	197.9	596.8
Output Current	RB	[kΩ]	3.3	3.3	3.3	3.3	3.3	3.3	3.3	3.3	3.3
	RA-1	[kΩ]	8.2	8.2	8.2	8.2	8.2	8.2	8.2	8.2	8.2
	RA-2	[kΩ]	0.68	0.68	0.68	0.68	0.68	0.68	0.68	0.68	0.68
	RA(total)	[kΩ]	0.628	0.63	0.63	0.63	0.63	0.63	0.63	0.63	0.63
	Vout=	[V]	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00
Over Current Protection	P/N of Wurth		74439370068	74439370068	744314200	74439369033	74439369033	7443340150	74439369033	74439369033	7443340100
	Size		16.4 x 15.4	16.4 x 15.4	6.9 x 6.9	11.6 x 10.5	11.6 x 10.5	8.4 x 7.9	11.6 x 10.5	11.6 x 10.5	8.4 x 7.9
	Rated Current	[A]	15	15	11.5	15	15	16.5	15	15	17
	L	[µH]	6.8	6.8	2	3.3	3.3	1.5	3.3	3.3	1
Input Voltage	Vin	[V]	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00
Ripple Current	ΔIL=	[A]	2.17	2.17	2.44	4.47	4.47	3.26	4.47	4.47	4.89
Max. Output Current	Iout	[A]	5	5	5	8	8	8	12	12	12
Peak Current of L	Ilpeak=	[A]	6.08	6.08	6.22	10.23	10.23	9.63	14.23	14.23	14.44
	Vsense(typ)	[mV]	50	50	50	50	50	50	50	50	50
	DCR(at 20℃)	[mΩ]	4.10	4.10	5.85	3.40	3.40	5.30	3.40	3.40	2.95
	Rs1	[kΩ]	4.3	4.3	1.5	2.4	2.4	1.5	3.0	3.0	1.5
	Rs2	[kΩ]									
	Rs1//Rs2	[kΩ]	4.3	4.3	1.5	2.4	2.4	1.5	3.0	3.0	1.5
	Rp	[kΩ]	Not Mounted	Not Mounted	Not Mounted	Not Mounted	Not Mounted	6.8	12.0	12.0	6.2
	Rsense		4.10	4.10	5.85	3.40	3.40	4.34	2.72	2.72	2.38
	OC(typ)	[A]	11.11	11.11	7.32	12.47	12.47	9.89	16.15	16.15	18.61
(Ref.) ΔIL of Short Current	ΔIL(SC)	[A]	0.07	0.07	0.24	0.15	0.15	0.32	0.15	0.15	0.48
(Ref.) Ave. Short Current	IL(SC)	[A]	4.41	4.41	2.81	4.92	4.92	3.79	6.39	6.39	7.20
Ripple Voltage Calculation	esr-1	[mΩ]	1.11	1.11	1.11	1.11	1.11	1.11	1.11	1.11	1.11
	Capacitance-1	[µF]	4.485	4.485	4.485	4.485	4.485	4.485	4.485	4.485	4.485
	esl-1	[nH]	0.83	0.83	0.83	0.83	0.83	0.83	0.83	0.83	0.83
	esr-2	[mΩ]	3.1	3.1	3.1	3.1	3.1	3.1	3.1	3.1	3.1
	Capacitance-2	[µF]	58.241	58.241	58.241	58.241	58.241	58.241	58.241	58.241	58.241
	esl-2	[nH]	0.36	0.36	0.36	0.36	0.36	0.36	0.36	0.36	0.36
	Total esr	[mΩ]	0.82	0.82	0.82	0.82	0.82	0.82	0.82	0.82	0.82
	Total Capacitance	[µF]	62.7	62.7	62.7	62.7	62.7	62.7	62.7	62.7	62.7
	Total esl	[nH]	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25
	Vr(esr)	[mV]	1.77	1.77	2.00	3.65	3.65	2.66	3.65	3.65	4.00
	Vr(cap)	[mV]	21.84	21.84	8.16	45.00	45.00	10.88	45.00	45.00	16.32
	Vr(ESL)	[mV]	0.44	0.44	1.51	0.91	0.91	2.01	0.91	0.91	3.01
	Vr(Total)	[mV]	24.05	24.05	11.67	49.57	49.57	15.56	49.57	49.57	23.33
	Target Ripple	[mV]	300	300	300	300	300	300	300	300	300

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3.3 V Output, total 9 circuits

	Optimization		3. 3V/10 A			3.3 V/13.3 A			3.3 A/18.2 A		
			①Optimized for 100% load	②Optimized for 50% load	③Optimized for compactness	①Optimized for 100% load	②Optimized for 50% load	③Optimized for compactness	①Optimized for 100% load	②Optimized for 50% load	③Optimized for compactness
Switching Frequency	Rfreq	[kΩ]	187	187	62	187	187	62	187	187	62
	fosc=	[kHz]	197.9	197.9	596.8	197.9	197.9	596.8	197.9	197.9	596.8
Output Current	RB	[kΩ]	3.3	3.3	3.3	3.3	3.3	3.3	3.3	3.3	3.3
	RA-1	[kΩ]	8.2	8.2	8.2	8.2	8.2	8.2	8.2	8.2	8.2
	RA-2	[kΩ]	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2
	RA(total)	[kΩ]	1.05	1.05	1.05	1.05	1.05	1.05	1.05	1.05	1.05
	Vout=	[V]	3.32	3.32	3.32	3.32	3.32	3.32	3.32	3.32	3.32
Over Current Protection	P/N of Wurth		7443630310	7443630310	744311100	7443630310	7443630310	7443340068	7443630310	7443630310	7443320047
	Size		18.2 x 18.2	18.2 x 18.2	6.9 x 6.9	18.2 x 18.2	18.2 x 18.2	8.4 x 7.9	18.2 x 18.2	18.2 x 18.2	12.1 x 11.4
	Rated Current	[A]	26	26	15	26	26	19	26	26	26
	L	[μH]	3.1	3.1	0.78	3.1	3.1	0.68	3.1	3.1	0.47
Input Voltage	Vin	[V]	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00
Ripple Current	ΔIL=	[A]	3.92	3.92	5.16	3.92	3.92	5.92	3.92	3.92	8.56
Max. Output Current	Iout	[A]	10	10	10	13.3	13.3	13.3	18.2	18.2	18.2
Peak Current of L	Ilpeak=	[A]	11.96	11.96	12.58	15.26	15.26	16.26	20.16	20.16	22.48
	Vsense(typ)	[mV]	50	50	50	50	50	50	50	50	50
	DCR(at 20℃)	[mΩ]	2.09	2.09	4.60	2.09	2.09	1.72	2.09	2.09	1.85
	Rs1	[kΩ]	3.3	3.3	1.3	3.3	3.3	1.8	3.30	3.30	1.5
	Rs2	[kΩ]									
	Rs1//Rs2	[kΩ]	3.3	3.3	1.3	3.3	3.3	1.8	3.3	3.3	1.5
	Rp	[kΩ]	Not Mounted	Not Mounted	3.9	Not Mounted	Not Mounted	Not Mounted	Not Mounted	Not Mounted	Not Mounted
	Rsense		2.09	2.09	3.45	2.09	2.09	1.72	2.09	2.09	1.85
	OC(typ)	[A]	21.97	21.97	11.91	21.97	21.97	26.11	21.97	21.97	22.74
(Ref.) ΔIL of Short Current	ΔIL(SC)	[A]	0.15	0.15	0.62	0.15	0.15	0.71	0.15	0.15	1.02
(Ref.) Ave. Short Current	IL(SC)	[A]	8.71	8.71	4.46	8.71	8.71	10.09	8.71	8.71	8.59
Ripple Voltage Calculation	esr-1	[mΩ]	1.11	1.11	1.11	1.11	1.11	1.11	1.11	1.11	1.11
	Capacitance-1	[μF]	6.168	6.168	6.168	6.168	6.168	6.168	6.168	6.168	6.168
	esl-1	[nH]	0.83	0.83	0.83	0.83	0.83	0.83	0.83	0.83	0.83
	esr-2	[mΩ]	3.1	3.1	3.1	3.1	3.1	3.1	3.1	3.1	3.1
	Capacitance-2	[μF]	82.099	82.099	82.099	82.099	82.099	82.099	82.099	82.099	82.099
	esl-2	[nH]	0.36	0.36	0.36	0.36	0.36	0.36	0.36	0.36	0.36
	Total esr	[mΩ]	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8
	Total Capacitance	[μF]	88.3	88.3	88.3	88.3	88.3	88.3	88.3	88.3	88.3
	Total esl	[nH]	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25
	Vr(esr)	[mV]	3.20	3.20	4.22	3.20	3.20	4.84	3.20	3.20	7.00
	Vr(cap)	[mV]	28.03	28.03	12.25	28.03	28.03	14.05	28.03	28.03	20.32
	Vr(ESL)	[mV]	0.97	0.97	3.86	0.97	0.97	4.43	0.97	0.97	6.41
	Vr(Total)	[mV]	32.21	32.21	20.33	32.21	32.21	23.32	32.21	32.21	33.74
	Target Ripple	[mV]	200	200	200	200	200	200	200	200	200

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1.5 V Ouput, total 3 circuits and 1.05 V output, total 3 circuits

			1.5 V/5 A			1.05 V/5 A		
	Optimization		①Optimized for 100% load	②Optimized for 50% load	③Optimized for compactness	①Optimized for 100% load	②Optimized for 50% load	③Optimized for compactness
Switching Frequency	Rfreq	[kΩ]	187	187	62	187	187	62
	fosc=	[kHz]	197.9	197.9	596.8	197.9	197.9	596.8
Output Current	RB	[kΩ]	2.2	2.2	2.2	3.3	3.3	3.3
	RA-1	[kΩ]	10	10	10	82	82	82
	RA-2	[kΩ]	3.3	3.3	3.3	12	12	12
	RA(total)	[kΩ]	2.48	2.48	2.48	10.47	10.47	10.47
	Vout=	[V]	1.51	1.51	1.51	1.05	1.05	1.05
Over Current Protection	P/N of Wurth		7443310150	7443310150	744323033	74439369022	74439369022	744316047
	Size		21.8 x 21.5	21.8 x 21.5	10.6 x 10.6	12.1 x 11.4	12.1 x 11.4	5.3 x 5.5
	Rated Current	[A]	19.5	19.5	18	16	16	15
	L	[µH]	1.5	1.5	0.33	2.2	2.2	0.47
Input Voltage	Vin	[V]	12.00	12.00	12.00	12.00	12.00	12.00
Ripple Current	ΔIL=	[A]	4.45	4.45	6.70	2.21	2.21	3.42
Max. Output Current	Iout	[A]	10	10	10	10	10	10
Peak Current of L	Ilpeak=	[A]	12.22	12.22	13.35	11.10	11.10	11.71
	Vsense(typ)	[mV]	50	50	50	50	50	50
	DCR(at 20℃)	[mΩ]	2.80	2.80	2.17	2.20	2.20	2.75
	Rs1	[kΩ]	3.30	3.30	1.50	2.2	2.2	1.6
	Rs2	[kΩ]						
	Rs1//Rs2	[kΩ]	3.3	3.3	1.5	2.2	2.2	1.6
	Rp	[kΩ]	Not Mounted	Not Mounted	Not Mounted	Not Mounted	Not Mounted	Not Mounted
	Rsense		2.80	2.80	2.17	2.20	2.20	2.75
	OC(typ)	[A]	15.63	15.63	19.69	21.62	21.62	16.47
(Ref.) ΔIL of Short Current	ΔIL(SC)	[A]	0.32	0.32	1.45	0.22	0.22	1.02
(Ref.) Ave. Short Current	IL(SC)	[A]	6.09	6.09	7.15	8.54	8.54	6.08
Ripple Voltage Calculation	esr-1	[mΩ]	1.11	1.11	1.11	1.11	1.11	1.11
	Capacitance-1	[µF]	9.098	9.098	9.098	9.826	9.826	9.826
	esl-1	[nH]	0.83	0.83	0.83	0.83	0.83	0.83
	esr-2	[mΩ]	3.1	3.1	3.1	1.03	1.03	1.03
	Capacitance-2	[µF]	186.55	186.55	186.55	427.1	427.1	427.1
	esl-2	[nH]	0.36	0.36	0.36	0.18	0.18	0.18
	Total esr	[mΩ]	0.8	0.8	0.8	0.5	0.5	0.5
	Total Capacitance	[µF]	195.6	195.6	195.6	436.9	436.9	436.9
	Total esl	[nH]	0.25	0.25	0.25	0.15	0.15	0.15
	Vr(esr)	[mV]	3.63	3.63	5.48	0.59	0.59	0.92
	Vr(cap)	[mV]	14.36	14.36	7.17	1.59	1.59	0.82
	Vr(ESL)	[mV]	2.01	2.01	9.13	0.81	0.81	3.78
	Vr(Total)	[mV]	20.00	20.00	21.78	2.99	2.99	5.51
	Target Ripple	[mV]	90	90	90	20	20	20

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