TB9083FTG
User manual

1. INTRODUCTION

The TB9083FTG is a gate-driver IC for brushless motors in vehicle application.

It features a built-in safety relay gate-driver in addition to the three-phase gate-driver. It also has a charge pump, a motor current detector circuit, an oscillator circuits and an SPI communication circuit. It has multiple error detection features. Trigger threshold, response action and other settings are modified via the SPI. The TB9083FTG is also equipped with ABIST/LBIST for testing and evaluation of the error detection functions.

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2. Power Boltage

2.1. Operating voltage ranges

Table 2.1 Operating voltage ranges

Parameter	Applied pin	Symbol	Operating voltage range	Unit	Condition
Input voltage	VB	Vb	4.5 to 28	V	DC
	VCC	Vcc	3.0 to 5.5	V	DC
	VCC_OP	Vccop	3.0 to 5.5	V	DC

*This product assumes to be used with a 12 V battery.
*It is not recommended to use this product at Vb<3.6 V all the time.

2.2. Startup sequence

・Apply voltage to VB and VCC, VCC_OP. (There is no starting sequence for VB and VCC. If VB undervoltage detection and VCC_OP undervoltage detection are not released at the start of ABIST, the ABIST result will be abnormal.Slew rates of Vb and Vcc should be within the ranges below.
Vb= less than 8V/μs,Vcc= less than 0.3V/μs)

・After IC startup, oscillator circuits start after a VCC undervoltage has been cancelled and the ABIST diagnosis begins after LBIST is finished.

- If LBIST returns a NG result, the ABIST diagnosis is cancelled and the charge pump and pre-drivers are disabled.

Once ABIST starts, turning on the diagnosis switch toggles the comparator input voltage and inverts the detection comparators.
The diagnosis is synchronized to the clock. Diagnostic data is input to the ABIST evaluation circuit. NDIAG remains at "L" while the diagnosis is in progress.

- When the diagnosis process is completed, the IC switches to normal operation and the charge pump starts operating, and the VCPH voltage rises.
- If no errors are detected during diagnosis, NDIAG changes to "H."
- If errors are detected, NDIAG remains at "L" and the diagnostic data is retained.

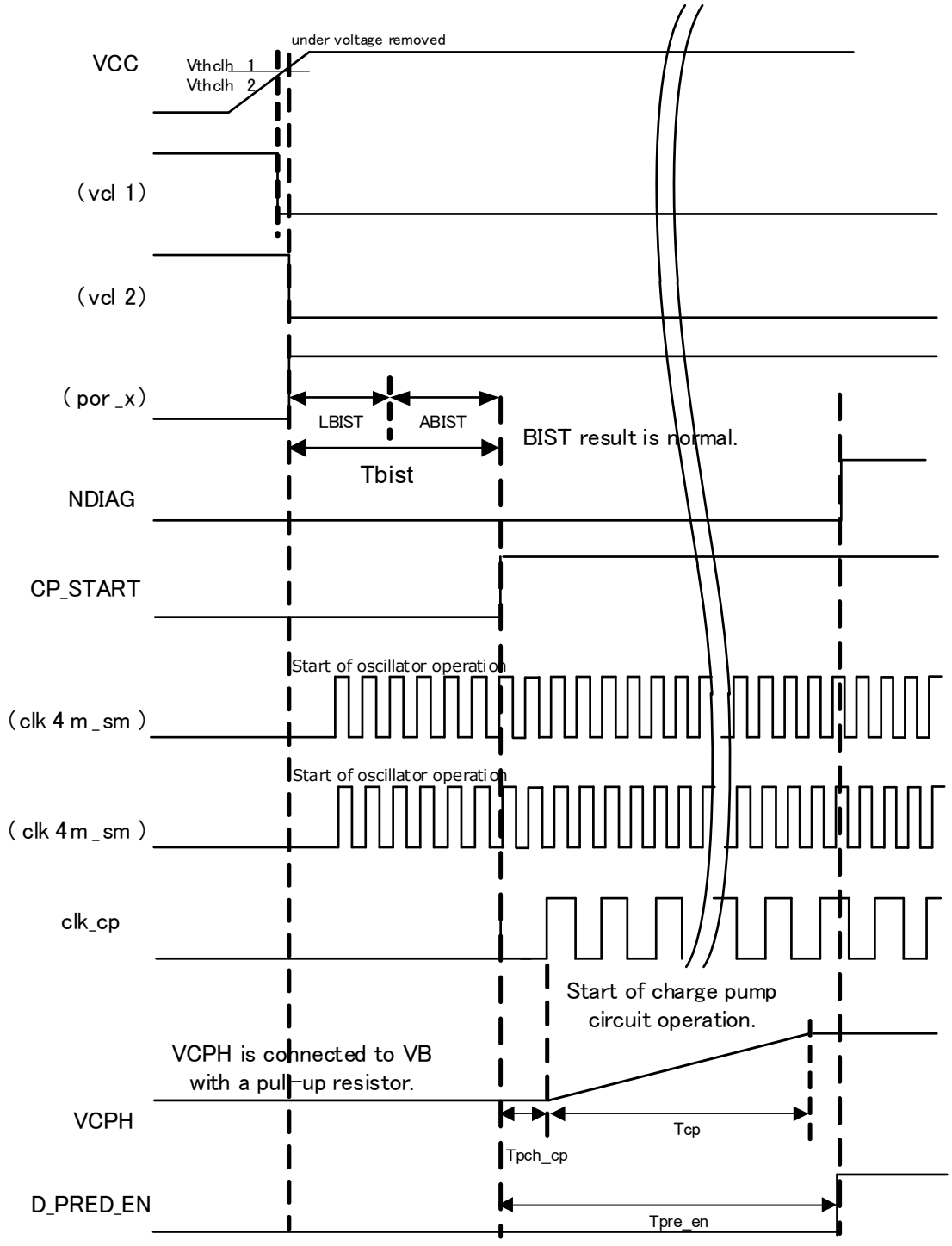


Fig. 2.1 Startup sequence

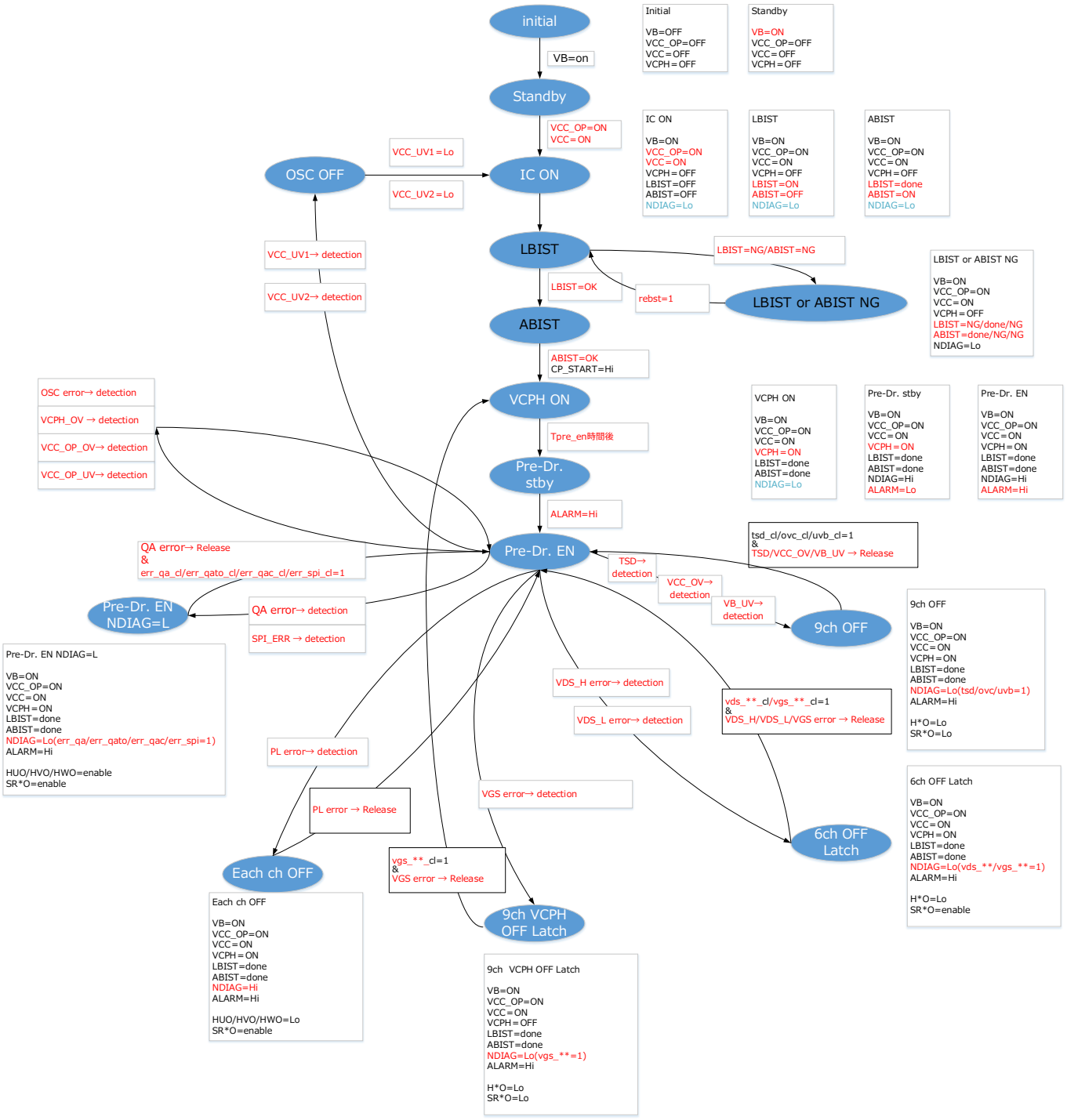


Fig. 2.2 State diagram

3. SPI communication, CRC calculation example

3.1. During write operation

The data format in the write operation is shown in Fig. 3.1.
SI consists of Address[7:0], address specifying bits, Write_Data[15:0], write data specifying bits, and CRC[7:0], bits for checking data. When writing, an address is specified by setting Address[7]=0. Address[0] is not used for address selection. CRC covers Address[7:0] and Write_Data[15:0].

Previous_Data[15: 0] of SO is the data immediately before Write_Data [15: 0] of the register specified by Address [7: 0] to be written. CRC covers Previous_Data[15:0].

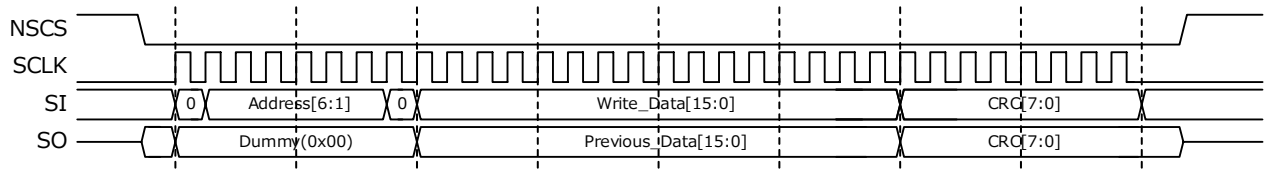
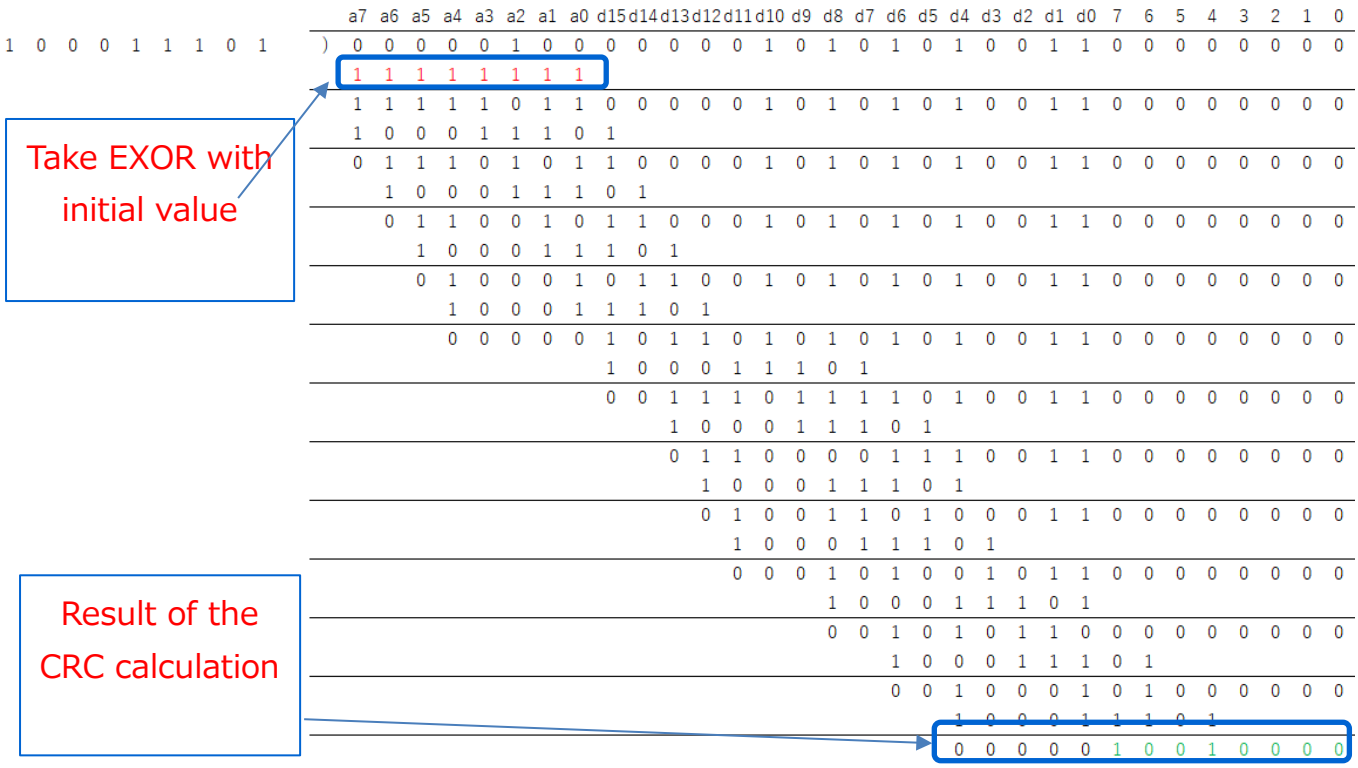


Fig. 3.1 Data format during write operation

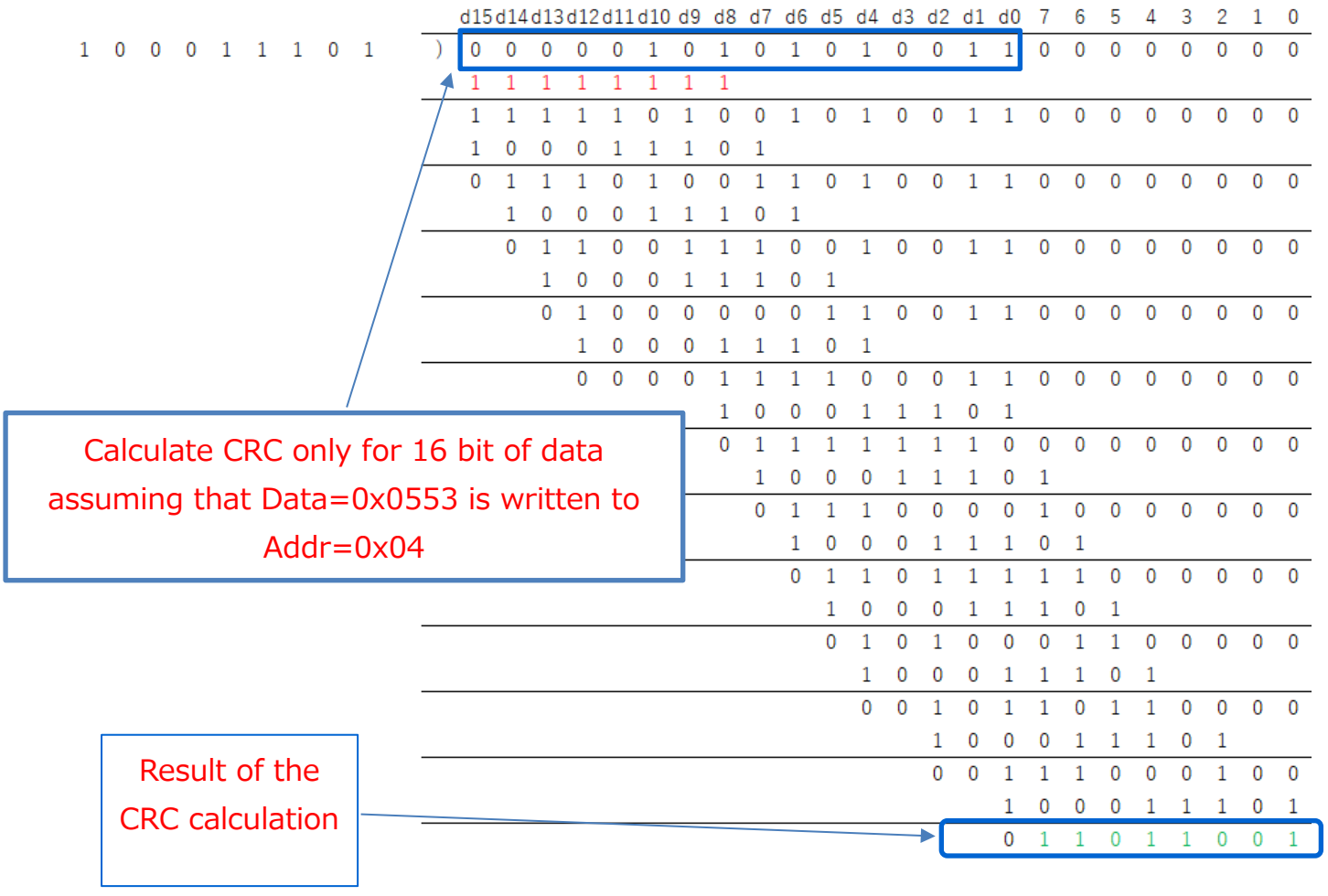
the generating polynomial of CRC is x8+x4+x4+x3+x2+1, So Write_Data is
1*x8+0*x7+0*x6+0*x5+1*x4+1*x3+1*x2+0*x+1
In binary numbers, Write_Data is 100011101

Example calculation: OPSEL2 Write Address=04h / Read Address=84h

When writing to the OPSEL2 register to set
tsd_op[10:8]='101',ferr_op[6:4]='101',uvd_op[2:0]='011',
SI is
[7:0] →0000 0100 (address part)
0000 0101 0101 0011 (data part)
The CRC calculation subject is
0000 0100 0000 0101 0101 0011.
Divide (XOR) it by the generating polynomial
100011101.
First, take a EXOR with initial value as 'FFF'. Then, the CRC is calculated to be 1001 0000.



The CRC for the SO data is '11011001' if the CRC is calculated only for the 16 bits of data, and assuming that Data=0x0553 was written to Addr=0x04.



3.2. During read operation

The data format in the read operation is shown in Fig. 3.3.
SI consist of Address[7:0], address specifying bits, Dummy[7:0], dummy data, and CRC[7:0], bits for checking data. When reading, an address is specified by setting Address[7]=1. Address[0] is not used for address selection. CRC covers Address[7:0].

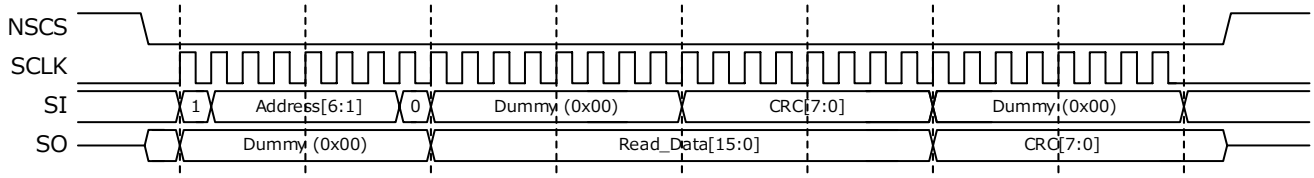
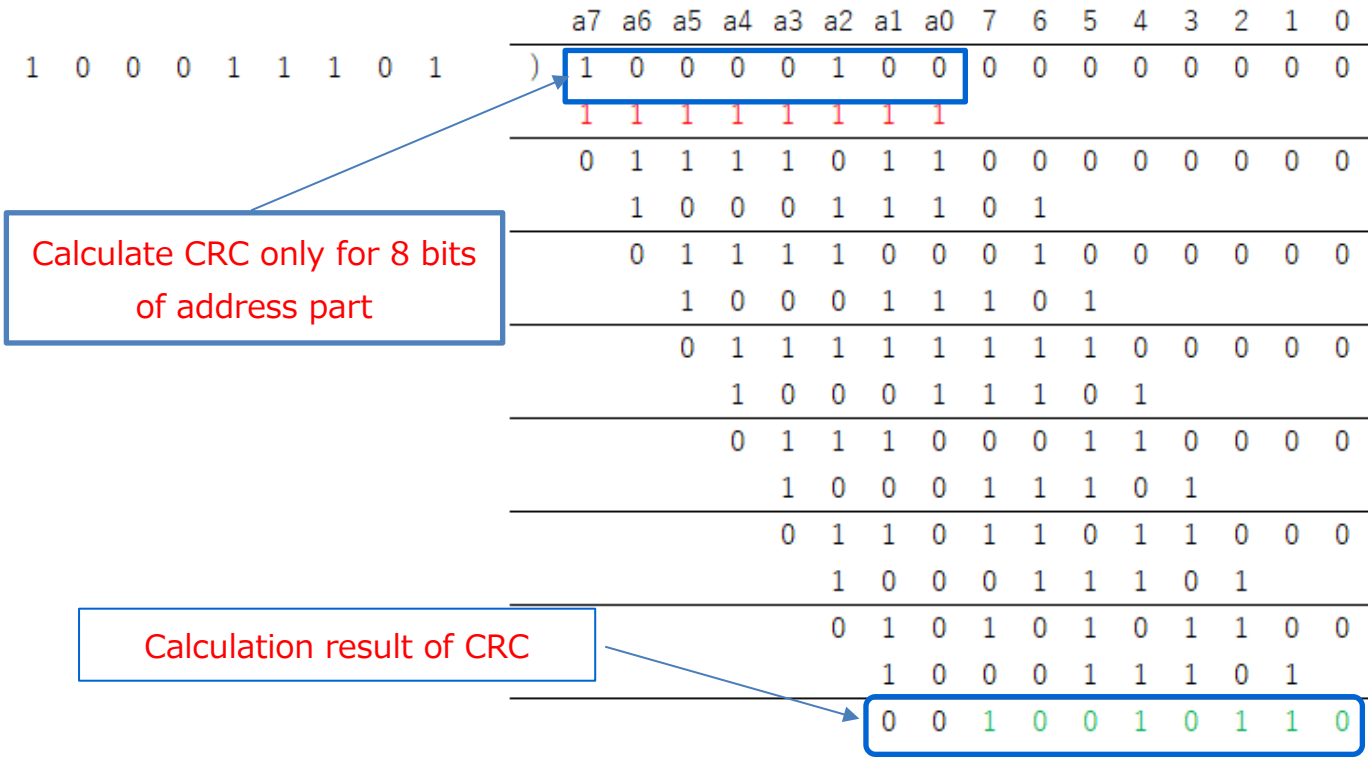


Fig. 3.2 Data format during read operation

The generating polynomial of CRC is x8+x4+x4+x3+x2+1, so Read_Data is
1*x8+0*x7+0*x6+0*x5+1*x4+1*x3+1*x2+0*x+1.
In binary numbers, Read_Data is
100011101

Example calculation: OPSEL2 Write Address=04h / Read Address=84h
When reading, the address part of SI
Adress[7:0] →0000 0100
is subject to CRC calculation.
First, take a EXOR with initial value as 'FFF'. Then, the CRC is calculated to be 1001 0110.



4. Initial diagnosis circuit for external FETs and relays

4.1. Block diagram

Fig. 4.1 shows the block diagram (this is a conceptual diagram and not a practical circuit). An inspection circuit (FET_TEST block) is fitted for executing the initial diagnosis on the external FETs and relays. During the inspection, VDS abnormality detection is disabled and the circuit for detecting VDS abnormality is used for inspecting external FETs and relays (FET_TEST hereafter). Even during FET_TEST, when a "pre-driver off" instruction appears (when gate_en_*="L") for reasons other than VDS abnormality detection, the pre-driver is turned off. During the FET_TEST period, pre-driver control signals for motor control is controlled by the FET_TEST block. Relays always follow CP_RLY_CTRL register setting.

The resistors to maintain HUS, HVS, HWS terminals to the mid-voltage when the pre-drivers are off are connected while an inspection by FET_TEST is being executed.

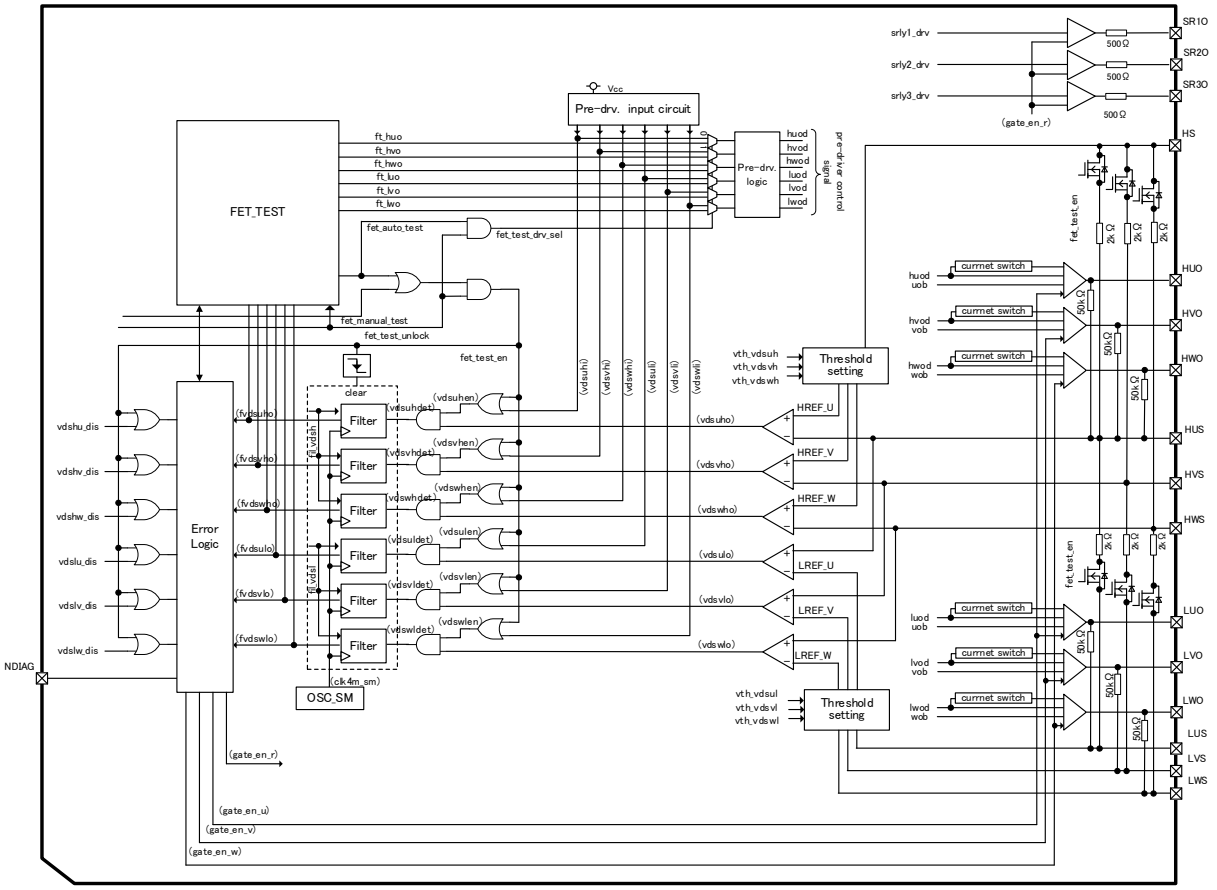


Fig. 4.1 Block diagram of the diagnosis circuit for external FETs and relays

4.2. Classification of inspection modes

Fig. 4.1 shows a list of inspection modes. When fet_test_unlock=0, it provides normal operation.
By setting fet_manual_test = 1 during the period of fet_test_unlock = 1, the external FET can be inspected manually. In this mode, relay drive signals are controlled by the register, FET drive signals are controlled by the input terminal, and the control method is the same as in the normal operation. In normal operation, the VDS detection comparator output is input to the noise filter only for the channels where the FET control input terminal is controlled to "H", but in the manual test mode, the comparator output for VDS detection is input to the noise filter regardless of the state of the input terminal for FET control. In manual test mode, VDS detection is disabled because the VDS detection circuit is used for FET inspection. fet_rmidonU, fet_rmidonV, fet_rmidonW are the control bits to set U phase, V phase and W phase of the mid-voltage generating resistors to ON, respectively. Set each bit to ON depending on the inspection method that the user assumes. When multiple bits are turned ON simultaneously, resistors of the corresponding phases are turned ON simultaneously. The inspection is through expectation comparison by the microcomputer that reads the comparator output (after being filtered) for VDS detection from the VDS_COMP_STAT register.
By setting the fet_test_start bit while fet_test_unlock=1, an inspection sequence is started, and when fet_auto_test="H," timing control of FET drive and saving of the output results of VDS detection comparators are performed by this IC automatically. The FET drive patterns are previously assumed pre-defined drive patterns for Type A, B and C, but for Type D, arbitrary patterns can be set by the register. Since the circuit for VDS abnormality detection is used for FET inspection, VDS abnormality detection is disabled. The resistors for generating the mid-voltage are ON for all phases while the automatic sequence is running. Since FETs are driven by previously assumed pre-defined drive patterns for Type A, B and C, the comparator output is automatically compared with expected values within the IC, but since the drive patterns can be arbitrarily set by the user for Type D, expectation comparison is conducted by the microcomputer.
When fet_manual_test and fet_auto_test become valid simultaneously, fet_auto_test is given priority. When fet_manual_test_[U,V,W] sets multiple bits simultaneously, mid-voltage generating resistors of the phases that are set to 1 are turned ON simultaneously. "*" In Table 4.1 a means Don't 'care.

Table 4.1 List of inspection modes

<table>
<tr><th colspan="7">Register setting or status flag</th><th colspan="5">Operation of each circuit element</th><th rowspan="2">Expected value comparison</th><th rowspan="2">Overview</th></tr>
<tr><th>fet_test_unlock</th><th>fet_auto_test</th><th>fet_manual_test</th><th>fet_rmidonU</th><th>fet_rmidonV</th><th>fet_rmidonW</th><th>fet_test_type</th><th>Relay drive signal</th><th>FET drive signal</th><th>VDS detection</th><th>VDS detection comparator (with Filter)</th><th>Mid-voltage generating resister</th></tr>
<tr><td>0</td><td>*</td><td>*</td><td>*</td><td>*</td><td>*</td><td rowspan="5">*</td><td rowspan="6">Controlled by resister setting by microcomputer.</td><td rowspan="5">Controlled by input terminal.</td><td rowspan="2">Valid</td><td rowspan="2">VDS detection</td><td rowspan="2">OFF</td><td rowspan="2">-</td><td>Normal operation</td></tr>
<tr><td rowspan="5">1</td><td rowspan="4">0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>FET test unlock state.</td></tr>
<tr><td rowspan="3">1</td><td>1</td><td>0</td><td>0</td><td rowspan="4">Invalid</td><td rowspan="4">External FET diagnosis</td><td>U phase ON</td><td rowspan="3">Judgement by microcomputer</td><td rowspan="4">Manual FET test.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>V phase ON</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>W phase ON</td></tr>
<tr><td>1</td><td colspan="4">*</td><td>A</td><td>Automatic control</td><td>All phase ON</td><td>Expected value</td><td>Automatic FET test Type A</td></tr>
</table>

Register setting or status flag							Operation of each circuit element					Expected value comparison	Overview
fet_test_unlock	fet_auto_test	fet_manual_test	fet_rmidonU	fet_rmidonV	fet_rmidonW	fet_test_type	Relay drive signal	FET drive signal	VDS detection	VDS detection comparator (with Filter)	Mid-voltage generating resister		
						B		by IC.				comparison by IC.	Automatic FET test Type B
						C							Automatic FET test Type C
						D		Controlled by resister setting by microcomputer				Judgment by microcomputer.	Automatic FET test Type D

4.3. Inspection method Type A

This type is intended to be performed while motor relays are off. Before starting inspection, set motor relays OFF by the CP_RLY_CTRL register. When a Type A inspection sequence is started, this IC turns on the mid-voltage generating resistors and waits for a certain period of time. After that, this IC turns all pre-drivers for motor control OFF and performs expectation comparison. Then, this IC compares comparator output (after being noise filtered) with expected values while tuning ON the pre-drivers for motor control one by one. While an inspection sequence is being executed, resistors for maintaining HUS, HVS, and HWS at the mid-voltage when pre-drivers are off are tuned ON. During an inspection sequence, VDS comparator (after being filtered) output is stored in registers according to the predefined timing.

Table 4.2 Expected values in the inspection method Type A

VDS_COMP_STAT			D10	D8	D6	D4	D2	D0
			compout_uh	compout_ul	compout_vh	compout_vl	compout_wh	compout_wl
			U phase Hi side	U phase Lo side	V phase Hi side	V phase Lo side	W phase Hi side	W phase Lo side
ft_seq_num	0	UVW All phases off	1	1	1	1	1	1
	1	U phase Hi side ON	0	1	1	1	1	1
	2	V phase Hi side ON	1	1	0	1	1	1
	3	W phase Hi side ON	1	1	1	1	0	1
	4	U phase Lo side ON	1	0	1	1	1	1
	5	V phase Lo side ON	1	1	1	0	1	1
	6	W phase Lo side ON	1	1	1	1	1	0

4.4. Inspection method Type B

This type is intended to be performed while motor relays are ON. Before starting inspection, set motor relays ON by the CP_RLY_CTRL register. When a Type B inspection sequence is started, this IC turns on the mid-voltage generating resistors and waits for a certain period of time. After that, this IC turns all pre-drivers for motor control OFF and performs expectation comparison. Then, this IC compares comparator output (after being noise filtered) with expected values while tuning ON the pre-drivers for motor control one by one. While an inspection sequence is being executed, resistors for maintaining HUS, HVS, and HWS at the mid-voltage when pre-drivers are off are tuned ON. During an inspection sequence, VDS comparator (after being filtered) output is stored in registers according to the predefined timing. Have the microcomputer check the inspection result after confirming that the sequence is completed by fet_auto_test="L."

Table 4.3 Expected values in the inspection method Type B

VDS_COMP_STAT			D10	D8	D6	D4	D2	D0
			compout_uh	compout_ul	compout_vh	compout_vl	compout_wh	compout_wl
			U phase Hi side	U phase Lo side	V phase Hi side	V phase Lo side	W phase Hi side	W phase Lo side
ft_seq_num	0	UVW All phases off	1	1	1	1	1	1
	1	U phase Hi side ON	0	1	0	1	0	1
	2	V phase Hi side ON	0	1	0	1	0	1
	3	W phase Hi side ON	0	1	0	1	0	1
	4	U phase Lo side ON	1	0	1	0	1	0
	5	V phase Lo side ON	1	0	1	0	1	0
	6	W phase Lo side ON	1	0	1	0	1	0

4.5. Inspection method Type C

This type is intended to be used when inspecting whether pre-drivers for motor control can be stopped when abnormality is detected. When motor relays or power supply relays are used, perform the inspection after stopping the pre-drivers by setting ALARM terminal = "L" on the microcomputer or other means after setting the relay operation by CP_RLY_CTRL register so that FETs for motor control operate normally. At this time, set alr_op="H" in ALM_CTRL so that only the pre-drivers for motor control should stop and relays should not stop when ALARM is detected.

By selecting fet_test_type=C and setting fet_test_start while fet_test_unlock="H," a Type C inspection sequence is started. When a Type C inspection sequence is started, this IC turns on the mid-voltage generating resistors and waits for a certain period of time. After that, this IC turns all pre-drivers for motor control off and performs expectation comparison. Then, this IC compares comparator output (after noise filtered) signals with the expected values for two cases: when three channels of the motor control pre-drivers in the high side are turned ON simultaneously and when three channels in the low side are turned ON simultaneously. While an inspection sequence is being executed, resistors for maintaining HUS, HVS, and HWS at the mid-voltage when pre-drivers are off are tuned ON. During an inspection sequence, VDS comparator (after being filtered) output is stored in registers according to the predefined timing.

Table 4.4 Expected values in the inspection method Type C

VDS_COMP_STAT			D10	D8	D6	D4	D2	D0
			compout_uh	compout_ul	compout_vh	compout_vl	compout_wh	compout_wl
			U phase Hi side	U phase Lo side	V phase Hi side	V phase Lo side	W phase Hi side	W phase Lo side
ft_seq_num	0	UVW All phases off	1	1	1	1	1	1
	1	Hi side all ON	1	1	1	1	1	1
	2	Lo side all ON	1	1	1	1	1	1

4.6. Inspection method Type D

This model is intended to be used when inspecting the independence of the motor relays, but allows any combination of FET drives to be set by the FET_TEST_CNT2 register, so can be used for general purposes. A Type D inspection is executed for a single pattern only. The Type D inspection allows any combination of FET drives to be set but uses the values at the timing when the Type D inspection sequence is started, so set the desired values before starting. When a drive pattern in which both high side and low side are ON simultaneously, both the high and low sides are treated as OFF. The IC does not perform expectation comparison but the comparator output (after being noise filtered) signals can be read for six channels. While an inspection sequence is being executed, resistors for maintaining HUS, HVS, and HWS at the mid-voltage when pre-drivers are off are tuned ON.

By selecting fet_test_type=D and setting the fet_test_start during a fet_test_unlock=H period, a Type D inspection sequence is started. When a Type D inspection sequence is started, this IC turns on the mid-voltage generating resistors and waits for a certain period of time. After that, FETs are driven by the drive pattern set in the FET_TEST_CONT2 register. During an inspection sequence, VDS comparator (after being filtered) output is stored in registers according to the predefined timing.

5. Application circuit example

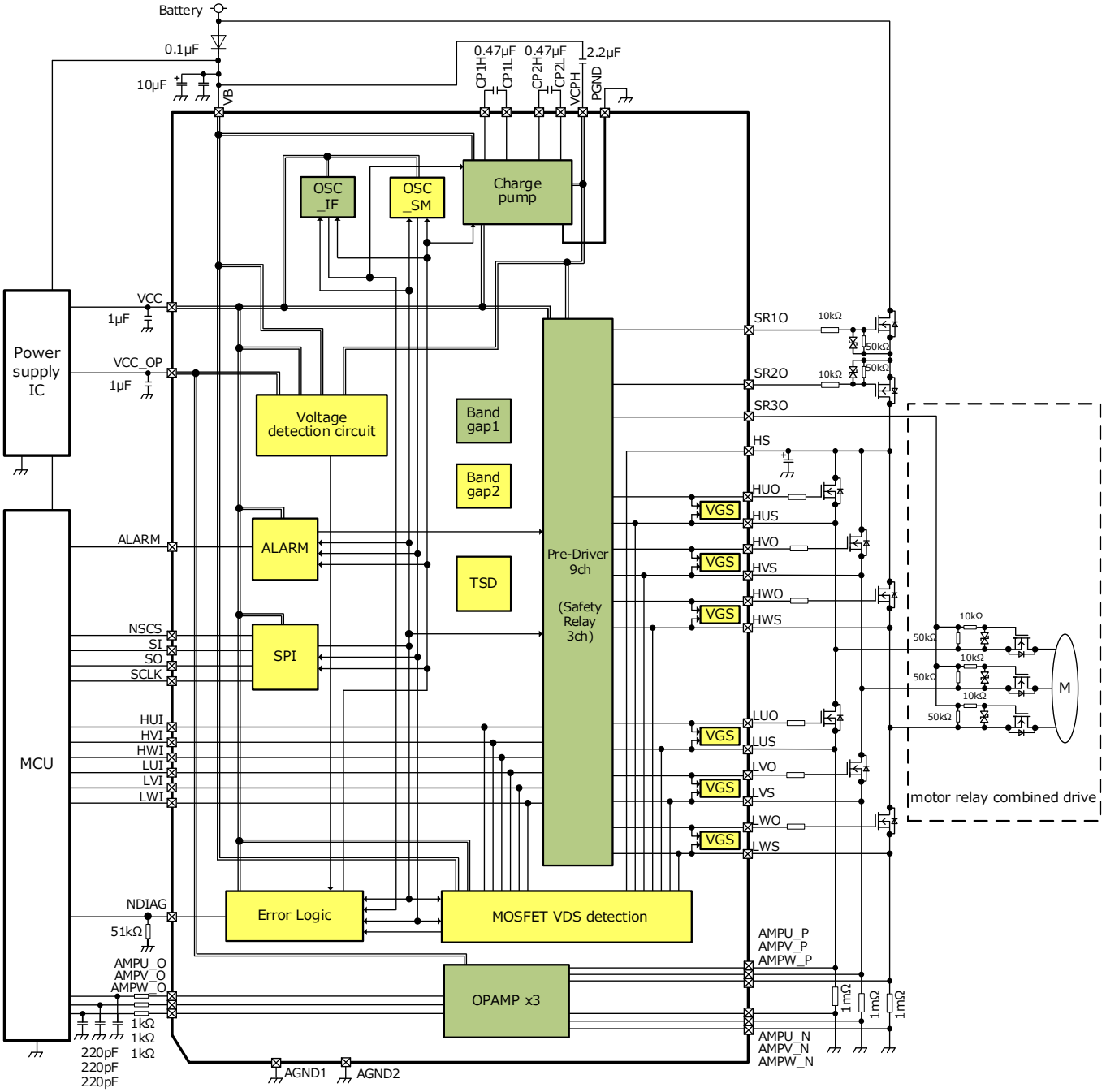


Fig. 5.1 Application circuit example (When driving motor relays collectively)

≪Notes for users≫

* The circuit constants are for the application circuit example, and not guaranteed. Determine the external circuits after a sufficient evaluation and check on a unit board, assuming the conditions of the operating environment.
* The smoothing capacitors externally added to the power supply terminals (VB, VCC, VCC_OP, VCPH) should be located as close to the roots of the IC as possible.
* AGND1, 2 and PGND should be the solid GND (same potential ±0.3V) on the unit board.
* When designing a unit, take into consideration the notes of the individual blocks as well.
* Do not connect the IC incorrectly. It may destroy the IC and/or damage the devices.

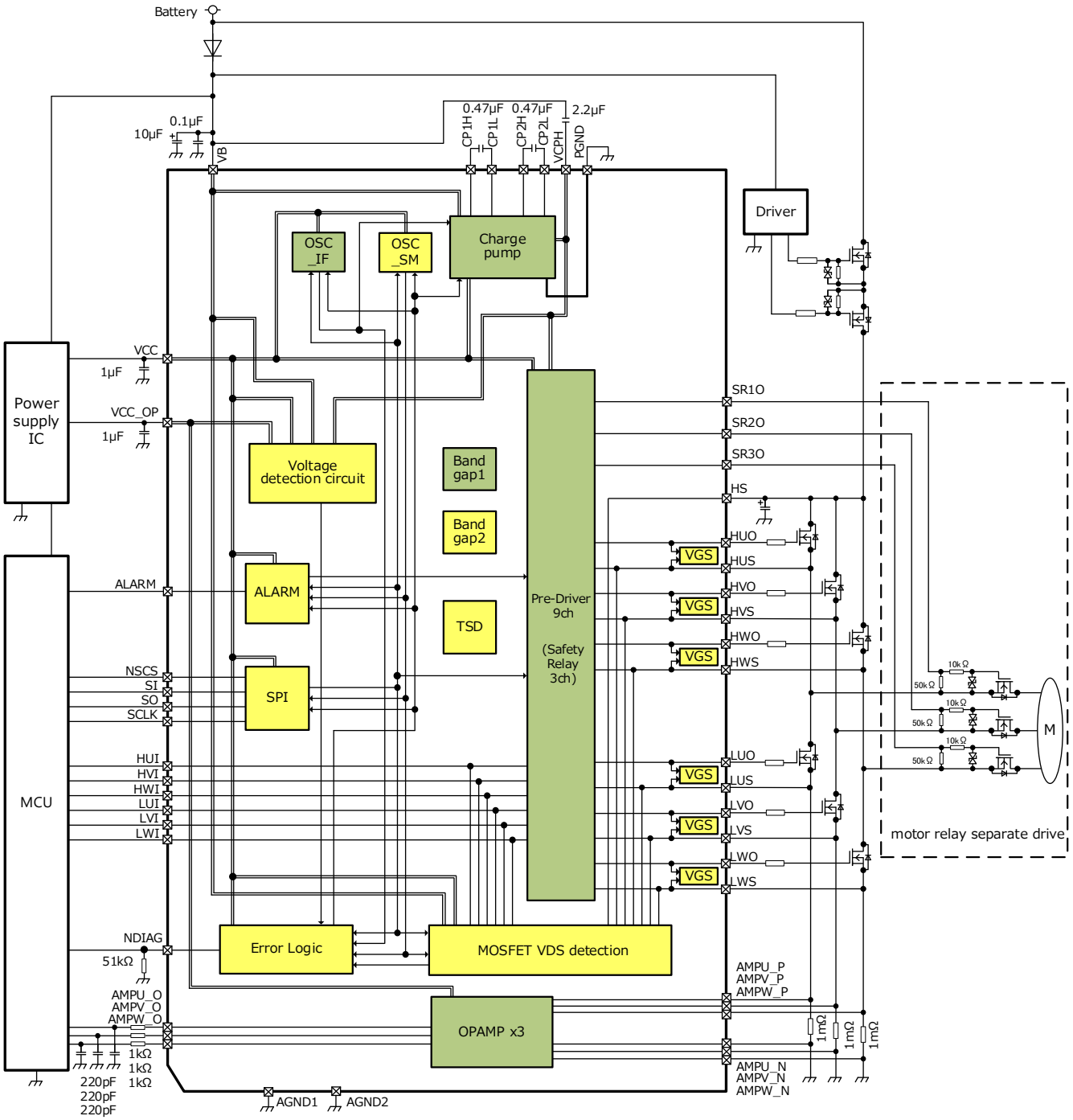


Fig. 5.2 Application circuit example (When driving motor relays individually)

≪Notes for users≫

* The circuit constants are for the application circuit example, and not guaranteed. Determine the external circuits after a sufficient evaluation and check on a unit board, assuming the conditions of the operating environment.
* The smoothing capacitors externally added to the power supply terminals (VB, VCC, VCC_OP, VCPH) should be located as close to the roots of the IC as possible.
* AGND1, 2 and PGND should be the solid GND (same potential ±0.3V) on the unit board.
* When designing a unit, take into consideration the notes of the individual blocks as well.
* Do not connect the IC incorrectly. It may destroy the IC and/or damage the devices.

6. Power consumption

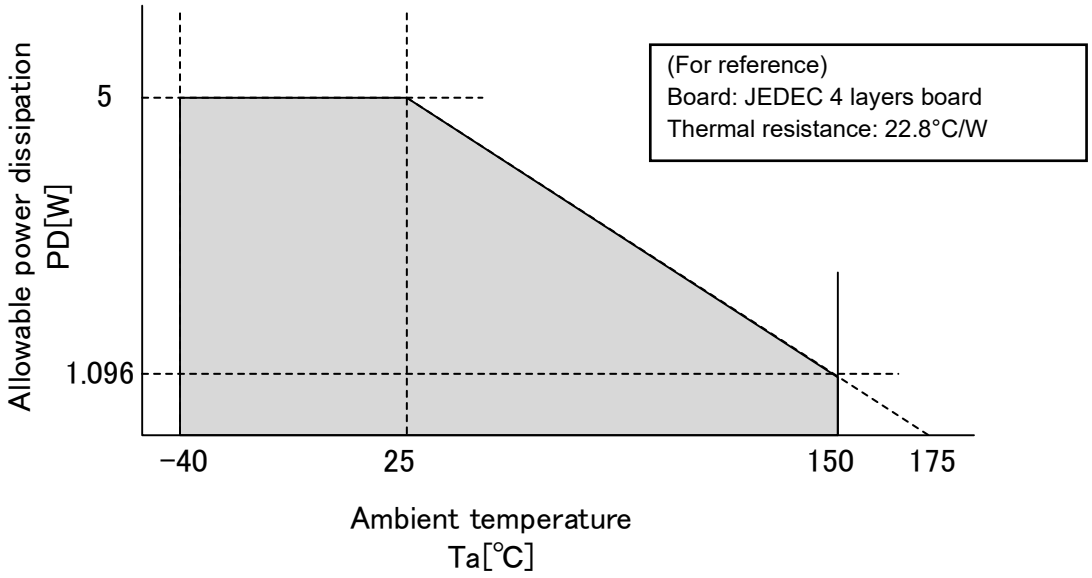


Fig. 6.1 Allowable dissipation curve

6.1. Calculation of power consumption

Refer to the Appendix for calculating the power consumption of each circuit block.

6.1.1. Power consumption of gate driver section (supplementary)

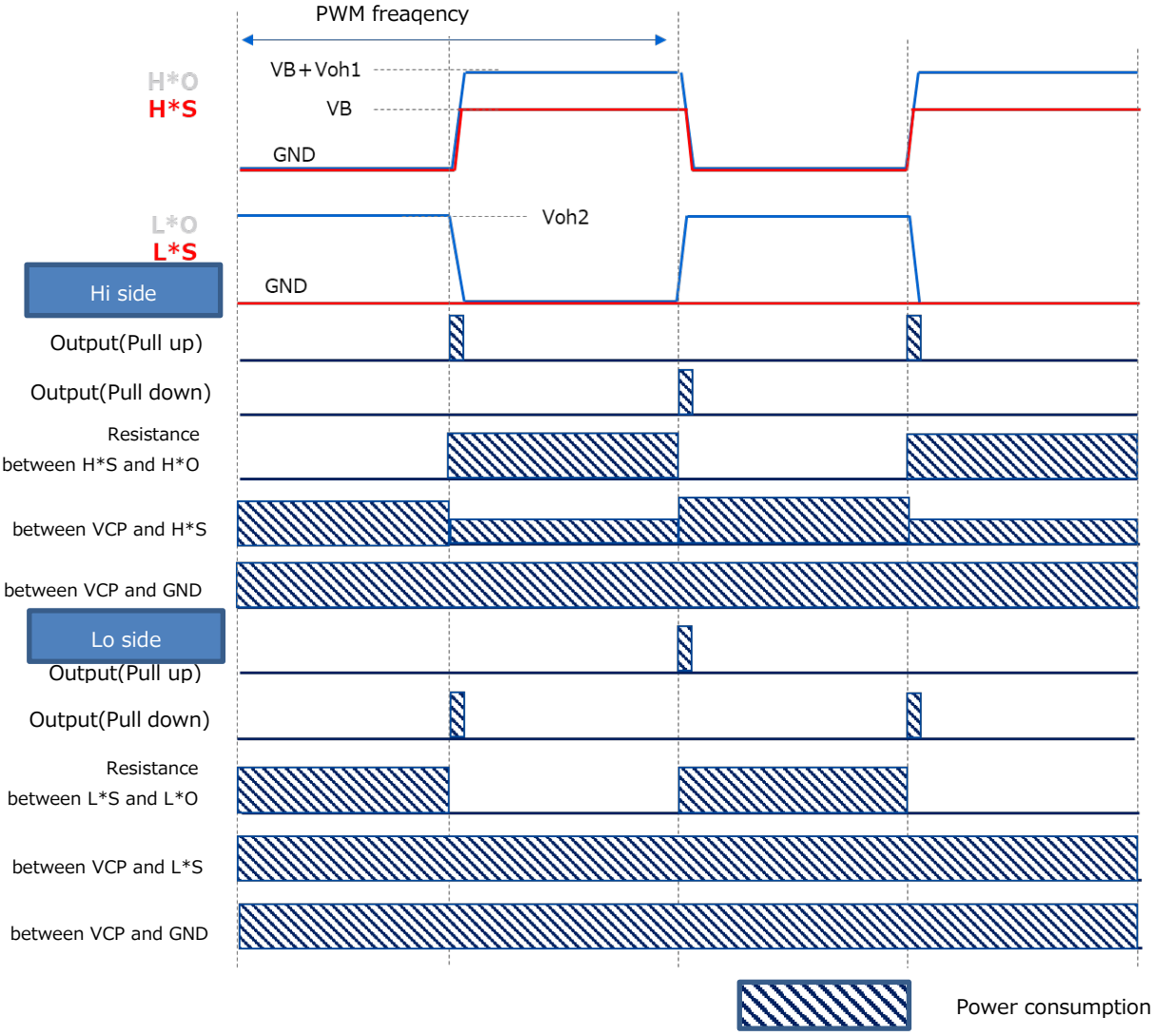


Fig. 6.2 Power consumption chart of gate driver section

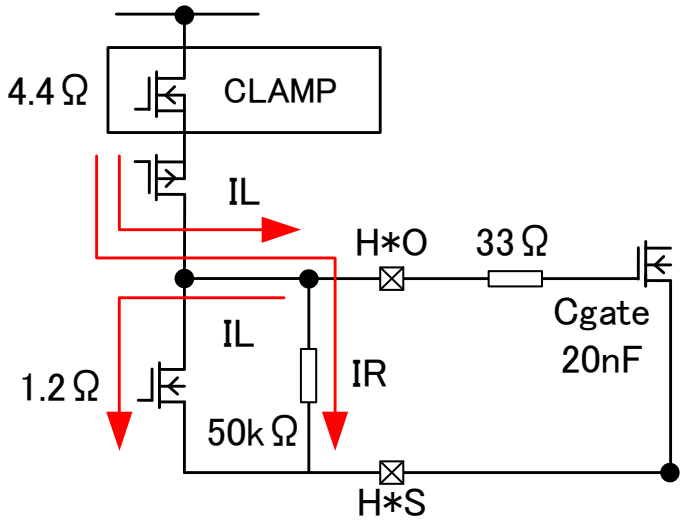


Fig. 6.3 Power consumption diagram of gate driver section

■Gate capacity charge/discharge
IL=Voh1*Cgate*PWM=10V*20nF*20kHz=4mA → Cell C14/E14
26*4m*(4.4+1.2)/(4.4+1.2+33+33)
=26*4m*5.6/71.6=8.13[mW]→The total value of the three channels is the Q40/R40 cell value.

■Pull-down resistor
Assuming Duty=20% of Pulldown resistance between H*O and H*S
IR=10V/50kΩ=0.2[mA]
0.2*10V^2/50kΩ=0.40[mW] →The total value of the three channels is the O40 cell value.

6.1.2. Power consumption of the safety relay (supplementary)

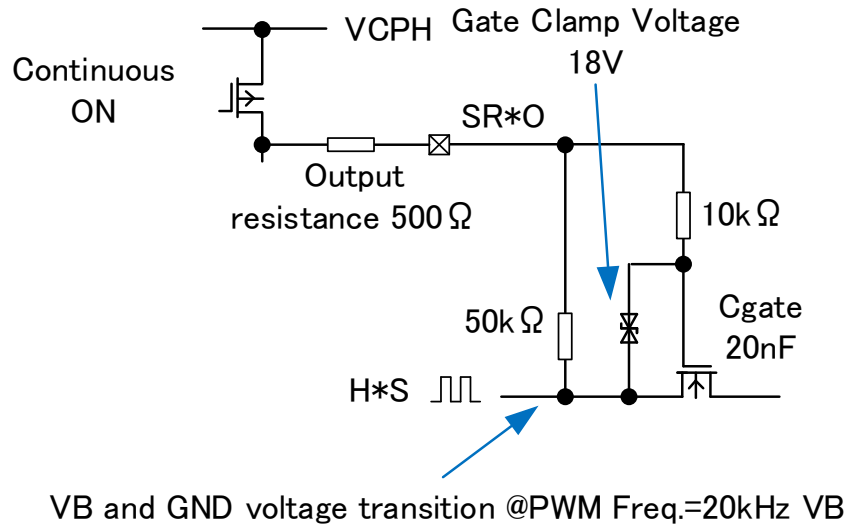


Fig. 6.4 Power consumption diagram of safety relay section No. 1

■When H*S=VB, No Gate clamp and charge Cgate
IL=(VCPH-VB)/(50k+0.5k)
=14/50.5k=0.277[mA]→Cell B21

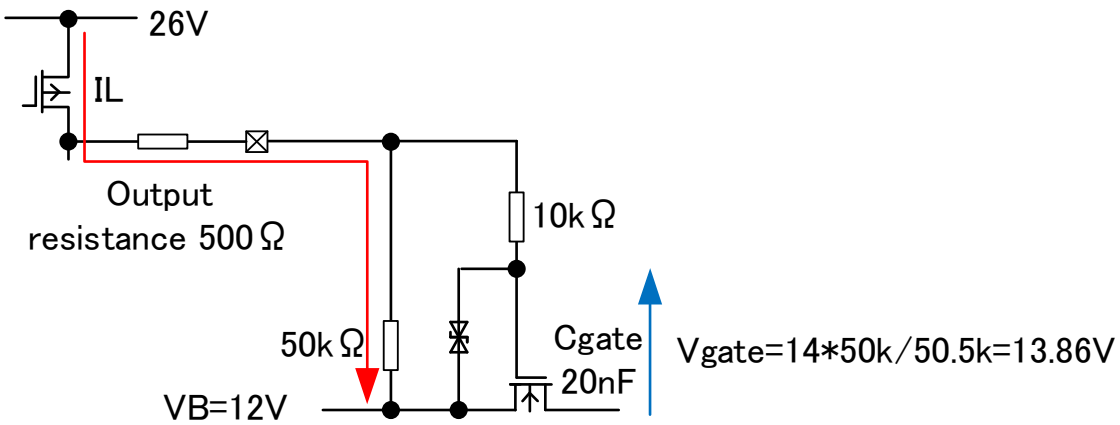


Fig. 6.5 Power consumption diagram of safety relay section No. 2

■When H*S=GND, charge Gate clamp and Cgate
The current at Gate clamping is
IL1*50k=IL2*10k+18
26V=0.5k*(IL1+IL2)+50k*IL1

Solve the simultaneous equations.
IL2=0.738[mA] →Cell D21
IL1=0.508[mA] →Cell C21

The charge current to Gate is

(18-13.86)*20n*20k=1.655mA→Cell E21

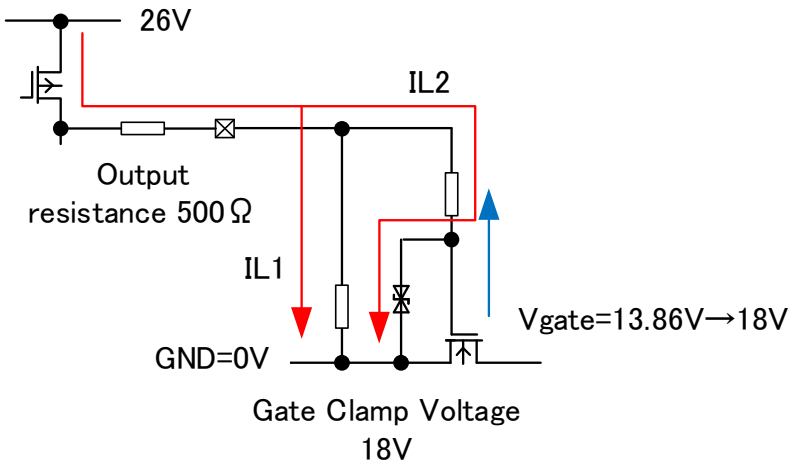


Fig. 6.6 Power consumption diagram of safety relay section No. 3

Assuming that the average current of safety relay is 20% duty,
0.277*0.2+(0.738+0.508+1.656)*0.8=2.376[mA]→Cell G21

6.1.3. Power consumption of charge pump section (supplementary)

Nothing of note, as it is being matched with the actual IC in simulation.

Notes on the contents of the description

1. **Block diagram**
   Functional blocks/circuits/constants in the block diagram may be partially omitted or simplified to explain their functions.

2. **Equivalent circuit**
   Equivalent circuits may be partially omitted or simplified to explain the circuit.

Ver	Editing content	Date
1.0	Create new	2023-03-20
2.0	Figures updated to new JIS symbols	2023-07-07

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