Bi-CMOS Linear Integrated Circuit Silicon Monolithic

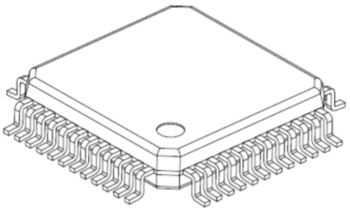
TB9M003FG

IC for automotive three-phase brushless DC motor

1. Description

The TB9M003FG is a gate driver IC with a microcontroller unit (MCU) for automotive brushless DC (BLDC) motor applications, which incorporates Toshiba's unique Vector Engine (VE) to simplify motor vector control and offload the CPU.

The TB9M003FG is designed to be used with external N-channel FET pairs, making it suitable for BLDC motors with a wide range of output. The TB9M003FG also incorporates a CPU and a flash ROM, making it possible to program a control method and parameters according to the motor and application requirements. The TB9M003FG can be configured to transition to Standby mode in the idle state in order to reduce power consumption.



HTQFP48-0707-0.50-001

weight: 0.14 g (typ.)

2. Applications

For automotive (electric pumps and fans), three-phase brushless motor control and drive.

3. Features

- Integrated MCU and gate drivers enable downsizing of the system
- Built-in vector engine for our original sensorless control

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Start of commercial production
2024-01

4. Functions

- 32 bit Arm® Cortex®-M0 core
    - Serial Wire Debug Support
    - 32ch Interrupt Controller1 cycle multiplier
    - Up to 40 MHz clock frequency
- Single Bus Master System
- 12 KBytes ROM(BootLoader, Flash API) (incECC SEC/DED)
- 64 KBytes Code Flash(incl. ECC SEC/DED)
- 4 KBytes SRAM (incl. ECC SEC/DED)
- 32-bit Compare Timers (DTIMER)
- 28-bit Capture Timer (8 inputs, 6 measurement)
- Watchdog Timer(WATCHDOG)
- Power saving modes (CPU Sleep, Standby)
- 4ch Pulse Width Modulator Generator(PWMGEN)
- 12 General-purpose I/O Ports (GPIO)
- 10-bit A/D Converter (GADC) with 2 analog inputs + internal temperature, VMON
- 12-bit A/D Converter (MADC)
- Vector Engine(VE)
- Programmable Motor Driver(PMD)
- Encoder(ENC)
- LDOs (LDO5V, LDO15V)
- Power On Reset (POR5V, PORL)
- 2 on-chip OSCs (IOSCH, IOSCL)
- External X'tal OSC
- PLL
- LIN ISO17987/SAEJ2602 transceiver + controller
- 2 full duplex serial interfaces (UART1, UART2), UART1 with LIN support
- SPI-I/F
- MOSFET driver including charge pump
- High-speed operational amplifier for motor current sensing via shunt
- Over current protection (LDO, MOSFET driver)
- Over temperature protection
- Package HTQFP48-0707-0.50
- Single power supply from 6.0V to 18V
- Temperature Range Tj = -40°C to +175°C
- Green package (RoHS compliant)
- AEC-Q100 grade 0 qualified

5. Block Diagram

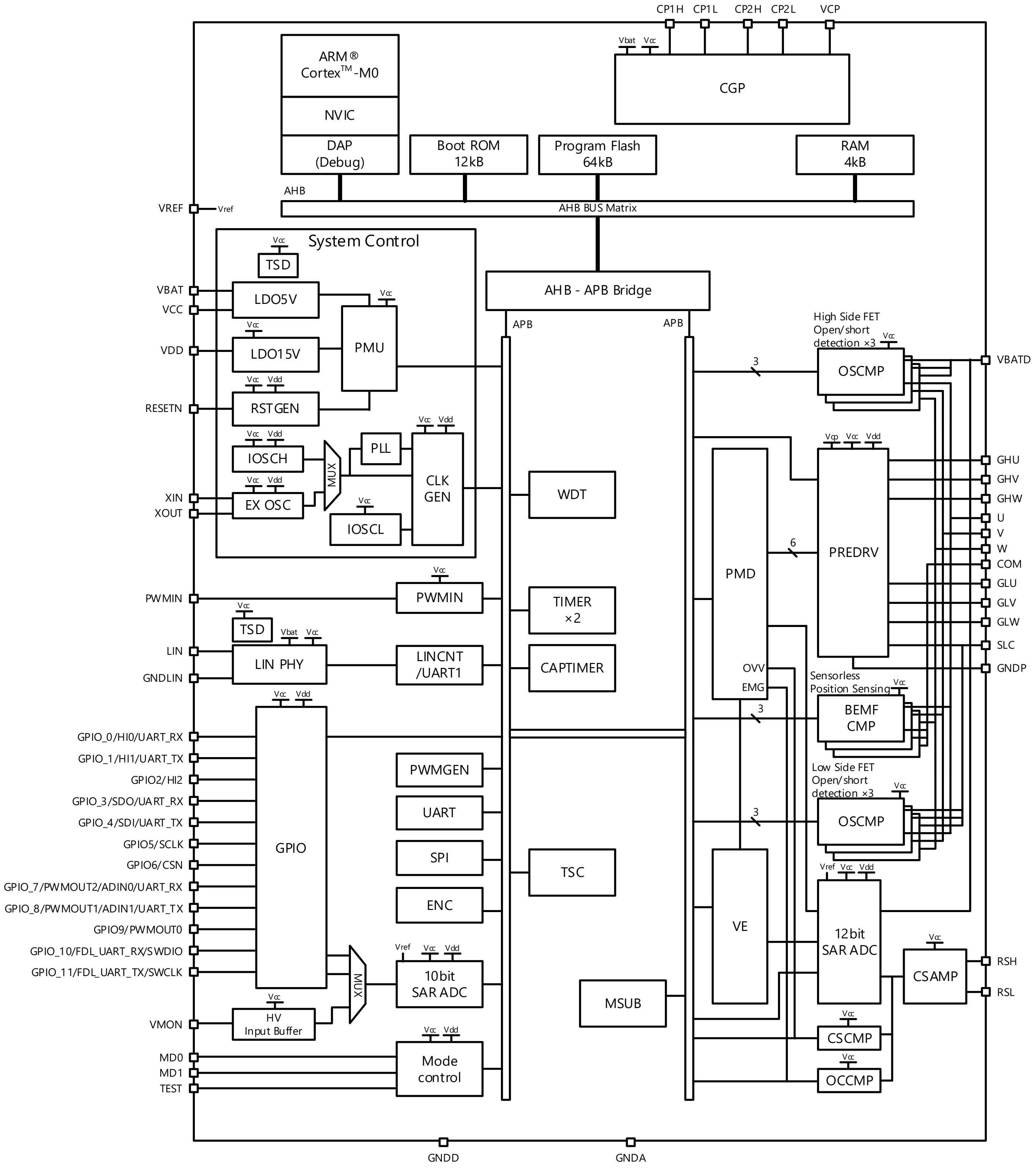


Figure 5.1 Block Diagram

6. Pin Assignments

(Top view)

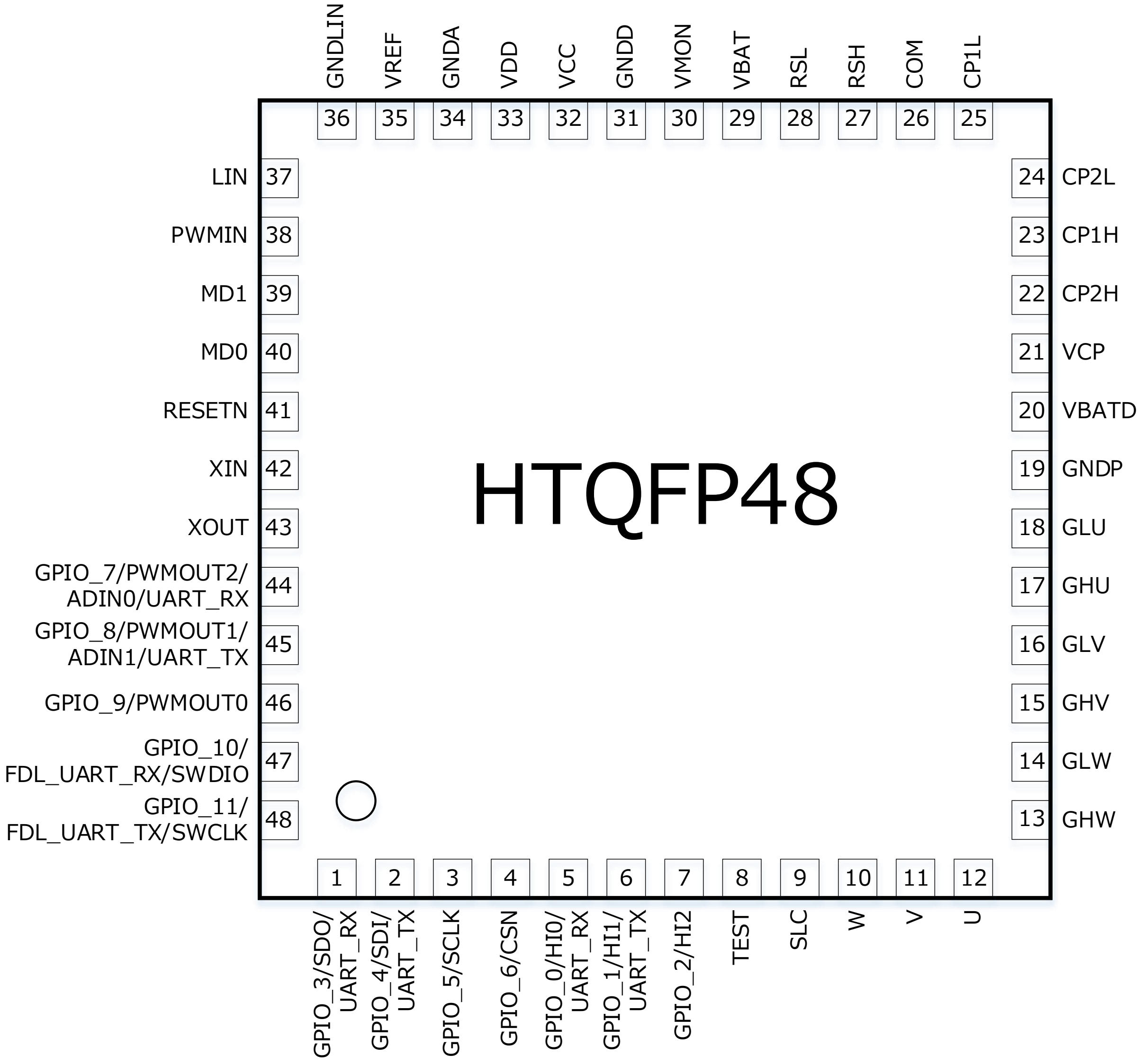


Figure 6.1 Pin Assignment Diagram

7. Pin Description

Table 7.1 Pin Description

Pin	Symbol	I/O	Description
1	GPIO_3/SDO/UART_RX	I/O	General-purpose I/O port / SPI data output/UART_RX
2	GPIO_4/SDI/UART_TX	I/O	General-purpose I/O port / SPI data input/UART_TX
3	GPIO_5/SCLK	I/O	General-purpose I/O port / SPI data clock
4	GPIO_6/CSN	I/O	General-purpose I/O port / SPI chip select
5	GPIO_0/HI0/UART_RX	I/O	General-purpose I/O port/ Hall sensor input/UART_RX
6	GPIO_1/HI1/UART_TX	I/O	General-purpose I/O port/ Hall sensor input/UART_TX
7	GPIO_2/HI2	I/O	General-purpose I/O port/ Hall sensor input
8	TEST	I	Test mode select
9	SLC	I	Low-side FET source input
10	W	I	Phase-W motor connection pin
11	V	I	Phase-V motor connection pin
12	U	I	Phase-U motor connection pin
13	GHW	O	Phase-W high-side FET gate output
14	GLW	O	Phase-W low-side FET gate output
15	GHV	O	Phase-V high-side FET gate output
16	GLV	O	Phase-V low-side FET gate output
17	GHU	O	Phase-U high-side FET gate output
18	GLU	O	Phase-U low-side FET gate output
19	GNDP	-	Power ground
20	VBATD	I	Battery voltage regulator input for driver circuit
21	VCP	O	Voltage regulator output for charge pump
22	CP2H	O	Boost capacitor connection pin for charge pump
23	CP1H	O	Boost capacitor connection pin for charge pump
24	CP2L	O	Boost capacitor connection pin for charge pump
25	CP1L	O	Boost capacitor connection pin for charge pump
26	COM	I	Motor pseudo-neutral point input
27	RSH	I	VCC side of current-sense resistor
28	RSL	I	Ground side of current-sense resistor
29	VBAT	I	Battery voltage regulator input
30	VMON	I	Battery voltage regulator input (for ADC input)
31	GNDD	-	Logic ground
32	VCC	O	5-volt regulator output
33	VDD	O	1.5-volt regulator output
34	GNDA	-	Analog ground
35	VREF	I	ADC reference voltage input
36	GNDLIN	-	Ground for LIN Phy
37	LIN	I/O	LIN bus line
38	PWMIN	I	PWM speed input
39	MD1	I	Mode select

40	MD0	I	Mode select
41	RESETN	I/O	Reset I/O
42	XIN	I	Crystal or ceramic oscillator connection pin
43	XOUT	O	Crystal or ceramic oscillator connection pin
44	GPIO_7/PWMOUT2/ADIN0/UART_RX	I/O	General-purpose I/O port / ADC input/UART_RX
45	GPIO_8/PWMOUT1/ADIN1/UART_TX	I/O	General-purpose I/O port / ADC input/UART_TX
46	GPIO_9/PWMOUT0	I/O	General-purpose I/O port / PWM output
47	GPIO_10/FDL_UART_RX/SWDIO	I/O	General-purpose I/O port / UART RX for FDL_UART/ SWDIO for Debug
48	GPIO_11/FDL_UART_TX/SWCLK	I/O	General-purpose I/O port / UART TX for FDL_UART/ SWCLK for Debug

8. I/O Equivalent Circuits

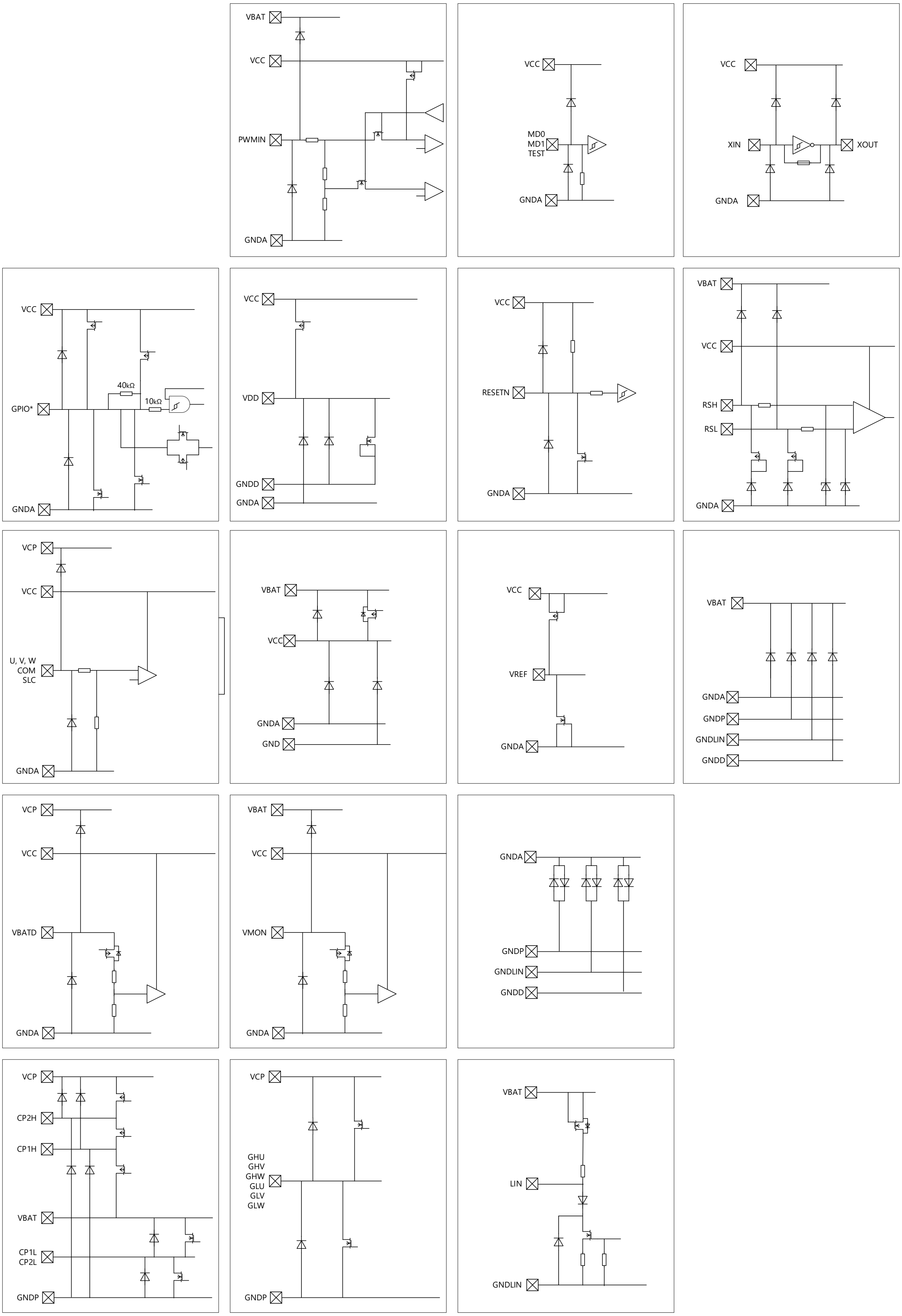


Figure 8.1 I/O Equivalent Circuit Diagrams

9. Functional Description

9.1. Predriver Circuit

- Six-channel predriver circuit for driving a three-phase inverter (consisting of high-side and low-side N-channel MOSFETs) for a BLDC motor
- Turns on and off the predrivers according to the drive signals from digital logic

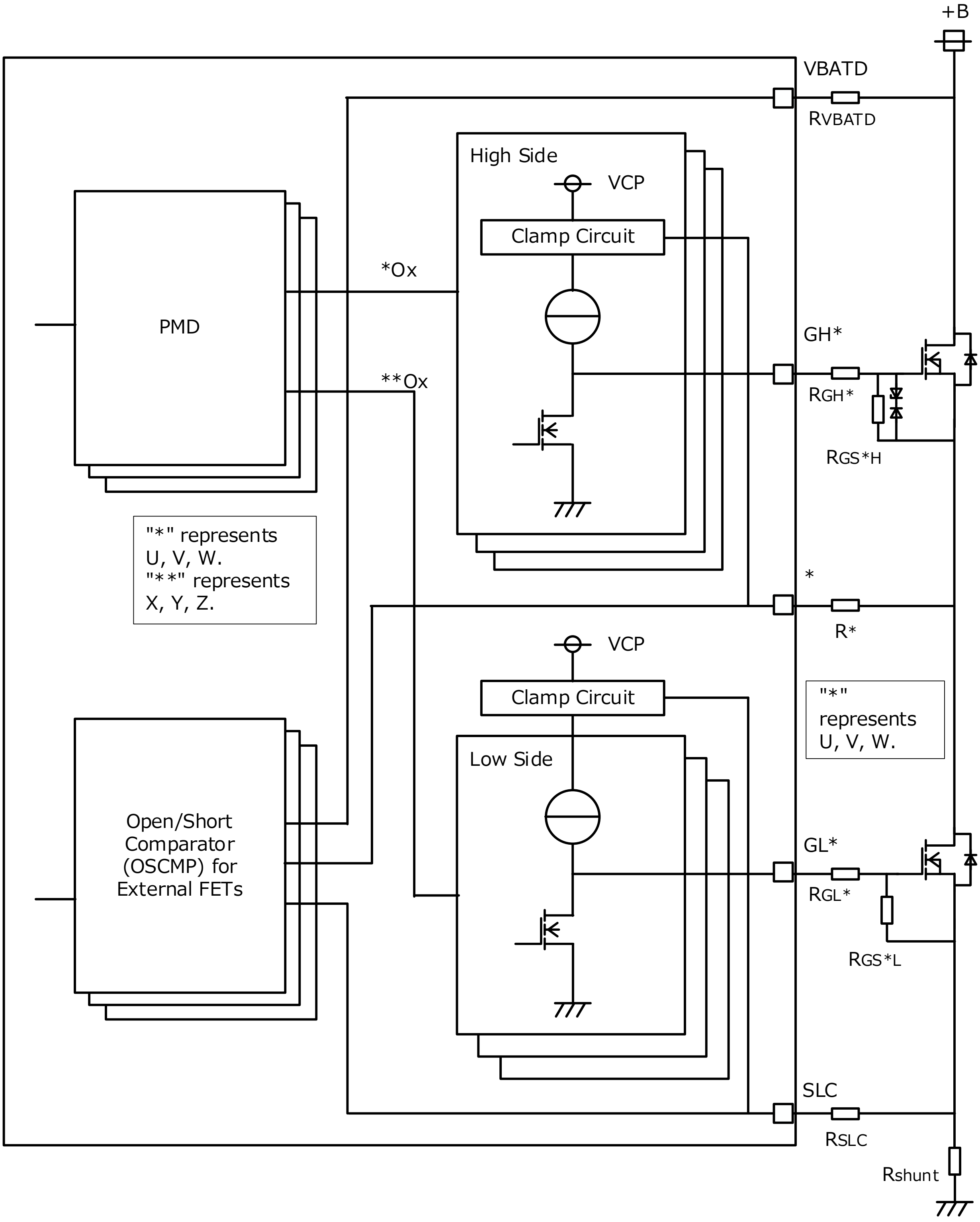


Figure 9.1.1 Predriver Circuit Diagram

9.2. Charge Pump Circuit

The CGP generates a voltage for the PREDRV to drive external high-side N-channel FETs.

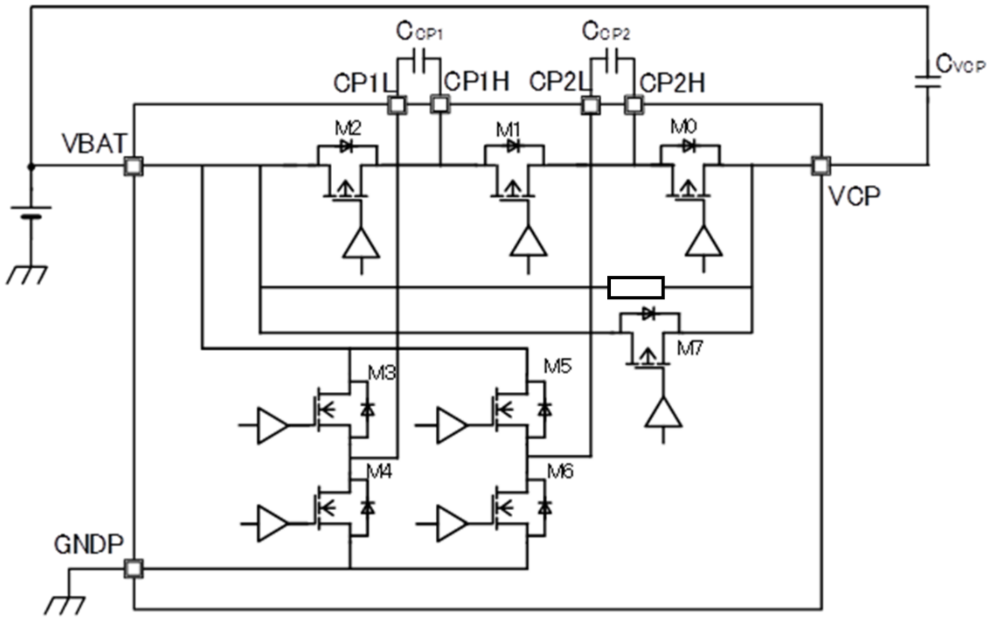


Figure 9.2.1 Charge Pump Circuit Diagram

9.3. Current-Sense Amplifier (CSAMP)

- The Current-Sense Amplifier (CSAMP) amplifies the voltage across an external shunt resistor by the gain programmed via a 3-bit register field.
- The amplified voltage is applied to the MADC, Overcurrent Detection Comparator (OCCMP), and Current Clamp Comparator (CLCMP).
- The output offset voltage can be adjusted prior.

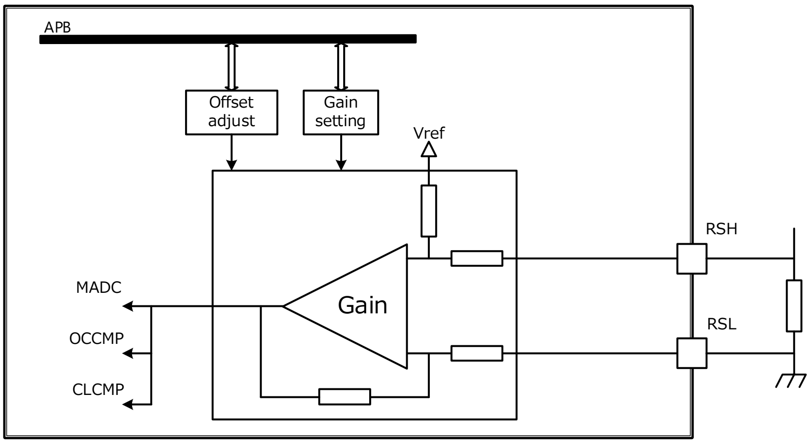


Figure 9.3.1 Current-Sense Amplifier Circuit Diagram

9.4. Current Clamp Comparator (CLCMP)

- The CLCMP limits current if the output from the Current-Sense Amplifier (CSAMP) exceeds the programmed voltage threshold.
- The output voltage of the CSAMP is applied to the CLCMP.
- This threshold is programmable in 32 steps (i.e., with a 5-bit value)
- The CLCMP incorporates a digital filter to prevent malfunction caused by noise.

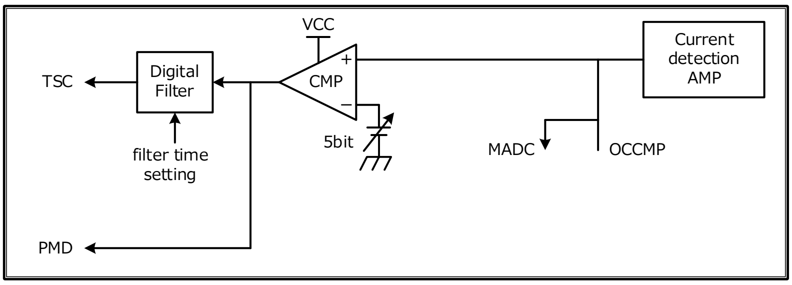


Figure 9.4.1 Current Clamp Comparator Circuit Diagram

9.5. Overcurrent Detection Comparator (OCCMP)

- The OCCMP reports an error when the output from the Current-Sense Amplifier (CSAMP) exceeds the programmed threshold.
- The OCCMP can be enabled and disabled via the ANASTBY register.
- The overcurrent threshold is programmable with a four-bit value via a special function register.
- The OCCMP incorporates a digital filter to prevent malfunction caused by noise.

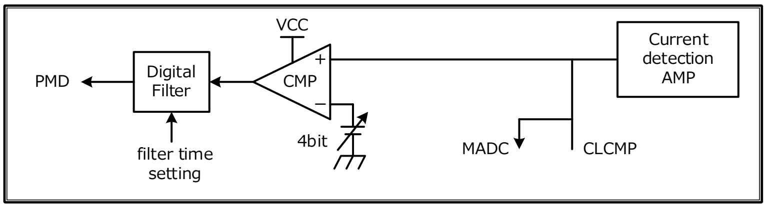


Figure 9.5.1 Overcurrent Detection Comparator Circuit Diagram

9.6. Open/Short Comparator (OSCMP) for External FETs

The Open/Short Comparator detects open- and short-circuits involving external FETs.

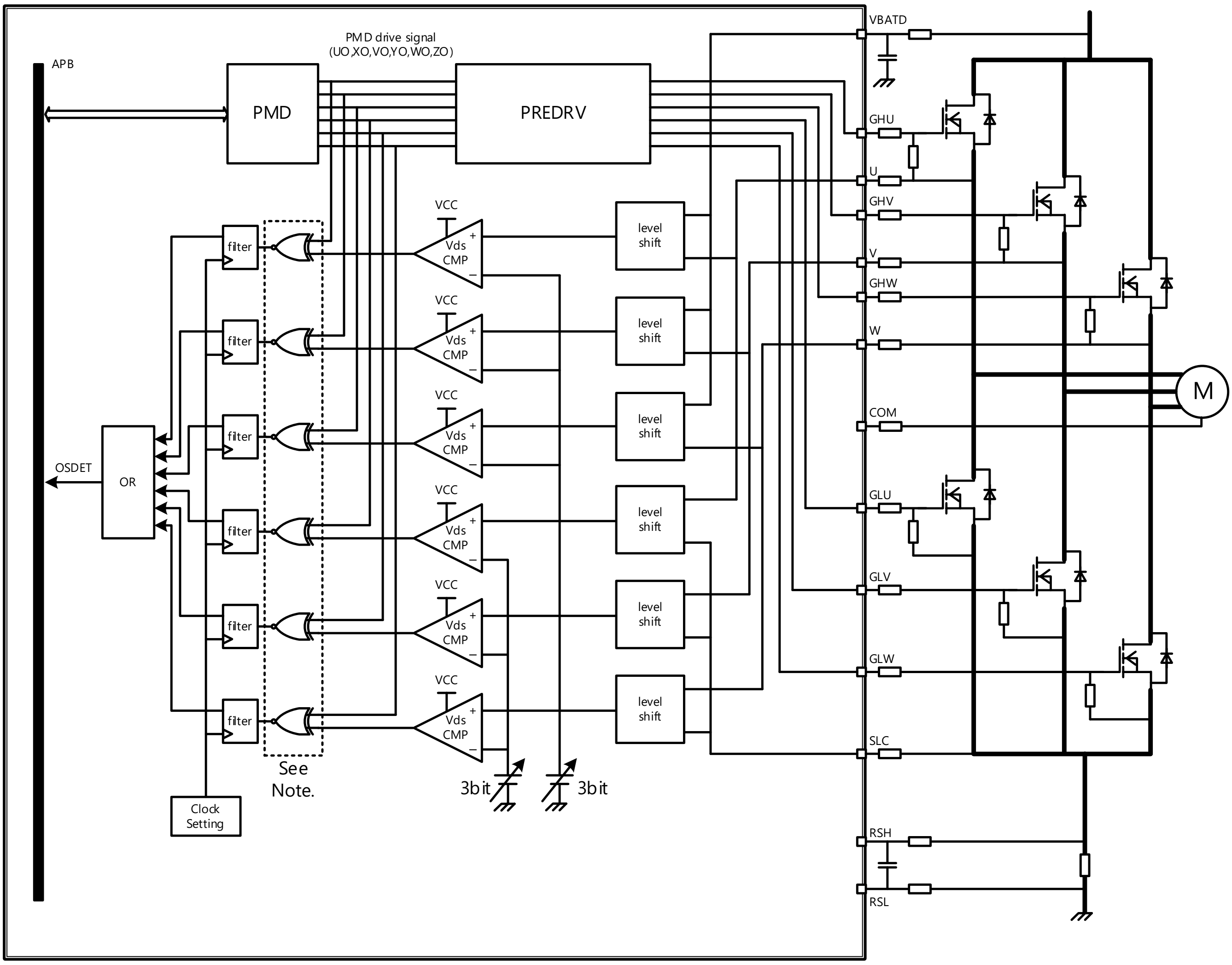


Figure 9.6.1 OSCMP Block Diagram

9.7. Vector Engine(VE)

Table 9.7.1 VE Function List

Category	Function	Description
Calculation	Basic functions	Fixed-point calculation Vector control tasks Tasks for interfacing with the PMD and MADC
	Current control tasks	PI control of d-axis and q-axis currents ・Non-interference control ・Output limiting based on scalar voltage values
	SIN/COS Calculation 1 task	Calculates the sine and cosine values of phase θ ・Allows phase interpolation and clipping
	SIN/COS Calculation 2 task	Calculates the sine and cosine values of phase θ
	SIN/COS Calculation 3 task	Calculates the sine and cosine values of phase θ ・Allows phase interpolation and clipping
	Output Voltage Transformation task	・Coordinate axis transformation (inverse Park transformation) Two types of phase transformation (space vector modulation and inverse Clark transformation)
	Output Control task	Converts three-phase voltage into PWM output settings for the PMD (two types) ・Allows output limiting ・Allows dead-time compensation
	Trigger Generation task	Calculates the PMD’s AD conversion sampling timing from three-phase duty cycles
	Current Correction Preparation task	Corrects detected current values for low inductance motor. Used in combination with Input Process 3 and Input Process 6 tasks.
	Input Process tasks	Reads conversion results from the MADC and converts them into fixed-point values (six types) Supports current polarity determination (hysteresis/reverse hysteresis)
	Input current transformation	・Phase transformation (Clark transformation) ・Coordinate axis transformation
	Individual functions	・Arctangent (ATAN) calculation ・Square-root calculation ・No Operation(NOP)
	Position Estimation task	・Calculates electrical angle speed and phase θ from motor parameters, voltage, and current
	Position Sensor Input Process task	Calculates phase θ and electric angular velocity from the inputs from a position sensor such as an encoder that generates multiple pulses per revolution
Schedule management	Program Schedule control	・Program schedule capable of defining the order in which to execute tasks and their start-up control ・Supports up to 32 tasks
	Start-up control	・Repetition start ・Starts the input schedule upon completion of an AD conversion Starts executing an Input Process task upon ADC-complete interrupt when the VE is in the Standby state following the completion of an output schedule
Interrupt control	Schedule-complete interrupt	Generates an interrupt when a task with the END flag set to "1" is executed repeatedly for the specified number of times ([REPTIME]).

	Error interrupt	Interrupt generated when the VE receives a PWM interrupt from the PMD during the execution of an output schedule, judging it as an error.
Other	Outputs for debugging	Outputs a signal that indicates that the task is running by toggling the debug output when the task starts and stops. For example, depending on the timing of the PMD debug output, the period indicating the operation may appear to be inverted (L output). This can be monitored by the debug output function of the PMD.

9.8. Programmable Motor Driver(PMD)

Table 9.8.1 PMD Function List

Category	Function	Description
PWM output	Resolution	The count resolution for PWM carriers is 1/VECLK. The PWM frequency and duty cycle are programmed with 15-bit values.
	PWM carrier generation	Capable of generating PWM carriers with a frequency between 0.06 kHz and 117.18 kHz (when VECLK=60 MHz) and with a 15-bit amplitude ・ Four types of carrier waveform (triangular, sawtooth, inverted triangular, and inverted sawtooth) ・ Selectable carrier waveforms for each phase ・ Capable of producing phase differences between the base carrier and each of the U, V, and W phases independently.
	Three-phase PWM generation	Three-phase PWM waveforms are generated by comparing the PWM carriers and the programmed duty cycles. The duty cycles of the three phases can be the same or independently programmed.
	Commutation control	Each of the six output ports can be programmed to be driven to the PWM output level, logic High, or logic Low. PWM waveforms can be generated independently for each of the three phases with a common PWM carrier (three-phase complementary PWM).
AD conversion triggering	Synchronous ADC trigger generation	Generates MADC synchronous trigger signals to start AD conversion at any timing synchronous to the PWM carrier
Protection functions	Protection control	Turns off the PWM outputs in response to a protection input signal ・ Provides two types of protection control (EMG and OVV)
	Dead-time control	Inserts a dead-time period to prevent a short-circuit between high-side and low-side switches (U/X, V/Y, W/Z) during their switching when generating three-phase complementary PWM signals
Register buffering	–	Double- and triple-buffered registers allow the PWM period, duty cycles, ADC trigger timing, and the commutation control settings for the six output ports to be changed dynamically. ・ The update timing of execute buffers is selectable from: 1) asynchronous, 2) the center of the PWM period, 3) the end of the PWM period, and 4) the center and end of the PWM period. ・ The update timing of intermediate buffers is selectable from: 1) asynchronous, 2) the center of the PWM period, 3) the end of the PWM period, 4) the 1/4 point of the PWM period, 5) the 3/4 point of the PWM period, 6) center and end point of the PWM period, and 7) the 1/4 and 3/4 point of the PWM period.
Interrupt requests	PWM interrupt (INTPWM)	Capable of generating interrupt requests synchronous to a PWM waveform ・ The interrupt timing is selectable from the center and end of the base carrier. ・ The interval between PWM interrupts is selectable from one-half, one, two, and four PWM periods. ・ Capable of enabling and disabling the decimation of synchronous MADC triggers and buffer updates when interrupts are decimated
	EMG interrupt (INTEMC)	Interrupt request generated in the event of a protection event via an EMGx input
	OVV interrupt (INTOVV)	Interrupt request generated in the event of a protection event via an OVVx input
Debug output	–	Capable of monitoring the operating timing of the motor-related peripherals via an output port ・ Monitor timing of the synchronous MADC trigger output from the PMD ・ Monitor timing of interrupt requests from motor-related peripherals ・ Monitor MADC conversion ・ Monitor timing of VE task transitions ・ Monitor ENC internal signal.

9.9. Memory Map

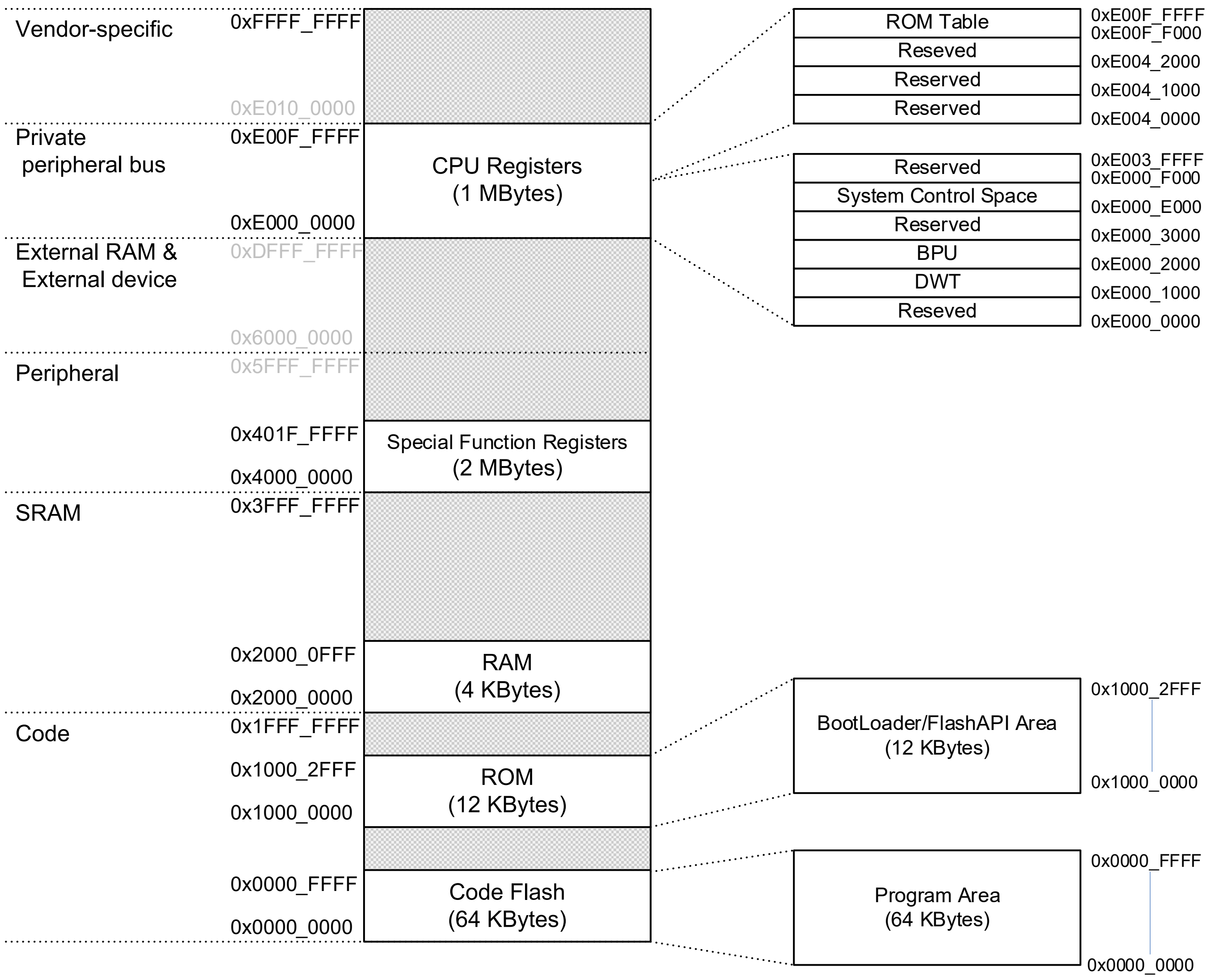


Figure 9.9.1 Memory Map

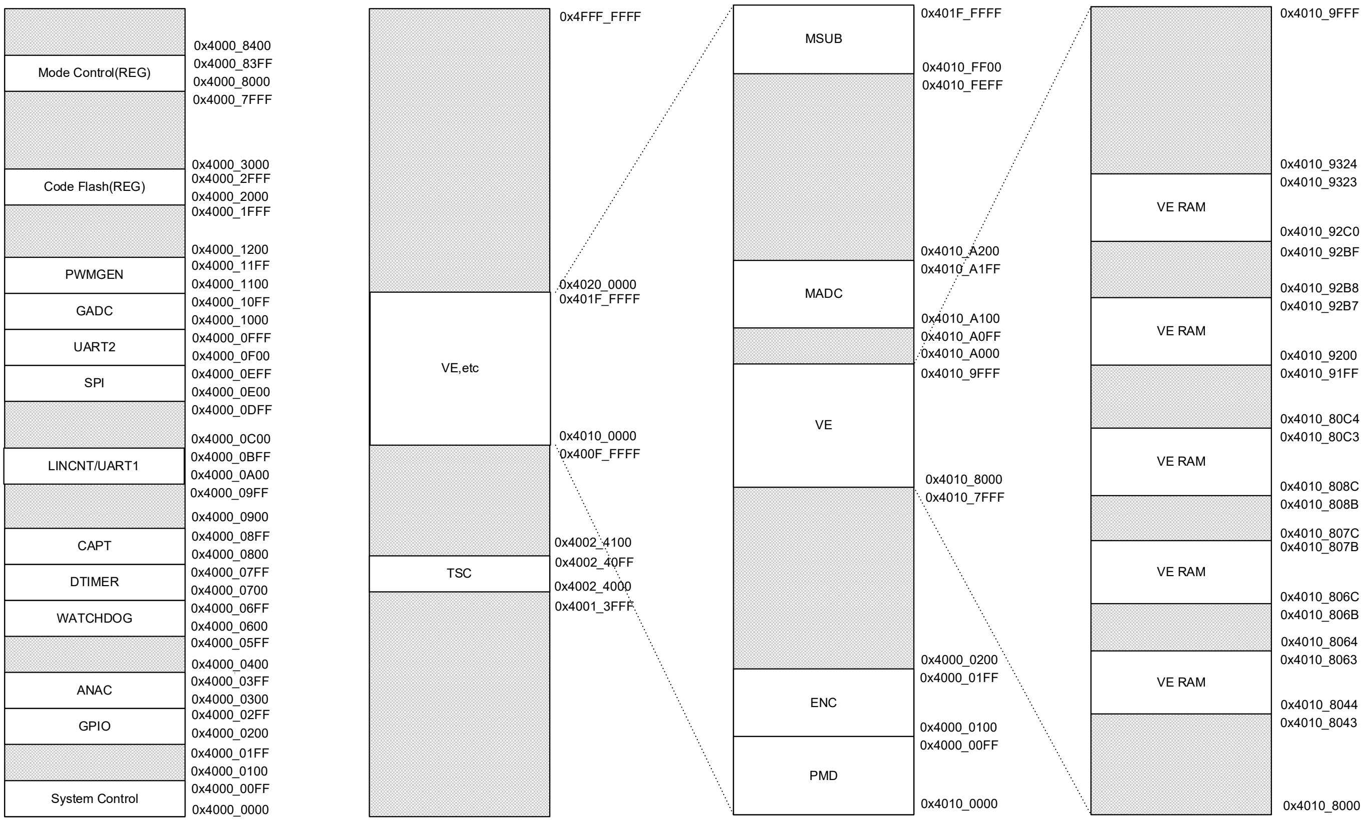


Figure 9.9.2 Memory Map

10. Absolute Maximum Ratings

Table 10.1 Absolute Maximum Ratings

Characteristic	Symbol	Pin(s)	Rating	Unit
Supply voltage	Vbat	VBAT	-0.3 to +40	V
	Vcp	VCP	-0.3 to +40	
	Vcc	VCC, VREF	-0.3 to +6	
	Vdd	VDD	-0.3 to +2.1	
Ground-to-ground voltage differential	Vgnd	GNDA, GNDD, GNDP, GNDLIN	-0.3 to +0.3	
Input voltage	Vin1	LIN	-27 to +40 (Note1)	V
	Vin2	VBATD,	-0.3 to Vcp+0.3 (40 V max)	
	Vin3	PWMIN	-4 to Vbat+0.3 (40 V max) (Note2), (Note5)	
	Vin4	VMON	-0.3 to Vbat+0.3 (40 V max)	
	Vin5	U, V, W, COM, SLC	-2.5 to Vcp+0.3 (40 V max) (Note3), (Note6)	
	Vin6	RSH, RSL	-2 to Vbat+0.3 (40 V max) (Note5)	
	Vin7	TEST, MD0, MD1, RESETN GPIO_x, XIN	-0.3 to Vcc+0.3 (6 V max)	
Output voltage	Vout1	LIN	-27 to +40 (Note1)	V
	Vout2	GHU, GHV, GHW GLU, GLV, GLW	-0.3 to Vcp+0.3 (40 V max) (Note4)	
	Vout3	CP1H, CP2H	-0.3 to Vcp+0.3 (40 V max)	
	Vout4	CP1L, CP2L	-0.3 to Vbat+0.3 (40 V max)	
	Vout5	XOUT, RESETN GPIO_x	-0.3 to Vcc+0.3 (6 V max)	
Operating temperature	Ta	-	-40 to +150	℃
Storage temperature	Tstg	-	-55 to +150	℃

Note:
- None of the absolute maximum ratings must be exceeded even instantaneously. Exposure to stress exceeding absolute maximum ratings might cause permanent destruction or degradation of an IC and adversely affect other components.
  Ensure that none of the absolute maximum ratings is exceeded under any operating conditions.
  Use the IC within the specified operating ranges.
- At outside the ±18-V range, there is a limit to the period during which the TB9M003FG may be exposed to such conditions: ≤ 90 minutes at 18 to 28 V and ≤ 400 ms at 28 to 40 V

Note1: VBAT = 6.0 to 18 V
Note2: Vin3 is the voltage applied by connecting 10kΩ minimum in series.
Note3: Vin5 is the voltage applied by connecting 47Ω minimum in series.
Note4: Vout2 is the voltage applied by connecting 47Ω minimum in series.
Note5: The voltage between VBAT and RSH, RSL should not exceed -0.3V to +40V.
Note6: The voltage between VCP and U, V, W, COM, SLC should not exceed -0.3V to +40V.

11. Operating Ranges

Table 11.1 Operating Ranges

Characteristic	Symbol	Rating	Unit	Remarks
Supply voltage	Vbat	18 to 27	V	Electrical characteristics are not guaranteed. (Note)
		6 to 18		Vbat range in which electrical characteristics are guaranteed.
		4.8 to 6		Electrical characteristics are not guaranteed.(Note)
Operating temperature	Topr	-40 to 150	°C	Ambient temperature, Ta
		-40 to 175		Junction temperature, Tj (Note)

Note: Not tested in a pre-shipment test

12. Electrical Characteristics

12.1. Overall Electrical Characteristics

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Standby current 1	Istby1	VBAT VBATD VMON	Standby mode LFCLK OFF VBAT=VBATD=12 V, Ta=25°C	-	-	20	μA
Standby current 2	Istby2		Standby mode LFCLK OFF VBAT=VBATD=12 V, Ta=70°C Guaranteed by design	-	-	90	μA

Reference information:

The current consumption at the VBAT pin is approximately 33mA under the following conditions:

- VBAT=12V, room temperature, HFCLK used, SYSCLK=40MHz, VECLK=60MHz (reset state), LIN is disabled, CGP is enable, PREDRV is disabled (no external FET gate drive), No other IC external load

Current consumption varies depending on usage conditions such as CPU load and operating frequency.

12.2. Reset Generator and Standby Time

Vbat=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Low-level reset output voltage	Voutlrst	RESETN	Iout=+5 mA	0	-	0.4	V
High-level input threshold voltage	Vihrst		-	VCC ×0.75	-	-	V
Low-level input threshold voltage	Vilrst		-	-	-	VCC ×0.25	V
Input noise filter (analog)	Tfilrst		(See Figure 12.2.1)	10	20	40	μs
Input pull-up resistor	Rpullup		Between the VCC and RESETN pins	30	50	100	kΩ
WATCHDOG reset time	Twdt	-	Time from a WATCHDOG reset request to an internal reset release (except when the flash memory is busy)	-	70	-	μs
Power-on reset settling time	Trst1	-	Time from recovery from a VCC undervolage condition to a CPU reset release	-	-	8	ms
Recovery settling time	Trst2	-	Time from when a wake-up request is detected to when a CPU reset is released after the LDO15V stabilizes	-	-	2	ms
External oscillator settling time	Trst3	-	Time from when the oscillator is started by software to when it settles to a steady state (when a 16-MHz CERALOCK ceramic resonator from Murata is used)	-	-	1	ms
PLL settling time	Tpll	-	-	-	-	140	μs

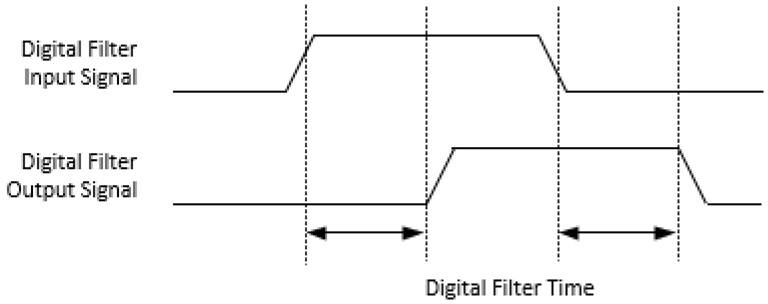


Figure 12.2.1 Measurement of Digital Filter Time

12.3. 5-V Regulator (LDO5V)

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
VCC output voltage 1	Vcc1	VCC	Iload = -10 μA to -135 mA (Total VCC/VDD current consumption of maximum self consumption current inside the IC and external load current (max. 60mA)) Tj = -40 to 150°C	4.9	5.0	5.1	V
VCC output voltage 3	Vcc3		Iload = -10 μA to -135 mA (Total VCC/VDD current consumption of maximum self consumption current inside the IC and external load current (max. 60mA)) Tj = 150 to 175°C	4.8	5.0	5.2	V
Current limit 1	Ilimit1		VCC ≥ 4.0 V	-850	-475	-250	mA
Current limit 2	Ilimit2		VCC ≤ 3.0 V	-250	-112	-10	mA
Dropout voltage	Vdrop		Vbat = 4.8 V,Iload = -120 mA < (-5mA + current consumed by LDO5V)	-	0.2	0.45	V
Undervoltage detection voltage 1	Vrst1		VCC falling (UV_VCC)	4.0	-	4.35	V
Undervoltage release voltage 1	Vrstr1		VCC rising (UV_VCC)	4.2	-	4.75	V
Undervoltage detection voltage 3	Vrst3		VCC falling (POR5V)	3.07	3.45	3.83	V
Undervoltage release voltage 3	Vrstr3		VCC rising (POR5V)	3.22	3.60	3.98	V

Note:
- Connect a capacitor of 1.0 μF or more as close as possible to the VCC pin.
- The current limit at VCC in Standby mode is Current Ilimit2.

12.4. 1.5-Voltage Regulator (LDO15V)

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
VDD output voltage	Vdd	VDD	Iload = -10 μA to -60 mA + (Total VDD current consumption of maximum self consumption current inside the IC and external load current (max. 1mA))	1.45	1.5	1.55	V
Current limit 3	Ilimit3		-	-250	-150	-70	mA
Undervoltage detection voltage 2	Vrst2		VDD falling	1.3	-	1.4	V
Undervoltage release voltage 2	Vrstr2		VDD rising	1.35	-	1.45	V
Overvoltage detection/release voltage	Vddov		-	1.55	-	1.65	V

Note: Connect a capacitor of 2.2 μF or more as close as possible to the VDD pin.

12.5. Charge Pump

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Output voltage 1	Vcp1	VCP	VBAT = 6 V, Iload = -10 μA to -31.8mA, Cload=15,000 pF	VBAT +6.5	-	-	V
Output voltage 2	Vcp2		VBAT = 8 to 18V, Iload = -10 μA to -31.8mA, Cload=15,000 pF	VBAT +10	VBAT +12	VBAT +14	V
Output voltage 3	Vcp3		VBAT=5 V, Iload = -10 μA to -13.8mA, Cload=5,500 pF	VBAT +6.5	VBAT +8.7	-	V
Boost overvoltage detection threshold voltage	Vcplim1		-	31	33	35	V
Boost overvoltage recovery threshold voltage	Vcplim_r1		-	29.5	31.5	33.5	V
Boost disable threshold voltage 1	Vcpstop1	VBAT	-	27	28.5	30	V
Boost enable threshold voltage 1	Vcpstop_r1		-	26	27.5	29	V
Boost disable threshold voltage 2	Vcpstop2	VCP	-	34	36	38	V
Boost enable threshold voltage 2	Vcpstop_r2		-	32	34	36	V
Boost frequency	Fcp	-	-	237.5	250	262.5	kHz
Rise time	Tcp	VCP	Time from when the boost start signal is asserted to when the output voltage reaches 90% of Vcp	-	-	1	ms

Note: Enable the charge pump when VBAT ≥ 5 V.

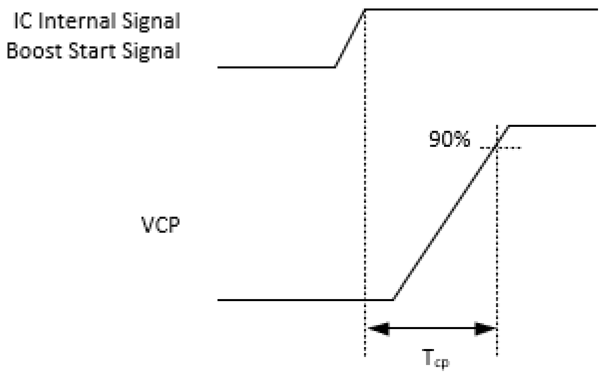


Figure 12.5.1 Measurement of Rise Time

12.6. Oscillator

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Oscillation frequency 1 (HFCLK)	Fosc1	-	-	19	20	21	MHz
Oscillation frequency 2 (LFCLK)	Fosc2	-	-	24	32	40	kHz
Oscillation frequency 3 (XCLK)	Fosc3	XIN XOUT	Values of a usable external CERALOCK ceramic resonator or crystal	16 (Note)	-	20 (Note)	MHz

Note: Typical value of an external oscillator.
Contact the manufacturer of external components for the matching with XCLK.
Toshiba has tested the CSTNE16M0VH3C000R0 and CSTNE20M0VH3C000R0 and confirmed that they operate with the XCLK properly.

12.7. 12-Bit ADC

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Conversion time 1	Tconv1	-	Settling time + Conversion time MADCCLK=30MHz	-	1.33	-	μs
INL1	Inl1	-	Guaranteed by design	-2	-	2	LSB
DNL1	Dnl1	-	Guaranteed by design	-1	-	2	LSB
Total error 1	Err_total1	-	Guaranteed by design	-6	-	6	LSB
Input voltage division ratio	Ratio_r1	VBATD	Buffer input voltage division ratio Input voltage range: 6 to 27 V	0.095	0.1	0.105	Times

Note: When the MADC is enabled, the pull-down resistors for reducing the input voltage have a value of 250 kΩ typical.

12.8. 10-Bit ADC

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Conversion time 2	Tconv2	-	Settling time + Conversion time GADCCLK=10MHz	-	16.4	-	µs
INL2	Inl2	-	-	-2.5	-	2.5	LSB
DNL2	Dnl2	-	-	-1.5	-	1.5	LSB
Total error 2	Err_total2	-	-	-3	-	3	LSB
Input voltage division ratio	Ratio_r2	VMON	Buffer input voltage division ratio Input voltage range: 6 to 27 V	0.095	0.1	0.105	Times
Amplifier error	Err_amp2	-	Buffer amplifier input-output differential Input voltage range between 0.2 V and supply voltage	-10	-	10	mV

12.9. Predriver Circuit (PREDRV)

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Output voltage HH1	Vohh1	GHU GHV GHW	High-side high-level output Referenced to the source of FETs VBAT ≥ 8 V, Icp=31.8 mA Cload=15,000 pF (Note1)	8	10	14	V
Output voltage HH2	Vohh2		High-side high-level output Referenced to the source of FETs VBAT ≥ 6V, Icp=31.8 mA Cload=15,000 pF (Note1)	4.5	-	14	V
Output voltage HH3	Vohh3		High-side high-level output Referenced to the source of FETs VBAT ≥ 4.8V, Icp=31.8 mA Cload=15,000 pF (Note1) Process variations are not considered. (Only temperature variations are considered.) Guaranteed by design	3.8	-	14	V
Output voltage HH4	Vohh4		High-side high-level output Referenced to the source of FETs VBAT ≥ 5V, Icp=13.8mA Cload=5,500 pF (Note2)	4.5	-	14	V
Output voltage LH	Volh		High-side low-level output Igx=100 μA * The VB values of 4.8 to 6 V and 18 to 27 V are guaranteed by design.	-0.1	-	0.1	V
Output voltage HL1	Vohl1	GLU GLV GLW	Low-side high-level output Referenced to the source of FETs VBAT ≥ 8 V, Icp=31.8 mA Cload=15,000 pF (Note1)	8	10	14	V
Output voltage HL2	Vohl2		Low-side high-level output Referenced to the source of FETs VBAT ≥ 6V, Icp=31.8 mA Cload=15,000 pF (Note1)	4.5	-	14	V
Output voltage HL3	Vohl3		Low-side high-level output Referenced to the source of FETs VBAT ≥ 4.8 V, Icp=31.8 mA Cload=15,000 pF (Note1) Process variations are not considered. (Only temperature variations are considered.) Guaranteed by design	3.8	-	14	V
Output voltage HL4	Vohl4		Low-side high-level output Referenced to the source of FETs Guaranteed by design: VBAT ≥ 5 V	4.5	-	14	V
Output voltage LL	Voll		Low-side low-level output Igx=100 μA * The VBAT values of 4.8 to 6 V and 18 to 27 V are guaranteed by design.	-0.1	-	0.1	V

Note1: Although the PREDRV specifications are prescribed at an Icp of 31.8 mA (i.e., a load current of the charge pump assuming that six FETs with a total Cloud of 15,000 pF are driven at a PWM frequency of 20 kHz), these output voltage characteristics are tested with a load current (Igx) of -100 μA.

Note2: Although the PREDRV specifications are prescribed at an Icp of 13.8 mA (i.e., a load current of the charge pump if six FETs with a total Cloud of 5,500 pF are driven at a PWM frequency of 20 kHz), this output voltage characteristic is tested with a load current (Igx) of -100 μA.

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Phase-1 charge current 1	Iphase1c1	GHU GHV GHW GLU GLV GLW	Minimum setting for Phase 1: [PREDRVSRCR]<IPHASE1> = 0000 (0mA) * Common to the high-side and low-side predrivers	-0.1	0	0.1	mA
Phase-1 charge current 2	Iphase1c2		[PREDRVSRCR]<IPHASE1> = 1000 (15mA) * Common to the high-side and low-side predrivers	-19.5	-15	-10.5	mA
Phase-1 charge current 3	Iphase1c3		[PREDRVSRCR]<IPHASE1> = 1001 (30mA) * Common to the high-side and low-side predrivers	-39	-30	-21	mA
Phase-1 charge current 4	Iphase1c4		[PREDRVSRCR]<IPHASE1> = 1011 (60mA) * Common to the high-side and low-side predrivers	-78	-60	-42	mA
Phase-1 charge current 5	Iphase1c5		Maximum setting Phase 1: [PREDRVSRCR]<IPHASE1> = 1111 (120mA) * Common to the high-side and low-side predrivers	-156	-120	-84	mA

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Phase-2 high-side current 1	Iphase2h1	GHU GHV GHW GLU GLV GLW	Minimum high-side setting for Phase 2: [PREDRVSRCR]<IPHASE2H> = 00000 (1mA)	-1.4	-1	-0.6	mA
Phase-2 high-side current 2	Iphase2h2		[PREDRVSRCR]<IPHASE2H> = 00001 (2mA)	-2.6	-2	-1.4	mA
Phase-2 high-side current 3	Iphase2h3		[PREDRVSRCR]<IPHASE2H> = 00011 (4mA)	-5.2	-4	-2.8	mA
Phase-2 high-side current 4	Iphase2h4		[PREDRVSRCR]<IPHASE2H> = 00111 (8mA)	-10.4	-8	-5.6	mA
Phase-2 high-side current 5	Iphase2h5		[PREDRVSRCR]<IPHASE2H> = 01111 (16mA)	-20.8	-16	-11.2	mA
Phase-2 high-side current 6	Iphase2h6		[PREDRVSRCR]<IPHASE2H> = 10000 (18mA)	-23.4	-18	-12.6	mA
Phase-2 high-side current 7	Iphase2h7		[PREDRVSRCR]<IPHASE2H> = 10001 (20mA)	-26	-20	-14	mA
Phase-2 high-side current 8	Iphase2h8		[PREDRVSRCR]<IPHASE2H> = 10011 (24mA)	-31.2	-24	-16.8	mA
Phase-2 high-side current 9	Iphase2h9		[PREDRVSRCR]<IPHASE2H> = 10111 (32mA)	-41.6	-32	-22.4	mA
Phase-2 high-side current 10	Iphase2h10		Maximum high-side setting for Phase 2: [PREDRVSRCR]<IPHASE2H> = 11111 (48mA)	-62.4	-48	-33.6	mA

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Phase-2 low-side current 1	Iphase2l1	GHU GHV GHW GLU GLV GLW	Minimum low-side setting for Phase 2: [PREDRVSRCR]<IPHASE2L> = 00000 (1mA)	-1.4	-1	-0.6	mA
Phase-2 low-side current 2	Iphase2l2		[PREDRVSRCR]<IPHASE2L> = 00001 (2mA)	-2.6	-2	-1.4	mA
Phase-2 low-side current 3	Iphase2l3		[PREDRVSRCR]<IPHASE2L> = 00011 (4mA)	-5.2	-4	-2.8	mA
Phase-2 low-side current 4	Iphase2l4		[PREDRVSRCR]<IPHASE2L> = 00111 (8mA)	-10.4	-8	-5.6	mA
Phase-2 low-side current 5	Iphase2l5		[PREDRVSRCR]<IPHASE2L> = 01111 (16mA)	-20.8	-16	-11.2	mA
Phase-2 low-side current 6	Iphase2l6		[PREDRVSRCR]<IPHASE2L> = 10000 (18mA)	-23.4	-18	-12.6	mA
Phase-2 low-side current 7	Iphase2l7		[PREDRVSRCR]<IPHASE2L> = 10001 (20mA)	-26	-20	-14	mA
Phase-2 low-side current 8	Iphase2l8		[PREDRVSRCR]<IPHASE2L> = 10011 (24mA)	-31.2	-24	-16.8	mA
Phase-2 low-side current 9	Iphase2l9		[PREDRVSRCR]<IPHASE2L> = 10111 (32mA)	-41.6	-32	-22.4	mA
Phase-2 low-side current 10	Iphase2l10		Maximum low-side setting for Phase 2: [PREDRVSRCR]<IPHASE2L> = 11111 (48mA)	-62.4	-48	-33.6	mA
Phase-3 current	Iphase3		Maximum high-side setting for Phase 2: [PREDRVSRCR]<IPHASE2H> = 11111 (48mA) Maximum low-side setting for Phase 2: [PREDRVSRCR]<IPHASE2H> = 11111 (48mA) * Separate to the high-side and low-side predrivers	-218.4	-168	-117.6	mA

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Output resistor 1	Routh	GHU GHV GHW	High-side discharge side Iol=-20 mA	2	5.4	12	Ω
Output resistor 2	Routl	GLU GLV GLW	Low-side discharge side Iol=-20 mA	2	5.4	12	Ω
Input propagation delay time 1	Thondelay	GHU GHV GHW GLU GLV GLW	High-side turn-on Cload=15,000 pF, 25% of VGHx Phase-1 charge current setting register [PREDRVSRCR]<IPHASE1> = 111 (120 mA max) Phase -2 charge current setting register [PREDRVSRCR]<IPHASE2H> = 11111 (48 mA max) Total: 168 mA U, V, W, SLC= 0 V (See Figure 12.9.1.)	-	0.4	1.0	μs
Input propagation delay time 2	Thoffdelay		High-side turn-off Cload=15,000 pF, 75% of VGHx U, V, W, SLC= 0 V (External parts: R=47 Ω, C=15,000 pF) Observed outside the 47-Ω resistor (See Figure 12.9.1.)	-	0.3	1.0	μs
Input propagation delay time 3	Tlondelay		Low-side turn-on Cload=15,000 pF, 25% of VGLx Phase-1 charge current setting register [PREDRVSRCR]<IPHASE1>= 111 (120 mA max) Phase -2 charge current setting register [PREDRVSRCR]<IPHASE2L>= 11111 (48 mA max) Total: 168 mA 10%-90% U, V, W, SLC= 0 V (See Figure 12.9.1.)	-	0.4	1.0	μs
Input propagation delay time 4	Tloffdelay		Low-side turn-off Cload=15,000 pF, 75% of VGLx U, V, W, SLC= 0 V (External parts: R=47 Ω, C=15,000 pF) Observed outside the 47-Ω resistor (See Figure 12.9.1.)	-	0.3	1.0	μs

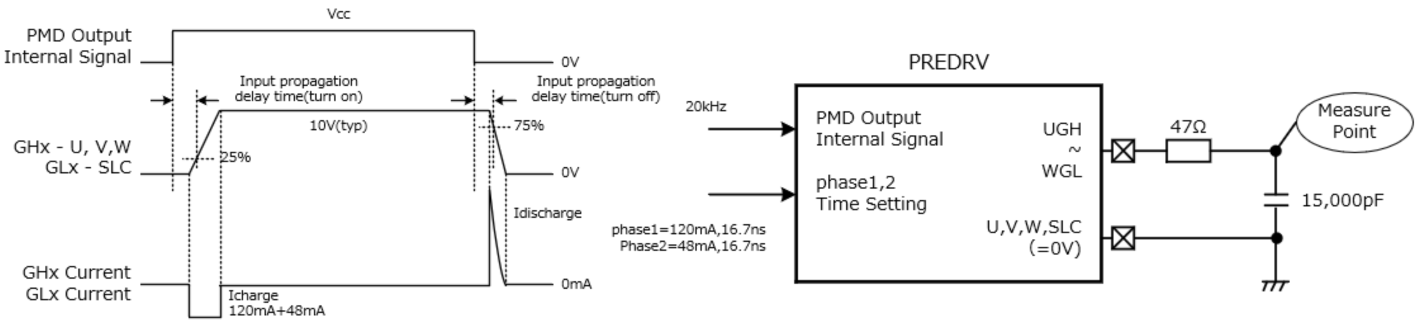


Figure 12.9.1 Measurement of Input Propagation Delay Times and Measurement circuit diagram

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Initial Phase-1 period 1	Tphase1i1	-	VECLK=60MHz [MCSSDRVPTSR]<TPHASE1>: 000000 (0 ns, minimum setting) Guaranteed by design	-	0	-	ns
Initial Phase-1 period 2	Tphase1i2	-	VECLK=60MHz [MCSSDRVPTSR]<TPHASE1>: 000001 (16.7 ns)	15.8	16.7	17.5	ns
Initial Phase-1 period 3	Tphase1i3	-	VECLK=60MHz [MCSSDRVPTSR]<TPHASE1>: 000011 (50 ns)	47.5	50	52.5	ns
Initial Phase-1 period 4	Tphase1i4	-	VECLK=60MHz [MCSSDRVPTSR]<TPHASE1>: 000111 (116.7 ns)	110.9	116.7	122.5	ns
Initial Phase-1 period 5	Tphase1i5	-	VECLK=60MHz [MCSSDRVPTSR]<TPHASE1>: 001111 (250 ns)	237.5	250	262.5	ns
Initial Phase-1 period 6	Tphase1i6	-	VECLK=60MHz [MCSSDRVPTSR]<TPHASE1>: 011111 (516.7 ns)	490.9	516.7	542.5	ns
Initial Phase-1 period 7	Tphase1i7	-	VECLK=60MHz [MCSSDRVPTSR]<TPHASE1>: 111111 (1050 ns, maximum setting)	997.5	1050	1102.5	ns

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Phase-2 target period 1	Tphase2t1	-	VECLK=60MHz [MCSSDRVPTSR]<TPHASE2>: 0000000 (0 ns, minimum setting) Guaranteed by design	-	0	-	ns
Phase-2 target period 2	Tphase2t2	-	VECLK=60MHz [MCSSDRVPTSR]<TPHASE2>: 0000001 (16.7 ns)	15.8	16.7	17.5	ns
Phase-2 target period 3	Tphase2t3	-	VECLK=60MHz [MCSSDRVPTSR]<TPHASE2>: 0000011 (50 ns)	47.5	50	52.5	ns
Phase-2 target period 4	Tphase2t4	-	VECLK=60MHz [MCSSDRVPTSR]<TPHASE2>: 0000111 (116.7 ns)	110.9	116.7	122.5	ns
Phase-2 target period 5	Tphase2t5	-	VECLK=60MHz [MCSSDRVPTSR]<TPHASE2>: 0001111 (250 ns)	237.5	250	262.5	ns
Phase-2 target period 6	Tphase2t6	-	VECLK=60MHz [MCSSDRVPTSR]<TPHASE2>: 0011111 (516.7 ns)	490.9	516.7	542.5	ns
Phase-2 target period 7	Tphase2t7	-	VECLK=60MHz [MCSSDRVPTSR]<TPHASE2>: 0111111 (1050 ns)	997.5	1050	1102.5	ns
Phase-2 target period 8	Tphase2t8	-	VECLK=60MHz [MCSSDRVPTSR]<TPHASE2>: 1111111 (2116.7 ns)	2010.9	2116.7	2222.5	ns
Dead time	Tdead	-	Dead-Time register: [DTR]<DTR[9:0]> = 0x02D When dead time is programmed to be 3 µs. VECLK=60 MHz	2.85	3	3.15	µs

12.10. Current-Sense Amplifier (CSAMP)

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Input common-mode voltage range	Vcomin	RSH RSL	-	-0.2	-	2.0	V
Gain 1	Gain1		Programmed to be ×5	4.95	5	5.05	Times
Gain 2	Gain2		Programmed to be ×10	9.9	10	10.1	Times
Gain 3	Gain3		Programmed to be ×15	14.85	15	15.15	Times
Gain 4	Gain4		Programmed to be ×20	19.8	20	20.2	Times
Gain 5	Gain5		Programmed to be ×40	39.6	40	40.4	Times
Gain 6	Gain6		Programmed to be ×60	59.25	59.85	60.45	Times
Output offset voltage 1	Vooffset1	-	Programmed to be Vcc/ 2 * Gain60 after calibration, including input offset	VCC/2 -0.0606	2.5	VCC/2 +0.0606	V
Output offset voltage 2	Vooffset2	-	Programmed to be Vcc/ 5 * Gain60 after calibration, including input offset	VCC/5 -0.0606	1.0	VCC/5 +0.0606	V
Output offset voltage 3	Vooffset3	-	Programmed to be Vcc/ 8 * Gain60 after calibration, including input offset	VCC/8 -0.0606	0.625	VCC/8 +0.0606	V
Output offset voltage 4	Vooffset4	-	Programmed to be Vcc/ 10 * Gain60 after calibration, including input offset	VCC/10 -0.0606	0.5	VCC/10 +0.0606	V
Settling time 1	Tsettle1	-	Gain = 5, output voltage: 2.5V ↔ 3.5 V No external input filter Time required for the output voltage to settle to within ±2% of its final value Guaranteed by design (See Figure 12.10.1)	-	-	0.5	μs
Settling time 2	Tsettle2	-	Gain = 20, output voltage: 2.5V ↔ 3.5 V No external input filter Time required for the output voltage to settle to within ±2% of its final value Guaranteed by design (See Figure 12.10.1)	-	-	0.8	μs
Settling time 3	Tsettle3	-	Gain = 60, output voltage: 2.5V ↔ 3.5 V No external input filter Time required for the output voltage to settle to within ±2% of its final value Guaranteed by design (See Figure 12.10.1)	-	-	1.7	μs
High-level output voltage	Voh_amp	-	-	VCC-0.3	-	-	V
Low-level output voltage	Vol_amp	-	-	-	-	0.3	V

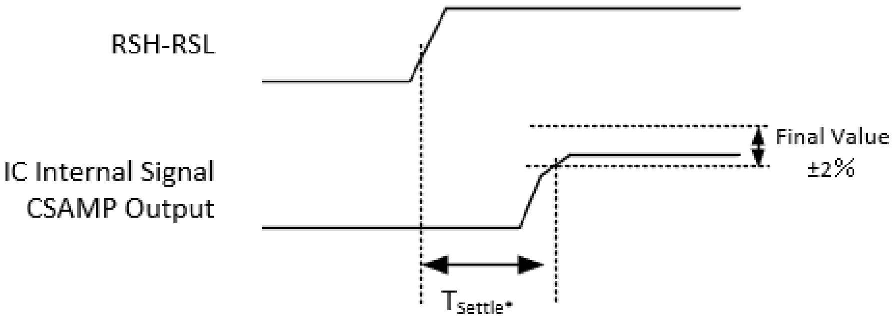


Figure 12.10.1 Measurement of Settling Time

12.11. Current Clamp Comparator (CLCMP)

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Current-limiting voltage threshold 1	Vlimit1	-	[CLCMPSR]<CLCMPTV> = 00000 Minimum setting	-39	0	39	mV
Current-limiting voltage threshold 2	Vlimit2	-	[CLCMPSR]<CLCMPTV> = 00001	VCC × 1/32 -0.039	0.156	VCC × 1/32+0.039	V
Current-limiting voltage threshold 3	Vlimit3	-	[CLCMPSR]<CLCMPTV> = 00011	VCC × 3/32-0.039	0.468	VCC × 3/32+0.039	V
Current-limiting voltage threshold 4	Vlimit4	-	[CLCMPSR]<CLCMPTV> = 00111	VCC × 7/32-0.039	1.094	VCC × 7/32+0.039	V
Current-limiting voltage threshold 5	Vlimit5	-	[CLCMPSR]<CLCMPTV> = 01111	VCC × 15/32-0.039	2.344	VCC × 15/32+0.039	V
Current-limiting voltage threshold 6	Vlimit6	-	[CLCMPSR]<CLCMPTV>=11111 Maximum setting	VCC × 31/32-0.039	4.844	VCC × 31/32+0.039	V
Digital filtering time 1	Tclfil1	-	OVV Control register: [OVVCR]<OVVCNT[4:0]> = 0x0F VECLK = 60 MHz (See Figure 12.2.1)	3.8	4.0	4.2	μs
Digital filtering time 4	Tclfil4	-	OVV Control register: [OVVCR]<OVVCNT[4:0]> = 0x06 VECLK = 60 MHz (See Figure 12.2.1)	1.52	1.6	1.68	μs
Digital filtering time 2	Tclfil2	-	[CLCMPDFSR]<CLCMPDFS>=0 32 count at 10 MHz (See Figure 12.2.1)	3.04	3.2	3.36	μs
Digital filtering time 3	Tclfil3	-	[CLCMPDFSR]<CLCMPDFS>=1 16 count at 10 MHz (See Figure 12.2.1)	1.52	1.6	1.68	μs

Note: Digital filtering time 1 and 4 is a characteristic of a digital filter located on a different path from the one with digital filtering time 2 and digital filtering time 3.
The digital filter with digital filtering time 1 and 4 can be disabled via a special function register.

12.12. Overcurrent Detection Comparator (OCCMP)

Vbat=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Voltage threshold 1 for overcurrent detection	Voc1	-	[OCCMPSR]<OCCMPTV> = 0000 Minimum setting	-39	0	39	mV
Voltage threshold 2 for overcurrent detection	Voc2	-	[OCCMPSR]<OCCMPTV> = 0001	VCC × 1/16 -0.039	0.313	VCC × 1/16+0.039	V
Voltage threshold 3 for overcurrent detection	Voc3	-	[OCCMPSR]<OCCMPTV> = 0011	VCC × 3/16 -0.039	0.9375	VCC × 3/16+0.039	V
Voltage threshold 4 for overcurrent detection	Voc4	-	[OCCMPSR]<OCCMPTV> = 0111	VCC × 7/16 -0.039	2.1875	VCC × 7/16+0.039	V
Voltage threshold 5 for overcurrent detection	Voc5	-	[OCCMPSR]<OCCMPTV> = 1111 Maximum setting	VCC × 15/16 -0.039	4.6875	VCC × 15/16+0.039	V
Digital filtering time 1	Tocfil1	-	[EMGCR]<EMGCNT[4:0]> = 0x06 VECLK = 60 MHz (See Figure 12.2.1)	1.52	1.6	1.68	μs
Digital filtering time 2	Tocfil2	-	[OCCMPDFSR]<OCCMPDFS> = 0 32 count at 10 MHz (See Figure 12.2.1)	3.04	3.2	3.36	μs
Digital filtering time 3	Tocfil3	-	[OCCMPDFSR]<OCCMPDFS> = 1 16 count at 10 MHz (See Figure 12.2.1)	1.52	1.6	1.68	μs

Note: Note that the longer one of digital filtering time 1 and digital filtering time 2/3 becomes effective.
The digital filter with digital filtering time 1 can be disabled via a special function register.

12.13. Back-EMF Comparator (BEMFCMP)

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Input voltage range	Vinrange	U, V, W, COM	Input via a 47-Ω resistor COM has half the voltage of the phase voltage.	-2.5	-	VBAT	V
Input offset voltage 1	Voffset1	U, V, W, COM	COM = 0 V COM voltage phase difference.	-80	-	80	mV
Input offset voltage 21	Voffset21		COM=VBAT/2, VBAT=6V COM voltage phase difference.	-75	-	75	mV
Input offset voltage 22	Voffset22		COM=VBAT/2, VBAT=12 V COM voltage phase difference.	-50	-	50	mV
Input offset voltage 23	Voffset23		COM=VBAT/2, VBAT=18 V COM voltage phase difference.	-75	-	75	mV
Input offset voltage 1 phase differential	Voffset1d	U, V, W	COM= 0 V, U-V, V-W, and W-U phase differentials	-99	-	99	mV
BEMFCMP filtering time	Tbemffil	-	Input Processing Control register: [INPCR]<FILVAL[6:0]> = 0x3C VECLK = 60 MHz (See Figure 12.2.1)	0.95	1	1.05	μs

12.14. Thermal Shutdown (TSD) Circuit

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
TSD detection temperature	Ttsd	-	Guaranteed by design	175	190	205	°C
TSD recovery temperature	Ttsdr	-	Guaranteed by design	145	160	175	°C

Note:
- TSD is not tested in a pre-shipment test. Only an evaluation is performed.
- The TSD circuits for the 5-volt regulator (LDO5V) and the LINPHY have the same electrical characteristics.

12.15. Open/Short Comparator (OSCMP) for External FETs

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Short-circuit detection threshold 1	Vos1	VBATD U, V, W SLC	VBATD-U/V/W, U/V/W-SLC [OSCMPSR]<OSCMPT> = 000 Minimum setting	10	240	460	mV
Short-circuit detection threshold 2	Vos2		VBATD-U/V/W, U/V/W-SLC [OSCMPSR]<OSCMPT> = 001	60	280	510	mV
Short-circuit detection threshold 3	Vos3		VBATD-U/V/W, U/V/W-SLC [OSCMPSR]<OSCMPT> = 010	160	380	610	mV
Short-circuit detection threshold 4	Vos4		VBATD-U/V/W, U/V/W-SLC [OSCMPSR]<OSCMPT> = 011	270	480	720	mV
Short-circuit detection threshold 5	Vos5		VBATD-U/V/W, U/V/W-SLC [OSCMPSR]<OSCMPT> = 100	360	580	830	mV
Short-circuit detection threshold 6	Vos6		VBATD-U/V/W, U/V/W-SLC [OSCMPSR]<OSCMPT> = 101	460	680	940	mV
Short-circuit detection threshold 7	Vos7		VBATD-U/V/W, U/V/W-SLC [OSCMPSR]<OSCMPT> = 110, 111 Maximum setting	560	780	1050	mV
Input current 1 (Note1)	Iosin1	U, V, W	VBAT = 12 V, U/V/W pin voltage = 12 V [OSCMPSR]<OSCMPTV> = 000 [PREDRVER]<PREDRVEN>=0	69	-	165	μA
Input current 2 (Note1)	Iosin2		VBAT = 12 V, U/V/W pin voltage = 0 V [OSCMPSR]<OSCMPTV> = 000 [PREDRVER]<PREDRVEN>=0	-5.0	-	5.0	μA
Input current 3	Iosin3	SLC	[OSCMPSR]<OSCMPTV> = 11x [PREDRVER]<PREDRVEN>=0 SLC pin sink current	-10	-	5	μA

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Digital filtering time 1 (Note2)	Tshortfil5	-	Time from the rising edge of the FET “on” signal to the Vds comparator output [OSCMPDFSR]<OSCMPDFS> = 00 64 count at 10 MHz (See Figure 12.2.1)	6.08	6.4	6.72	μs
Digital filtering time 2 (Note2)	Tshortfil6	-	Time from the rising edge of the FET “on” signal to the Vds comparator output [OSCMPDFSR]<OSCMPDFS> = 01 48 count at 10 MHz (See Figure 12.2.1)	4.56	4.8	5.04	μs
Digital filtering time 3 (Note2)	Tshortfil7	-	Time from the rising edge of the FET “on” signal to the Vds comparator output [OSCMPDFSR]<OSCMPDFS> = 10 32 count at 10 MHz (See Figure 12.2.1)	3.04	3.2	3.36	μs
Digital filter time 4 (Note2)	Tshortfil8	-	Time from the rising edge of the FET “on” signal to the Vds comparator output [OSCMPDFSR]<OSCMPDFS> = 11 16 count at 10 MHz (See Figure 12.2.1)	1.52	1.6	1.68	μs

Note1: The U, V, and W pins are also connected to other circuit blocks. Iosin2 and Iosin2 include the amount of input currents to these circuit blocks.

Note2: The filtering time of the digital filter for the OSCMP is the longer of the time shown above (Tshortfil5 to Tshortfil8) and digital filtering time 1 (Tocfil1) of the OCCMP shown in Section 12.12.

12.16. LIN

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Supply voltage range	V_{VB}	VBAT	ECU operating voltage range (Param 9)	8.0	-	18.0	V
Supply voltage range	V_{SUP}		Note：Param 10 of LIN configuration is defined 7.0V(min), IC requires 6.0V(min) on 5V regulator.	6.0	-	18.0	V
Supply voltage MAX Ratings	$V_{SUP\_NON\_OP}$		Voltage range with in which the device is not destroyed. An optional time limit for the maximum value shall be at least 400 ms. No guarantee of correct operation. (Param 11)	-0.3	-	40	V
BUS MAX Ratings	$V_{BUS\_MAX\_RATING}$	LIN	Voltage range with in which the device is not destroyed. (Param 82) An optional time limit for the maximum value shall be at least 400 ms. No guarantee of correct operation.	-27	-	40	V
Receiver threshold voltage, recessive to dominant edge	V_{th_rec}		Low Voltage: Recessive Input Threshold(SAE)	0.4	-	0.53	V_{SUP}
Receiver threshold voltage, dominant to recessive edge	V_{th_dom}		High Voltage: Dominant Input Threshold(SAE)	0.47	-	0.6	V_{SUP}
BUS current limitation	I_{BUS_LIM}		Current Limitation for Driver dominant state driver on VBUS = VBAT_maxd (Param 12)	40	-	200	mA
Leakage current (dominant)	$I_{BUS\_PAS\_dom}$		Input leakage current at the receiver incl. slave pull-up resistor as specified in Param 26 driver off VBUS = 0 V VBAT = 12 V (Param 13)	-1	-	-	mA
Leakage current (recessive)	$I_{BUS\_PAS\_rec}$		Driver off 8 V < VBAT < 18 V, 8 V < VBUS < 18 V, VBUS > VBAT (Param 14)	-	-	20	μA
Leakage current1	$I_{BUS\_NO\_GND}$		Control unit disconnected from ground GNDDevice = VSUP 0 V < VBUS < 18 V VBAT = 12 V Loss of local ground shall not affect communication in the residual network. (Param 15)	-1	-	1	mA
Leakage current2	$I_{BUS\_NO\_BAT}$		VBAT disconnected VSUP = GND 0 V < VBUS < 18 V Node shall sustain the current that can flow under this condition. Bus shall remain operational under this condition. (Param 16 and SAE)	-	-	23	μA
Voltage of Receiver dominant state	V_{BUS_dom}		Receiver dominant state Note: Param 17 of LINPHY configuration is not defined minimum voltage. (Param 17)	-27	-	0.4 x VBAT	V

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Voltage of Receiver recessive state	V_{BUS_rec}	LIN	Receiver recessive state (Param 18)	0.6	-	-	V_{SUP}
Receiver center voltage	V_{BUS_CNT}		VBUS_CNT = (Vth_dom + Vth_rec)/2 (Param 19)	0.475	-	0.525	V_{SUP}
Receiver hysteresis	V_{HYS}		VHYS = Vth_rec–Vth_dom (Param 20 and SAE)	0.07	-	0.175	V_{SUP}
Duty cycle D1 (for worst case at 20 kbps)	D1		THRec(max) =0,744 × VSUP; THDom(max) =0,581 × VSUP; VSUP = 7,0 V to 18 V; tBIT = 50 μs; D1 = tBus_rec(min)/(2 × tBIT) (Param 27) <PHYFBRM>=0	0.396	-	-	-
Duty cycle D2 (for worst case at 20 kbps)	D2		THRec(min) =0,422 × VSUP; THDom(min) =0,284 × VSUP; VSUP = 7,6 V to 18 V; tBIT = 50 μs; D2 = tBus_rec(max)/(2 × tBIT) (Param 28) <PHYFBRM>=0	-	-	0.581	-
Duty cycle D3 (for worst case at 10 kbps)	D3		THRec(max) =0,778 × VSUP; THDom(max) =0,616 × VSUP; VSUP = 7,0 V to 18 V; tBIT = 96 μs; D3 = tBus_rec(min)/(2 × tBIT) (Param 29) <PHYFBRM>=0	0.417	-	-	-
Duty cycle D4 (for worst case at 10 kbps)	D4		THRec(min) =0,389 × VSUP; THDom(min) =0,251 × VSUP; VSUP = 7,6 V to 18 V; tBIT = 96 μs; D4 = tBus_rec(max)/(2 × tBIT) (Param 30) <PHYFBRM>=0	-	-	0.59	-
Propagation delay	t_{rx_pd}		Propagation delay of receiver (Param 31) ・bus dominant to RxD LOW(t_{rx_pdf}) ・bus recessive to RxD HIGH(t_{rx_pdr}) (See Figure 12.16.1)	-	-	6	μs
Receiver delay symmetry	t_{rx_sym}		Symmetry of receiver propagation delay rising edge with respect to falling edge (Param 32) $t_{rx\_sym} = t_{rx\_pdf} - t_{rx\_pdf}$	-2	-	2	μs
Bus pull-up resistance1	R_{SLAVE}		internal resistance (Param 26)	20	30	60	kΩ
Bus pull-up resistance2	R_{MASTER}		The serial diode is mandatory. Only for valid for transceiver with integrated master pull-up resistor. (Param 25) external resistance	900	-	1100	Ω
LIN input capacity (Guaranteed by design)	C_{SLAVE}		Capacitance of slave node (Param 37) 250pF -220pF = 30pF max	-	-	30	pF
Current consumption in sleep mode (Guaranteed by design)	I_{sleep_LIN}	VBAT	VBAT=12V, RT=25℃, Only working LIN bus Wakeup signal Only LINPHY current consumption at [PMUSCR]<LIN_MODE>=0(Sleep Operate Mode)	-	-	3	μA

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Dominant time for bus Wakeup	t_{WAKE}	LIN	Wakeup pulse width from LIN bus (See Figure 12.16.2)	30	-	150	μs
Turn off time to sleep	t_{sleep}	-	Turn off time from Standby or Active to Sleep mode	-	-	1	ms
Wake-up threshold voltage	V_{BUSwk}	LIN	Threshold voltage for Wakeup signal detection	0.4	0.5	0.6	V_{SUP}
ESD Susceptibility HBM1 pins LIN vs. LINGND	V_{ESDLIN}	LIN	IEC61000-4-2 Conducted HBM	-6	-	6	kV
ESD Susceptibility HBM3 pins LIN vs. LINGND	$V_{ESDLIN3}$		AEC-Q100-002	-6	-	6	kV

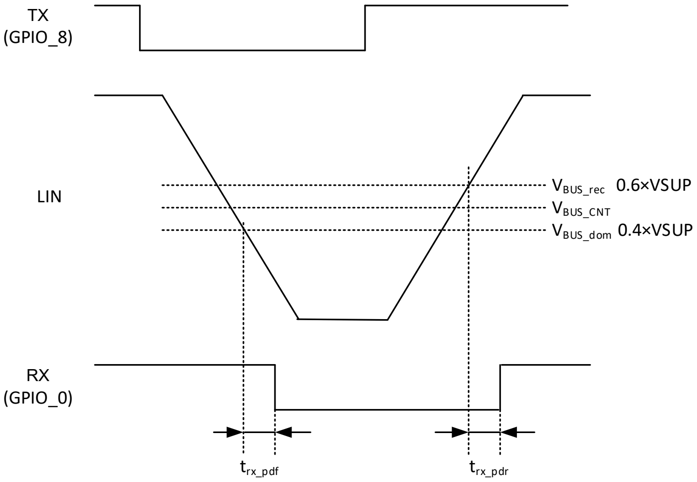


Figure 12.16.1 Measurement of LIN Propagation delay

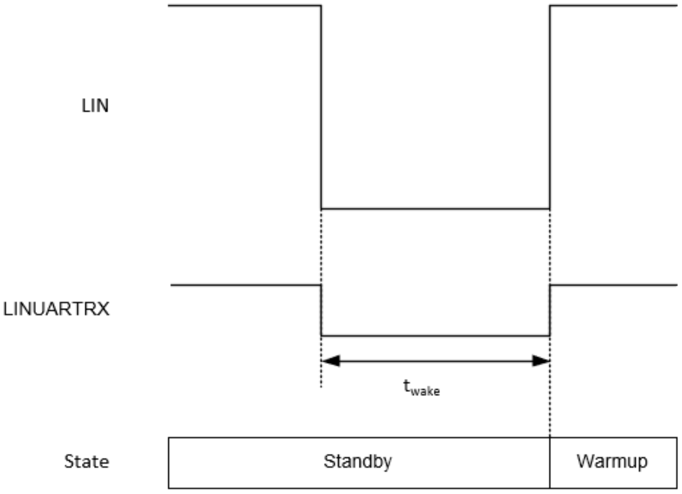


Figure 12.16.2 Measurement of LIN Dominant time for bus Wakeup

12.17. PWM Communication Circuit 1

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Output voltage H1	Vouth1	LIN	Pull-up resistor: 3.6 kΩ	VBAT-1.0	-	VBAT	V
Output voltage L1	Voutl1		Pull-up resistor: 3.6 kΩ	0	-	1.2	V

Note: Since the LIN Bus and PWM Communication Circuit 1 shares the LIN bus, they have the same electrical characteristics.

12.18. PWM Communication Circuit 2

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
High-level input threshold voltage	Vinh	PWMIN	-	VCC ×0.86	VCC ×0.91	VCC ×0.96	V
Low-level input threshold voltage	Vinl		-	VCC ×0.82	VCC ×0.87	VCC ×0.92	V
Input threshold voltage hysteresis	Vinhys		Vinhys=Vinh-Vinl Guaranteed by design	-	0.2	-	V
Input current 1	Iin1		Vin=18 V	-	20	36	μA
Input current 2	Iin2		Vin=0 V	-1	-	1	μA
Input digital filter	Tpwmfil		The assumption is that the input digital filter for the CAPT is used. When CPUCLK is 40 MHz and divided by 128 (See Figure 12.2.1)	6.08	6.4	6.72	μs
High-level output voltage	Vouth2	GPIO_9 /PWMOUT 0	Load condition: [GPOPSR]<GPIOPSx>=00: -1 mA [GPOPSR]<GPIOPSx>=01: -2 mA [GPOPSR]<GPIOPSx>=10: -4 mA [GPOPSR]<GPIOPSx>=11: -6 mA	VCC ×0.8	-	-	V
Low-level output voltage	Voutl2		Load condition: [GPOPSR]<GPIOPSx>=00: 1 mA [GPOPSR]<GPIOPSx>=01: 2 mA [GPOPSR]<GPIOPSx>=10: 4 mA [GPOPSR]<GPIOPSx>=11: 6 mA	-	-	0.5	V

12.19. UART

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Data rate	Fuart	GPIO_10/UART_RX, GPIO_11/UART_TX	-	-	-	1	Mbps

12.20. SPI

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
SCLK period (master)	Tm	SCLK	-(See Figure 12.20.1, Figure 12.20.2)	T×m ≥250 ns	-	-	ns
SCLK period (slave)	Ts		-(See Figure 12.20.3, Figure 12.20.4)	T×n ≥1 μs	-	-	ns
SCLK Low-level pulse width in Master mode	Twlm		-(See Figure 12.20.1, Figure 12.20.2)	0.4	-	0.6	Tm
SCLK High-level pulse width in Master mode	Twhm		-(See Figure 12.20.1, Figure 12.20.2)	0.4	-	0.6	Tm
SCLK Low-level pulse width in Slave mode	Twls		-(See Figure 12.20.3, Figure 12.20.4)	0.4	-	0.6	Ts
SCLK High-level pulse width in Slave mode	Twhs		-(See Figure 12.20.3, Figure 12.20.4)	0.4	-	0.6	Ts
SCLK rise/fall to SDO valid in Master mode	Todsm		-(See Figure 12.20.1, Figure 12.20.2)	-	-	50	ns
SCLK rise/fall to SDO hold in Master mode	Todhm		-(See Figure 12.20.1, Figure 12.20.2)	-20	-	-	ns
SCLK rise/fall to SDI valid in Master mode	Tidsm		-(See Figure 12.20.1, Figure 12.20.2)	55	-	-	ns
SDI hold time from SCLK rise/fall in Master mode	Tidhm		-(See Figure 12.20.1, Figure 12.20.2)	100	-	-	ns
CSN valid to SCLK rise/fall in Master mode	Tofsm	CSN SCLK	-(See Figure 12.20.1, Figure 12.20.2)	T×m -50	-	-	ns

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
SCLK rise/fall to SDO valid in Slave mode	Todss	SCLK	(See Figure 12.20.3, Figure 12.20.4)	-	-	3T+90	ns
SCLK rise/fall to SDO hold in Slave mode	Todhs		(See Figure 12.20.3, Figure 12.20.4)	2T	-	-	ns
SCLK rise/fall to SDI valid in Slave mode	Tidss		(See Figure 12.20.3, Figure 12.20.4)	10	-	-	ns
SCLK rise/fall edge to SDI hold in Slave mode	Tidhs		(See Figure 12.20.3, Figure 12.20.4)	3T+20	-	-	ns
CSN valid to SCLK rise/fall in Slave mode	Tifss	CSN SCLK	(See Figure 12.20.3, Figure 12.20.4)	T×n -20	-	-	ns
SCLK rise/fall to CSN deasserted in Master mode	Tofhm		(See Figure 12.20.1, Figure 12.20.2)	T×m -50	-	-	ns
SCLK rise/fall to CSN deasserted in Slave mode	Tifhs		(See Figure 12.20.3, Figure 12.20.4)	T×n -20	-	-	ns

Note:
- Load capacitance, CL = 100 pF
- [GPOPSR]< GPIOPSx>=11（6mA setting）
- The electric character of Section 39.22 is Guaranteed by design.
- T represents the SSPCLK period (e.g., 25 ns at 40 MHz).
- n represents a ratio of the SCLK period to the SSPCLK period (n ≥ 12).
- m represents the ratio of the SCLK period to the SSPCLK period (65024 ≥ m ≥ 12).

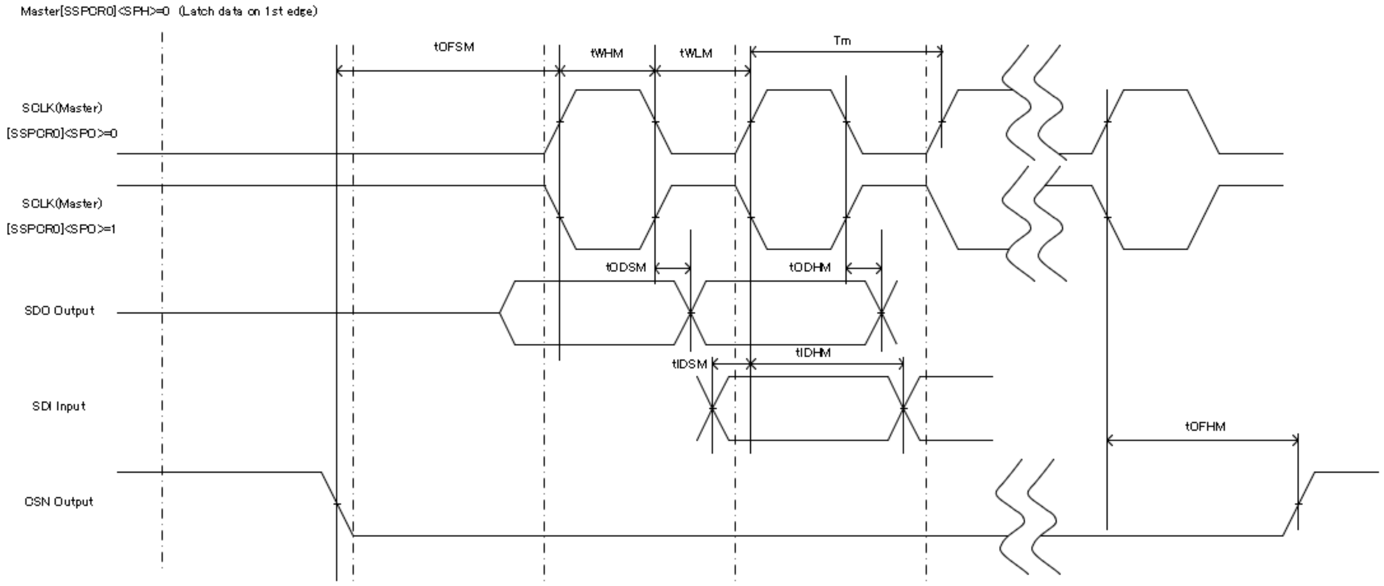


Figure 12.20.1 SPI Communication Waveform 1

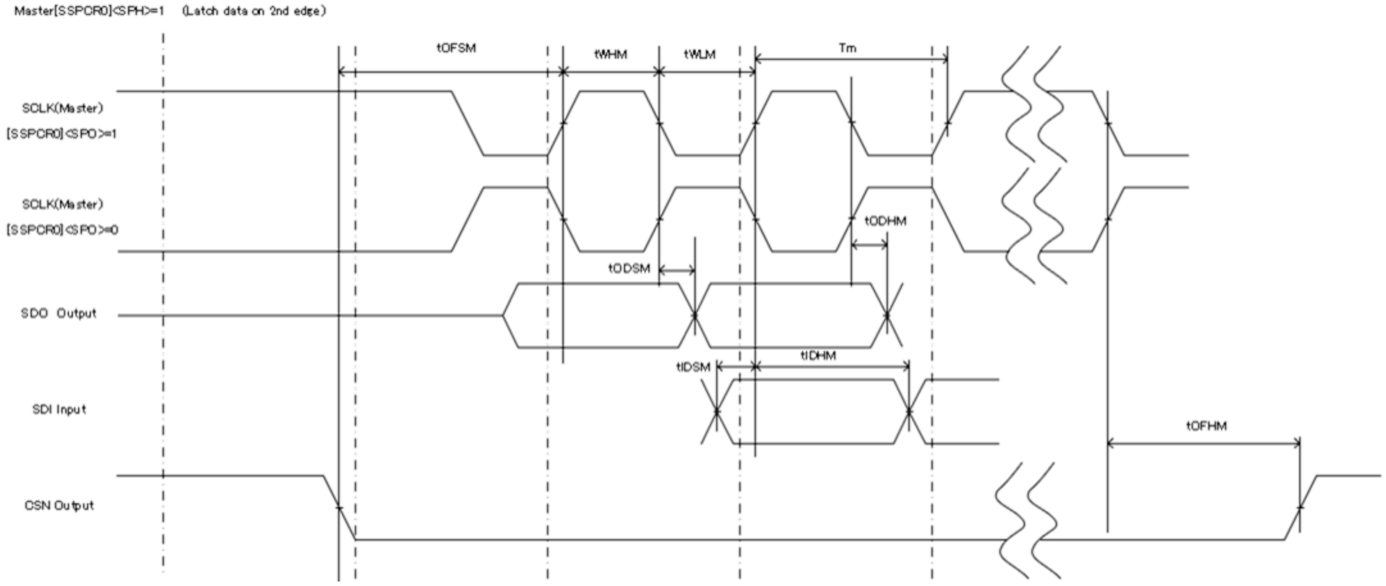


Figure 12.20.2 SPI Communication Waveform 2

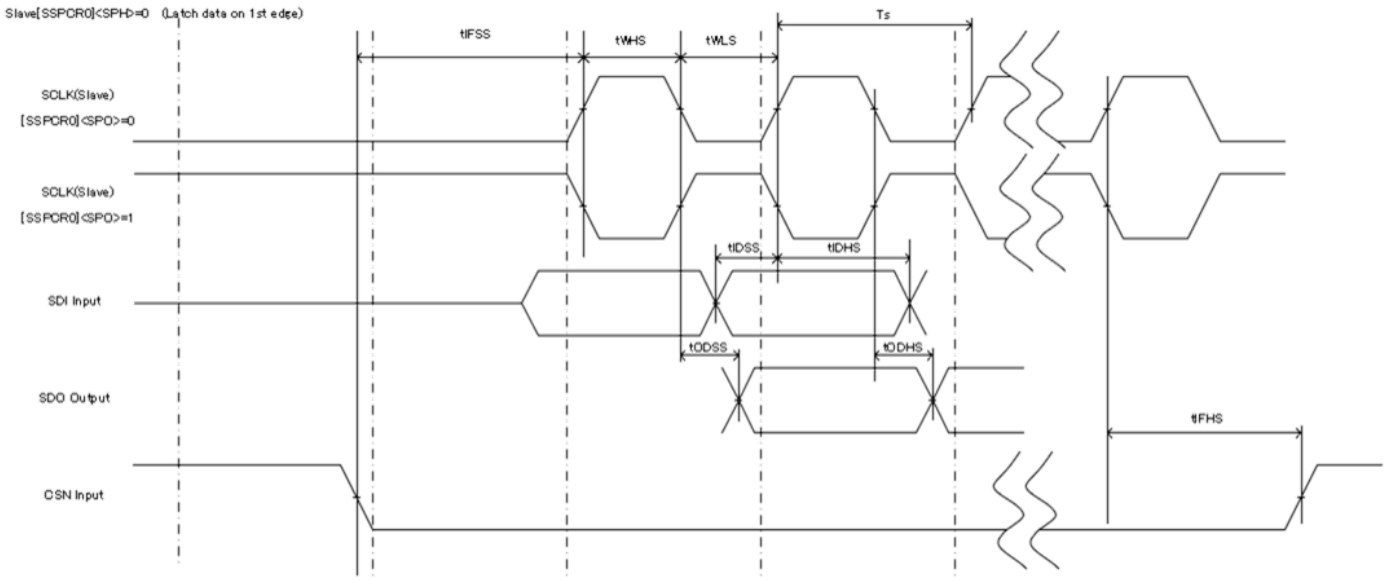


Figure 12.20.3 SPI Communication Waveform 3

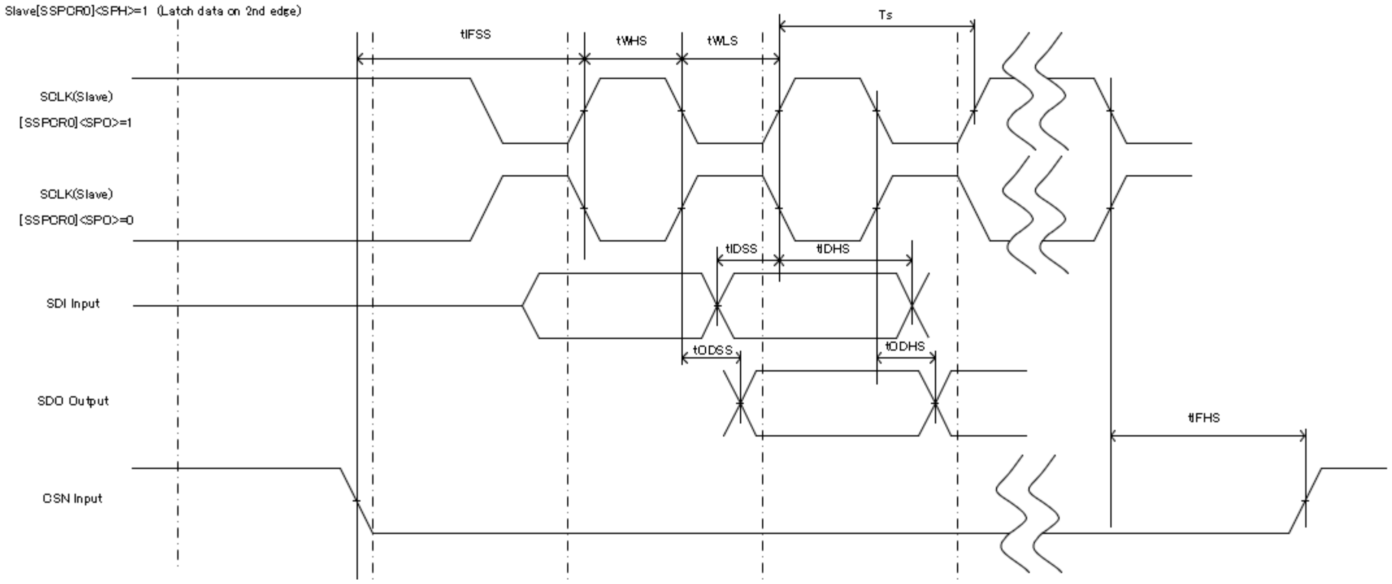


Figure 12.20.4 SPI Communication Waveform 4

12.21. GPIO

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
High-level input threshold voltage	Vinh*	GPIO_x	-	VCC×0.75	-	-	V
Low-level input threshold voltage	Vinl*		-	-	-	VCC ×0.25	V
Pull-up resistor	Rpullup		-	30	50	100	kΩ
Pull-down resistor	Rpulldown		-	30	50	100	kΩ
High-level output voltage	Vouth		Load condition: [GPOPSR]<GPIOPSx>=00: -1 mA [GPOPSR]<GPIOPSx>=01: -2 mA [GPOPSR]<GPIOPSx>=10: -4 mA [GPOPSR]<GPIOPSx>=11: -6 mA	VCC×0.8	-	-	V
Low-level output voltage	Voutl		Load condition: [GPOPSR]<GPIOPSx>=00: 1 mA [GPOPSR]<GPIOPSx>=01: 2 mA [GPOPSR]<GPIOPSx>=10: 4 mA [GPOPSR]<GPIOPSx>=11: 6 mA	-	-	0.5	V

12.22. Flash (Code Flash)

Vbat=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Conditions	Values			Unit
				Min.	Typ.	Max.	
Bus frequency	-	-	-	-	-	42	MHz
Read frequency	-	-	-	-	-	10.5	MHz
Data retention time 1	-	-	Tj=85°C, after 1,000 program/erase cycles	40	-	-	years
Flash capacity	-	-	-	-	64	-	Kbytes
Data access size	-	-	Same as read/write operations	-	Word (32 bits)	-	-
Erase time	-	-	64 KB, Tj = -40 to 150°C	-	80	-	ms
Program time	-	-	Tj = -40 to 150°C	-	2	-	s
Erase block size	-	-	-	-	8	-	Kbytes
Erase block time	-	-	1 block (8 Kbytes), Tj = -40 to 150°C	-	6.8	-	ms
Program block size	-	-	-	-	128	-	bytes
Program block time	-	-	128 bytes, Tj = -40 to 150°C	-	2.4	-	ms

Note: It is necessary to set the number of wait cycles for read access according to the bus frequency.

12.23. Other

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
High-level input threshold voltage	Vmd*inh	MD0 MD1	-	VCC ×0.75	-	-	V
Low-level input threshold voltage	Vmd*inl		-	-	-	VCC ×0.25	V
Pull-down resistor	Rmd*pd		-	30	50	100	kΩ

12.24. Thermal resistance

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Junction to Ambient	θJA	-	Thermal resistance between Junction and Ambient	-	30	-	℃/W
Junction to Package Top	ψJT		Thermal resistance between Junction and Package Top	-	0.21	-	℃/W

Note:

- This value is the result of thermal simulation and is a guaranteed design value. Shipping inspection will not be conducted.
- The board conditions are as follows.
  - Board Size : 114.3mm × 76.2mm × 1.6mm (JEDEC Board : Jesd51-7)
  - Number of layers : Multi-Layer (Cu 4 layer)
  - Cu layer thickness : 35μm (2/3 layer)、70μm (1/4 layer)
  - Cu layer area : 74.2 × 74.2 mm^2
  - Number of Cu VIA : 16 (4mm × 4mm)
  - Ambient temperature : 25℃ （No wind）

Application Circuit Example

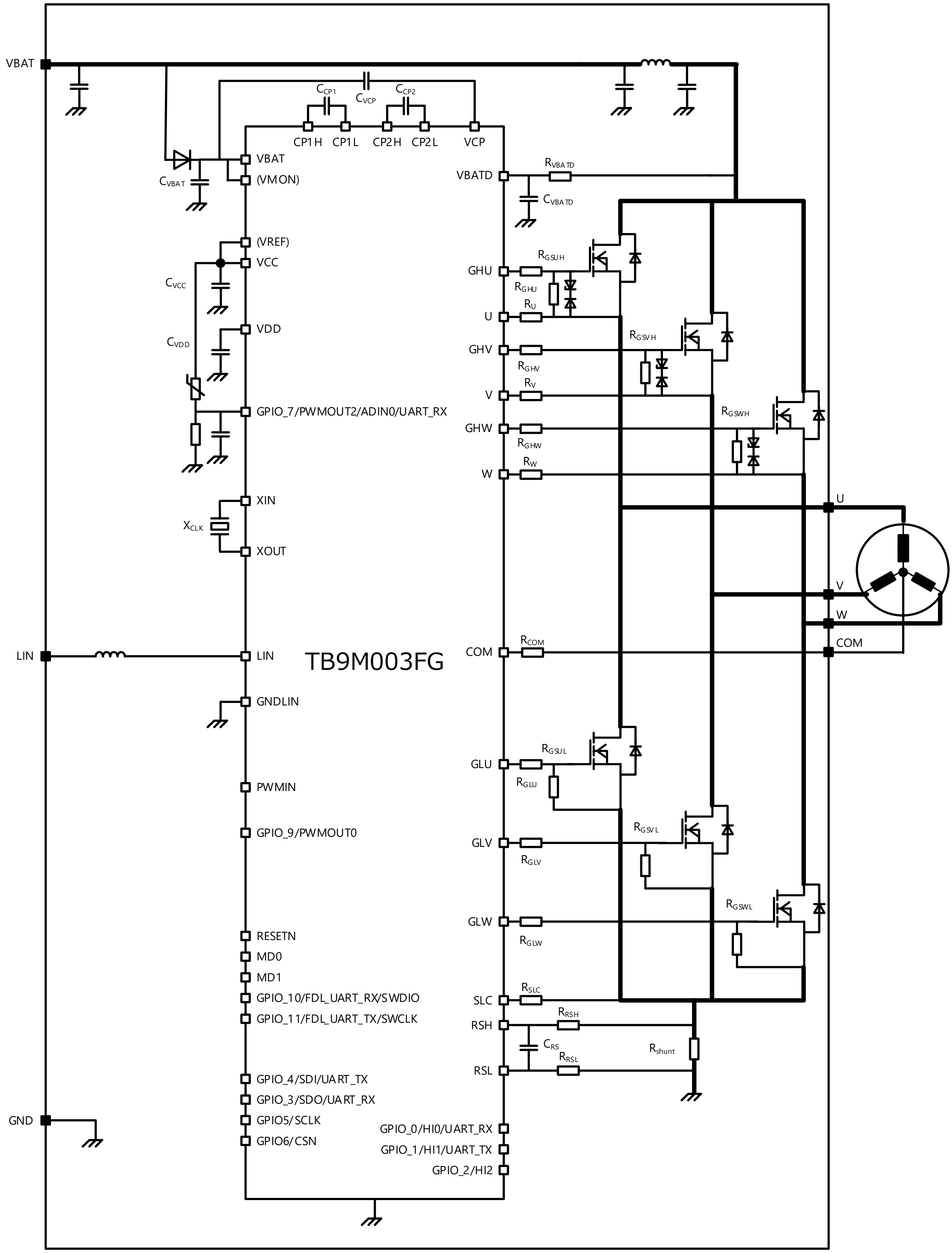
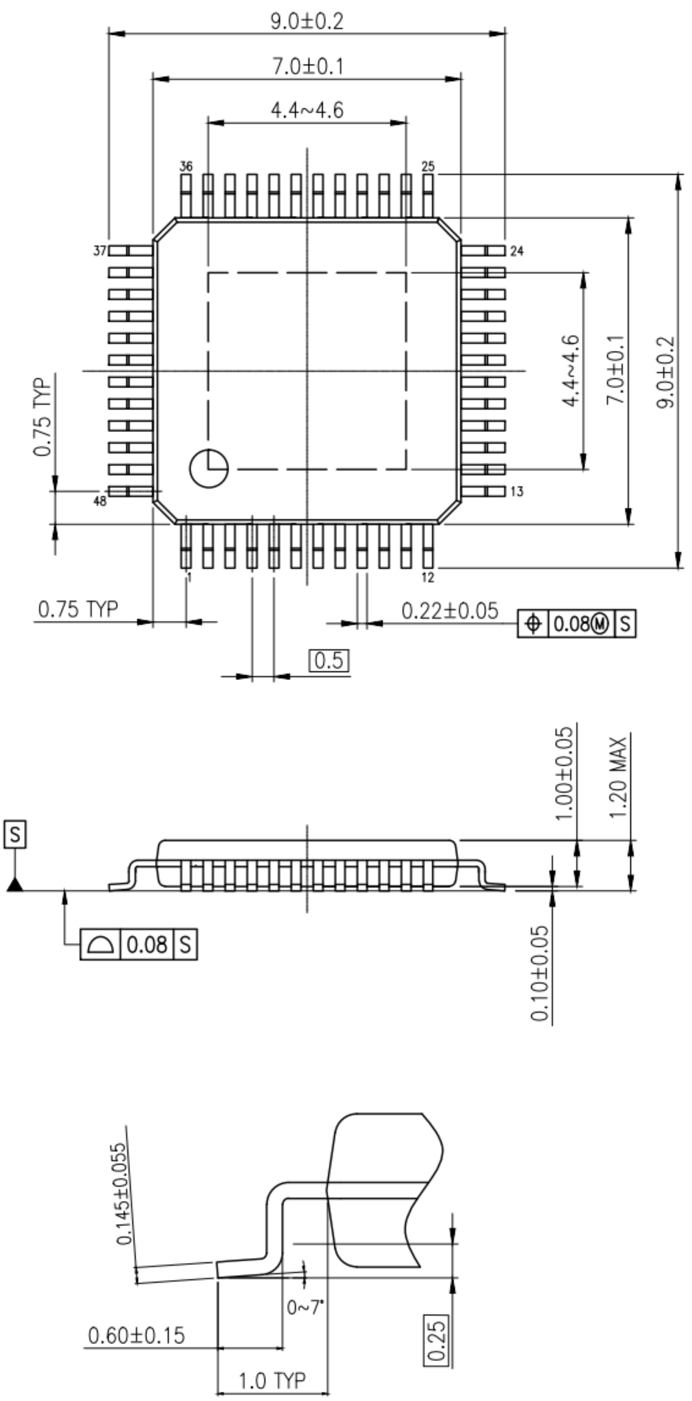


Figure 12.1 Application Circuit Example

13. Package Information

13.1. Package Dimensions

P-HTQFP48-0707-0.50-001 "Unit:mm"



Weight: 0.14 g

Figure 13.1 Package Dimensions

13.2. Marking

Product name：TB9M003FG

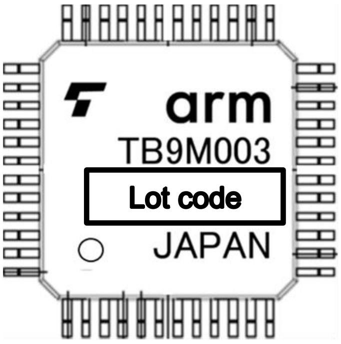
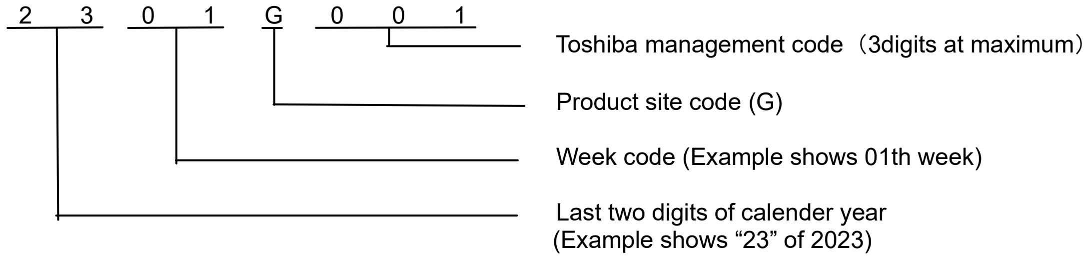


Figure 13.2 Marking

Example : Lot code



14. IC Usage Considerations

14.1. Notes on Handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure.

14.2. Points to Remember on Handling of ICs

(1) Over current Protection Circuit
Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.

(2) Thermal Shutdown Circuit
Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature clears the heat generation status immediately.

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