Isolated Gate Drive Circuit for 3-Phase Inverter

Design guide

RD238-DGUIDE-01

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1. Introduction

This Design Guide describes the design of the Isolated Gate Drive Circuit for 3-Phase Inverter (hereinafter referred to as "this Design").

3-phase inverters which is capable of converting power are indispensable for not only industrial inverters but also for renewable energy such as photovoltaic power generation, and will become increasingly important in the future.

This design allows isolated gate drive of power modules (such as IGBT modules) used in 3-phase inverter circuits.

It incorporates various protective functions and uses the smart gate driver coupler TLP5222 that does not require complicated external circuit, realizing a 7-channel (U-, V-, and W-phase high-side low-side and braking circuit) gate drive circuit on a small board. UVLO monitors and protects against the drop in gate-drive-voltage, overcurrent protection by detecting DESAT (non-saturation) and self-turn-on prevention by active miller clamp can be equipped to safely drive the power module.

It is also possible to adjust each component according to the actual circuit designs. Refer to this design guide, the datasheets of TLP5222 and other equipped components, and other related documents.

When this design is considered to use actual application, refer to the TLP5222 datasheet and design circuits to make operation conditions and environments meet applied safety standard.

Fig. 1 Photograph of the design

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2. Main components used

2.1. Smart Gate Driver Coupler TLP5222

This design uses a smart gate driver coupler TLP5222 with various built-in protective functions for the gate drive of the Power Module. The main features of TLP5222 are as follows.

- Peak output current: ± 2.5A (Max.)
- Operating temperature:-40 to 110°C
- Power supply voltage: 15 to 30V (recommended)
- Input-side power supply:-0.5 to 7V
- Output-side total power supply:-0.5 to 35V
- Threshold input current: 6.0mA (Max.)
- Supply current: 5mA (Max.)
- Propagation delay: 250ns (Max.)
- DESAT leading edge blanking time: 1.4μs (Typ.)
- DESAT mute time: 40μs (Max.)
- Common-mode transient immunity: ± 25kV/μs (Min.)
- Isolation voltage: 5000Vrms (Min.)
- Safety Standards

  UL approved : UL1577, File No. E67349

  cUL approved : CSA Component Acceptance Service No. 5A File No. E67349

  VDE approved : EN 60747-5-5, EN 62368-1 (Note 2.1)

  CQC approved : GB4943.1, GB8898 Japan Factory

  Note 2.1: When a VDE approved type is needed, please designate the Option (D4).

- Mechanical parameters: creepage and clearance distances 8mm (Min.)

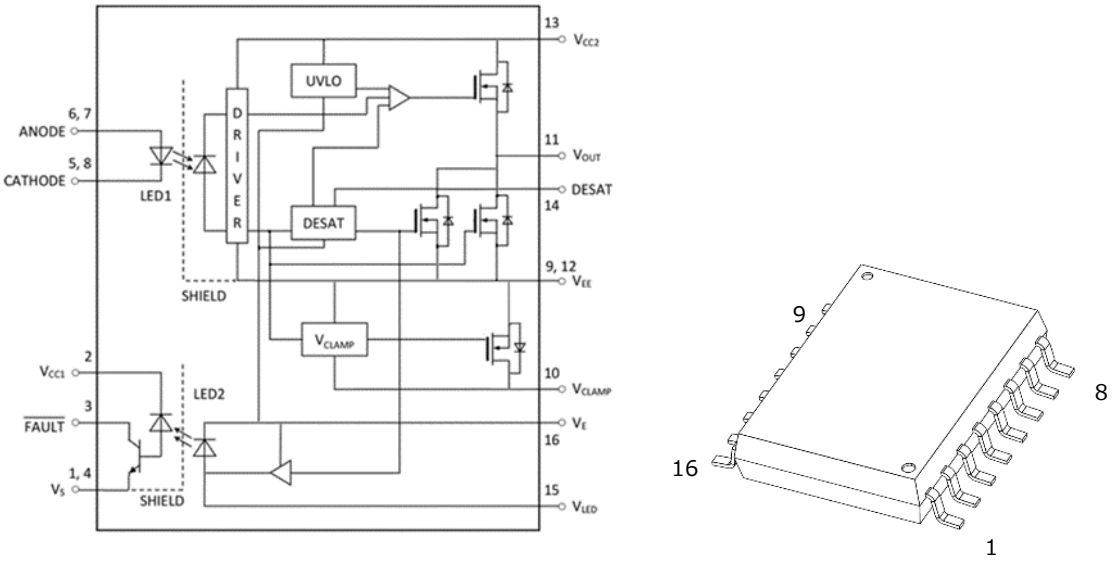

Fig. 2.1 TLP5222 Internal Circuit Configuration and Package (SO16L)

2.2. Small signal MOSFET SSM3K15AFS

This design uses the N-ch MOSFET SSM3K15AFS to drive TLP5222. The main features of SSM3K15AFS are as follows.

- 2.5V drive
- Low on-resistance:
  $R_{DS(ON)}$ = 3.6Ω (Max.) (@V_{GS} = 4V)
  $R_{DS(ON)}$ = 6.0Ω (Max.) (@V_{GS} = 2.5V)

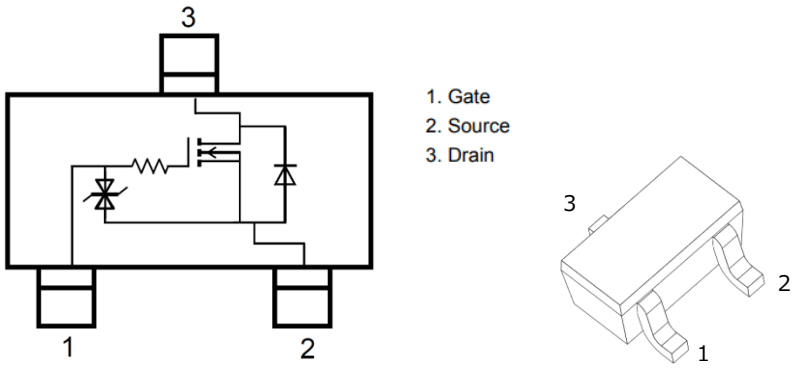

Fig. 2.2 SSM3K15AFS Internal Circuit Configuration and Package (SOT-416)

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3. Outline of Isolated Gate Drive Circuit for 3-Phase Inverter

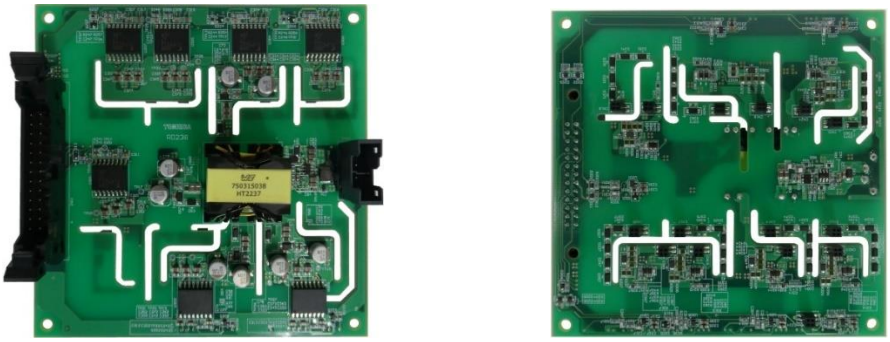
This design is a gate driver that can drive power modules for 3-phase inverters. This design is equipped with a gate drive circuit using the smart gate driver coupler TLP5222, the isolated power supply, and the protective circuits.

3.1. Features

- Single power entry (DC24V)
- Short-circuit proof (DESAT detecting method)
- Gate-drive voltage-protection (UVLO)
- Active miller clamp (AMC)
- Output on/off control
- Fault detection output and automated reset of protection operation
- Temperature monitor output

3.2. External View of Gate Driver Board and Example of Power Module Connection

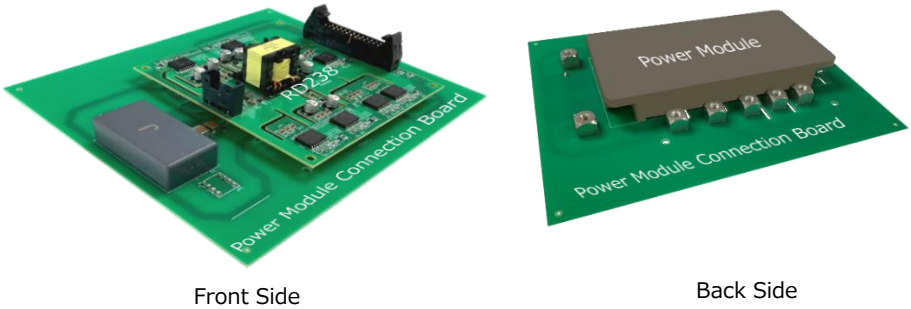
Fig. 3.1 is an external view of this design.



Front Side　　Back Side

Fig. 3.1 External View

Fig. 3.2 shows the configuration of this design and the power module.
Connect the design to the power module connection board (Front Side image in Fig. 3.2) and the power module to the power module connection board (Back Side image in Fig. 3.2). Prepare a separate BOARD for the power module so that the power module pins can be connected to the connector of this design according to Table 3.3.



Front Side　　Back Side

Fig. 3.2 Power Module Connection Board Example

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3.3. Pin Description

This section describes specifications of pin for each connector.

Table3.1 shows the description of the control power supply connector (CN10).

Table 3.1 Control Power Supply Connector (CN10)

Pin#	Signal name	Description	Pin#	Signal name	Description
1	VDD	Power supply voltage for control	2	GND	GND

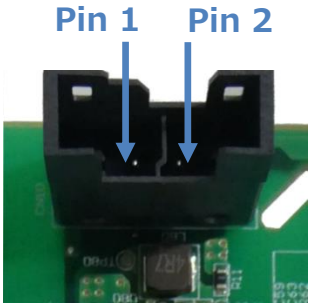

Fig. 3.3 Control Power Supply Connector

Table3.2 shows the description of the input/output signal connector (CN11).

Table 3.2 Input/Output Signal Connector (CN11)

Pin #	Signal name	I/O	Description	Pin#	Signal name	I/O	Description
1	IN_HU	I	U-phase high side PWM signal input	2	GND	-	GND
3	IN_HV	I	V-phase high side PWM signal input	4			
5	IN_HW	I	W-phase high side PWM signal input	6			
7	IN_LU	I	U-phase low side PWM signal input	8			
9	IN_LV	I	V-phase low side PWM signal input	10			
11	IN_LW	I	W-phase low-side PWM signal input	12			
13	EN	I	Enable signal input	14			
15	FAULT	O	Fault Detection Output (pull-up resistor collector output)	16			
17	IN_BR	I	Gate signal input for brake	18			
19	TH1	-	Temperature detection terminal 1	20			
21	TH2	-	Temperature detection terminal 2	22			
23	(5V)	-	Terminal for applying external power 5V (Optional)	24			
25				26			

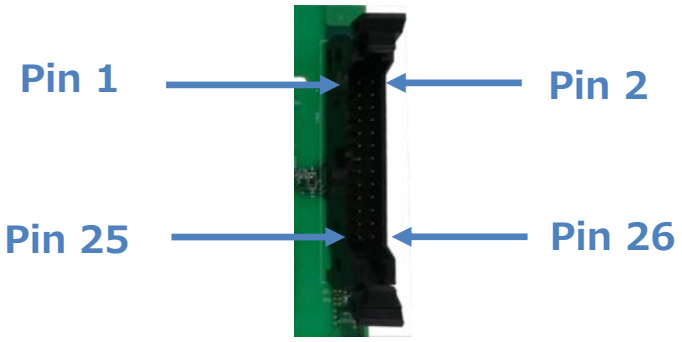

Fig. 3.4 Input/Output Signal Connector

Table 3.3 shows the description of the power module connectors.

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Table 3.3 Power Module Connectors

	Pin#	Description
CN21	1,2,3,4	W-phase high-side collector
CN24	1,3	W-phase high-side gate
	2,4	W-phase high-side emitter
CN18	1,3	V-phase high-side gate
	2,4	V-phase high-side emitter
CN20	1,2,3,4	V-phase high-side collector
CN16	1,3	U-phase high-side gate
	2,4	U-phase high-side emitter
CN13	1,2,3,4	U-phase high side collector

	Pin#	Description
CN22	1,2,3,4	W-phase low-side collector
CN23	1,3	W-phase low-side gate
	2,4	W-phase low-side emitter
CN12	1,3	Temperature detection 1
	2,4	Temperature detection 2
CN15	1,3	U-phase low-side gate
	2,4	U-phase low-side emitter
CN14	1,2,3,4	U-phase low-side collector
CN19	1,3	V-phase low-side gate
	2,4	V-phase low-side emitter
CN17	1,2,3,4	V-phase low-side collector
CN26	1,3	Brake gate
	2,4	Brake emitter
CN25	1,2,3,4	Brake collector

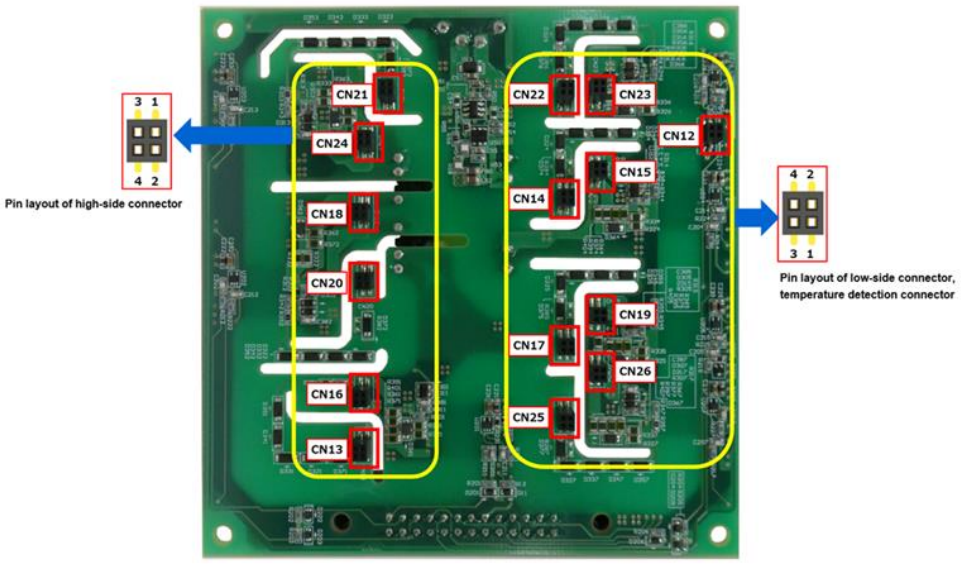

Fig. 3.5 Power Module Connectors

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3.4. Specifications

Table 3.4 lists the recommended operating ranges of the gate driver for the power module for the 3-phase inverter, and Table 3.5 lists the electrical characteristics of the gate drive output voltage and protection functions.

Table 3.4 Recommended Operating Range

Item			Min.	Typ.	Max.	Unit
Power supply voltage for control	V_{DD}		20.0	24	28.0	V
Input signal (gate control signal, enable signal)	INPUT	H Level	4.0	—	5.0	V
		L Level	0	—	1.8	
Switching Frequency Note 3.1	f_{sw}		—	—	20	kHz

Note 3.1: Please set within the rated temperature of each component in actual use conditions.

Table 3.5 Electrical Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Gate drive output H level voltage	V_{CC2_HU}	—	14.4	16	17.6	V
Gate drive output L level voltage	V_{EE_HU}	—	-10	-8	-6	V
UVLO_threshold (V_{CC2_HU}-V_{E_HU})	V_{UVLO-_HU}	Protection operation voltage	9.2	10.0	11.1	V
	V_{UVLO+_HU}	Protection release voltage	10.5	11.4	12.5	
Gate drive H level peak current	I_{OPH_HU}	—	—	—	2.5	A
Gate drive L level peak current	I_{OPL_HU}	—	-2.5	—	—	A

Table 3.5 shows the electrical characteristics of the U-phase high side. 'HU' in the symbol indicates the U-phase high side. V-phase/W-phase high-side, U-phase/V-phase/W-phase low-side and brake circuit are also the same as U-phase high-side.

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4. Circuit Design

4.1. Overall Block Diagram

Fig. 4.1 shows the block diagram of this design. Smart gate driver coupler TLP5222 and isolated DC-DC converter are equipped. This design has seven gate outputs for the high-side, low-side and brake circuits of the U-, V-, and W-phases.

It operates according to the control power supply from VDD.

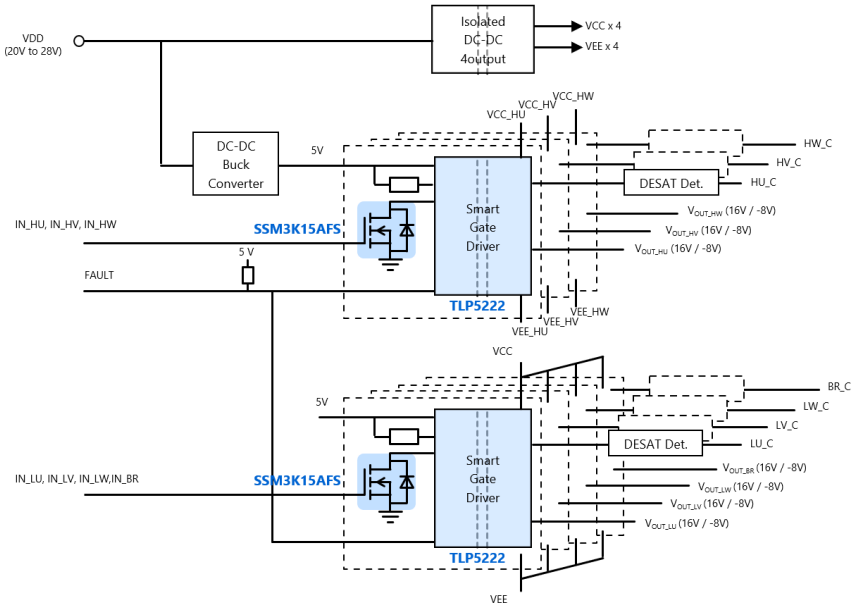

Fig. 4.1 Block Diagram of Isolated Gate Drive Circuit for 3-Phase Inverter

4.2. Internal 5V Power Supply

Fig. 4.2 shows the internal 5V power supply circuit. The control power V_{DD} is supplied to the control IC (U80) for 5V power supply. LMR51430XDDCR (made by Texas Instruments) is used for the control IC. The output 5V of the internal 5V power supply circuit is supplied to the input-side power supply terminal V_{CC1} and gate-control-signal input circuit of TLP5222 (U301 to U307).

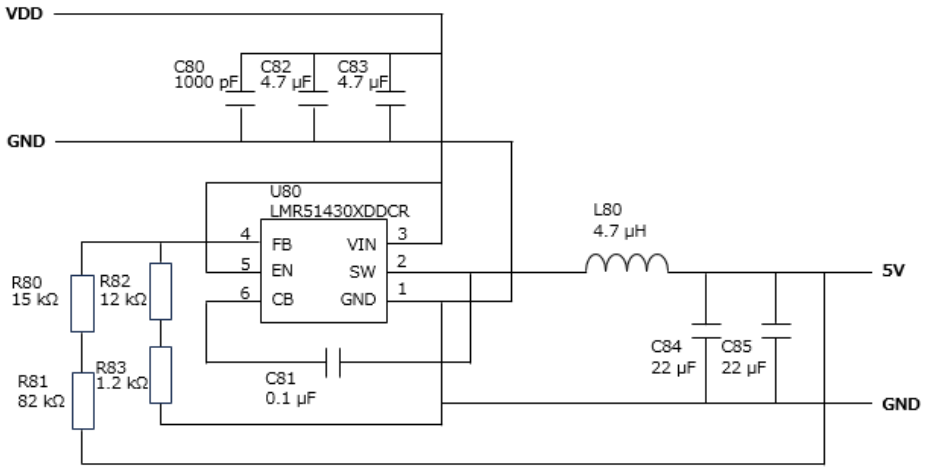

Fig. 4.2 Internal 5V Power Supply

4.3. Gate Control Signal Input Circuit (TLP5222 Primary Side)

Fig. 4.3 shows the gate control signal input circuit of TLP5222 on the U-phase high side.

V-phase/W-phase high-side, U-phase/V-phase/W-phase low-side and brake circuit are also the same as U-phase high-side. However, EN controls the active/inactive state of this design with one input (Pin13 of CN11).

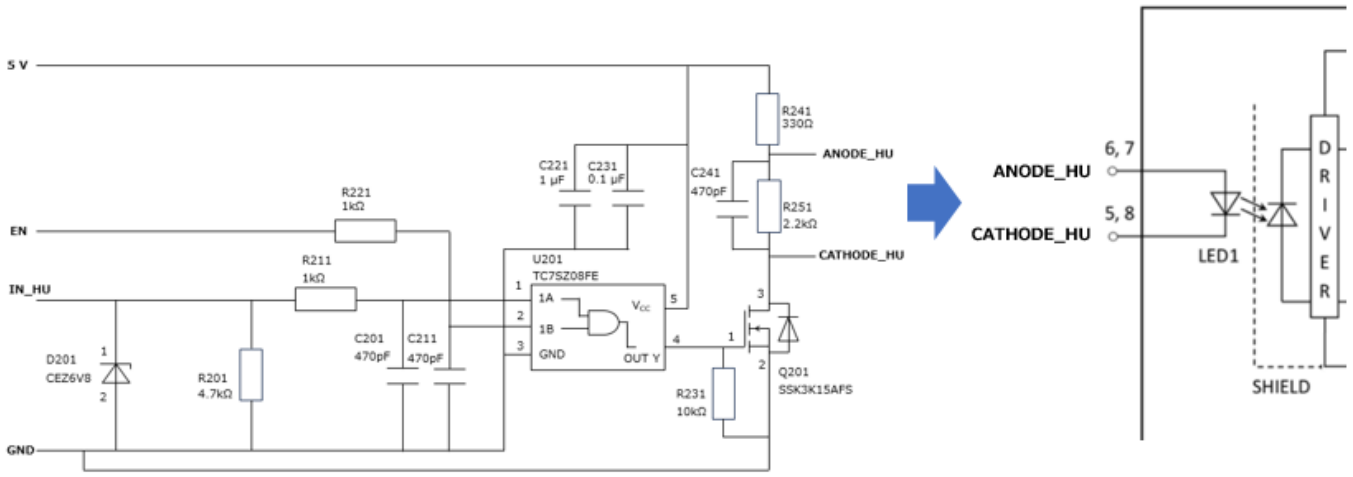

Fig. 4.3 Gate Control Signal Input Circuit

4.3.1. Gate Control Signal Input

There are U-phase high-side gate control signal input, IN_HU (input signal), and EN (enable). EN can control enable/disable of gate drive output. When enabled, EN signal is High and when disabled EN is Low. When EN is open, it is enabled because it is pulled up by the internal circuit. The IN_HU and EN are input to TC7SZ08FE (AND circuit), and the OUTPUT Y is input to the gates of MOSFET Q_{201}. When both IN_HU and EN are H (output Y is H), an input on-current $I_{F(ON)}$ flows between ANODE_HU (of LED1) and CATHODE_HU (of LED1) of the U-phase high-side TLP5222 after MOSFET Q_{201} is turned on. This $I_{F(ON)}$ turns on the U-phase high-side power module. When Y is Low, there is no I_F between ANODE_HU and CATHODE_HU, so the power module is disabled.

The I_F (LED incoming forward current) between the anode and cathode on the primary side of the TLP5222 is expressed by the following equation:

$$I_F = \frac{V_{DD} - V_F}{R241} - \frac{V_F}{R251} \qquad (4-1)$$

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I_F of TLP5222 is set between 9mA and 10mA the current flowing through R241. R241 is connected to 5V power supply, and the current flowing to R251 is 1mA. The LED incoming forward voltage V_F between the anode and cathode on the primary side of the TLP5222 is calculated as 1.67V (Typ.). R241 and R251 are determined by the following equations.

$$R241 = \frac{V_{DD} - V_F}{10mA} = \frac{5 - 1.67}{10mA} \fallingdotseq 333\Omega$$

$$R251 = \frac{V_F}{1\ mA} = \frac{1.67}{1mA} \fallingdotseq 1670\Omega$$

In the actual circuit, R241 of 330Ω and R251 of 2200Ω are selected to be close to the values calculated above.

In this situation, according to equation (4-1), I_F is 9.33mA.

$$I_F = \frac{5 - 1.67}{330} - \frac{1.67}{2200} = 9.33mA$$

Table 4.1 shows the truth values.

Table 4.1 Truth Table

IN_HU (CN11:Pin1)	EN (CN1:Pin13)	U-phase high side Power module
L	L	OFF
H	L	OFF
H	H	ON
L	H	OFF

Since a pull-up resistor is connected to EN pin in this design, this pin is active when no EN is input. In order to be inactive by EN, a low-level input is required.

4.3.2. Error Detection Output

In this design, FAULT pin (Pin15 of CN11) is set to L-level when one of the seven channels of the power module activates DESAT detect. Each of the seven faults is detected by a wired OR and outputted to FAULT pin (Pin15 of CN11). During UVLO operation, gate output voltage pin (VOUT) goes to the VEE voltage, but FAULT pin does is not set go to the L level. FAULT pin returns from L level to H level due to the automated reset of protection operation.

Refer to the TLP5222 datasheet and the application note for the smart gate driver coupler - Advanced edition.

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4.4. Gate Drive Power Supply Circuit

Fig. 4.4 shows the power supply circuit for gate drive. The gate-drive power supply is a 4-output isolated DC-DC converter. The DC-DC converter has 3 outputs for high side of the U-phase, V-phase, and W-phase, because the emitter voltage of each phase high-side swings independently from GND to the collector voltage of the power module.

The emitters on each phase's low-side are of a single-output configuration, as they share the same GND.

In this section, the output voltage of the U-phase high side is calculated. Calculations for the V-phase high-side, W-phase high-side, and each phase low-side are also the same as for the U-phase high-side.

In this design, the isolated DC-DC converter is a flyback converter method that converts the power supply V_{DD} for control into a voltage 24V between V_{CC2_HU}-V_{EE_HU}. Between V_{CC2_HU}-V_{EE_HU}, the Zener Diode (D56) of the Zener Voltage 16V and Resistor (R75) are connected in series. The turn-on gate drive output voltage is generated by the Zener voltage 16V (V_{CC2_HU}-V_{E_HU}) and the turn-off gate drive output voltage is generated by the voltage-8V (V_{EE_HU}-V_{E_HU}) across R75.

These gate drive output voltages are set in consideration of the rated gate voltage and gate switching characteristics of the power module.

To change the positive voltage, adjust the Zener voltage.

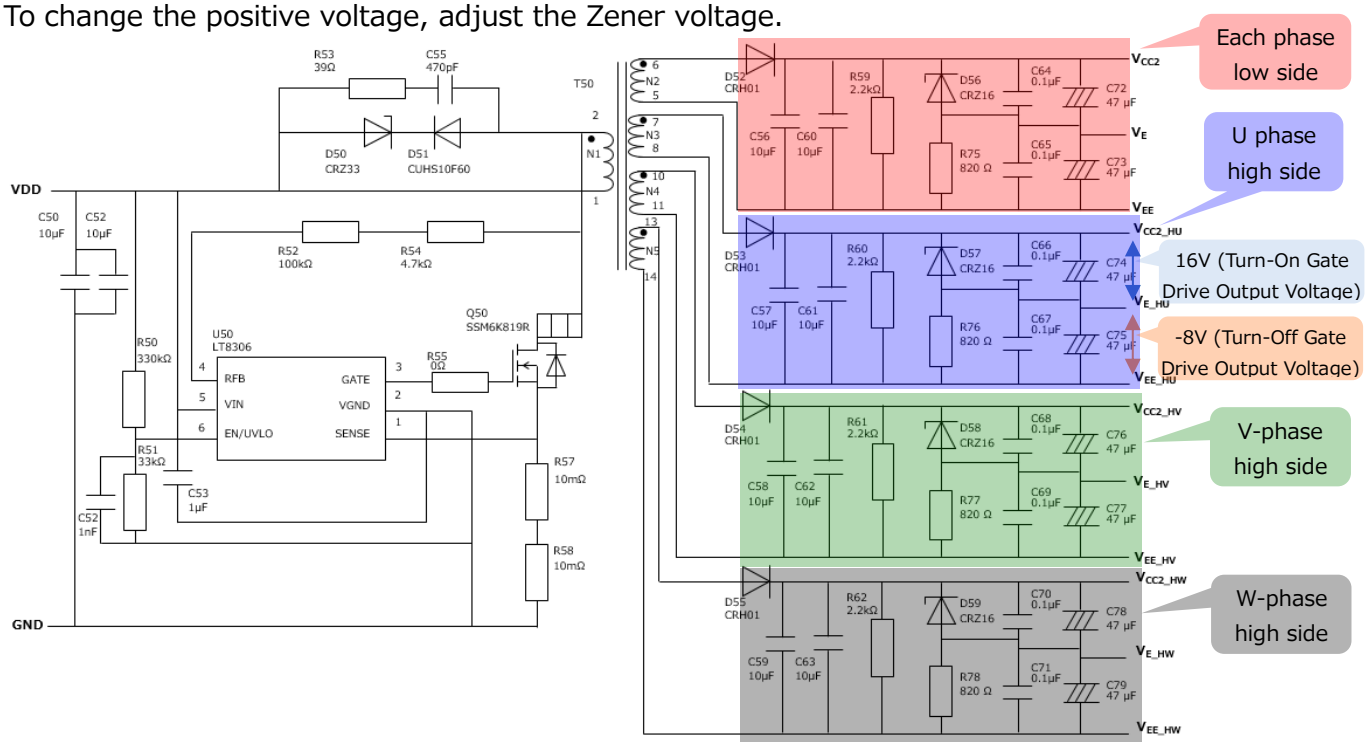

Fig. 4.4 Gate Drive Power Supply Circuit

LT8306 (made by Analog Devices) is used for the control IC of the flyback converter. The voltage between V_{CC2_HU}-V_{EE_HU} can be expressed as equation (4-2) using the external resistor (R52, R54) and the transformer turns ratio (N_{PS1}).

$$V_{CC2\_HU} - V_{EE\_HU} = I_{RFB} \times \left(\frac{R52 + R54}{N_{PS1}}\right) - V_F \quad (4-2)$$

From equation (4-2), (R52+R54) can be expressed by equation (4-3).

$$R52 + R54 = \left(\frac{N_{PS1}}{I_{RFB}}\right) \times \{ (V_{CC2\_HU} - V_{EE\_HU}) + V_F \} \quad (4-3)$$

In this design, R52, R54 are set under the following conditions.

N_{PS1} = 0.429 (T50 turns ratio)
I_{RFB} = 100μA (U50 internal reference current)
V_F = 0.4V (D53 forward voltage)
V_{CC2_HU}-V_{EE_HU} = 24V

If the measured output voltage $V_{CC2\_TOP\_U}$-$V_{EE\_TOP\_U\ (MEAS)}$ of the actual resistance value (R52, R54) is incorrect with respect to the target output voltage V_{CC2_HU}-V_{EE_HU}, readjust it to the final resistance value (R52 (FINAL) and R54 (FINAL)) using the following formula.

$$R_{52(FINAL)} + R_{54(FINAL)} = \frac{V_{CC2\_HU} - V_{EE\_HU}}{V_{CC2\_HU} - V_{EE\_HU\ \ (MEAS)}} \times (R_{52} + R_{54})$$

In this design, R52 = 100kΩ and R54 = 4.7kΩ are readjusted.

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4.5. Gate Drive Circuit (TLP5222 Secondary Side)

Fig. 4.5 shows the gate-drive circuit of the U-phase high side (NM stands for Not Mounted, and it is not installed). V-phase/W-phase high-side, U-phase/V-phase/W-phase low-side and brake circuit are also the same as U-phase high-side.

The gate drive circuit consists of a gate resistor for adjusting the turn-on and turn-off and a circuit for detecting DESAT.

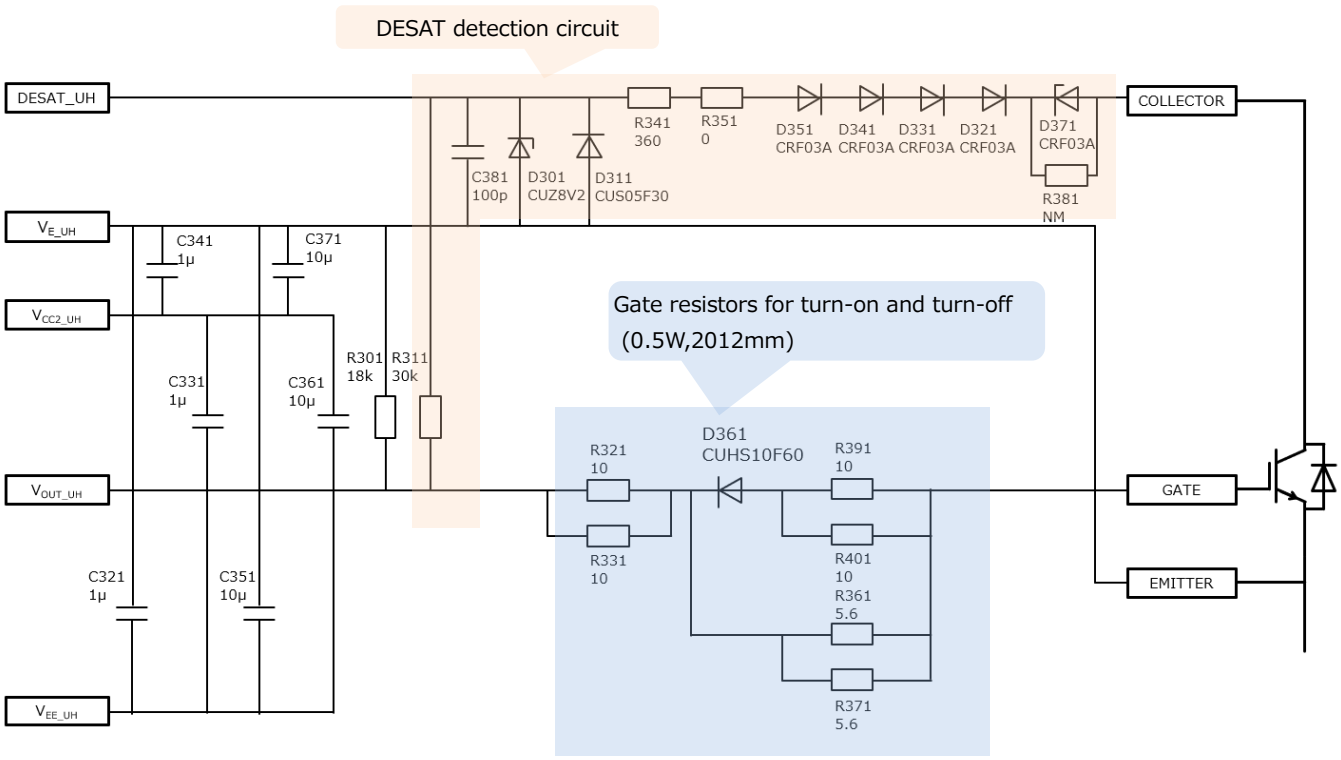

Fig. 4.5 Gate Drive Circuit

4.5.1. Gate Resistance

Fig. 4.6 shows the gate resistance configuration at turn-on. When the gate-control signal applied to HU (Pin 1 of CN11) goes to the H level, V_{OUT_HU} signal goes to the H level. The power module gate is charged via the resistance path shown in Fig. 4.6 to turn on the power module.

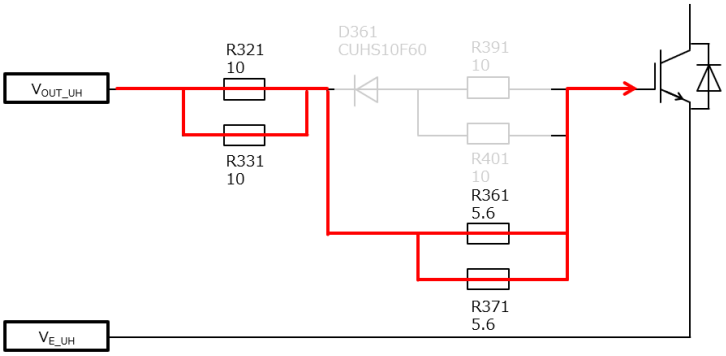

Fig. 4.6 Gate Resistance Configuration at Turn-On

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The gate-resistor $R_{G(ON)}$ at turn-on can be expressed by equation (4-4).

$$R_{G(ON)} = \frac{R_{321} \times R_{331}}{R_{321} + R_{331}} + \frac{R_{361} \times R_{371}}{R_{361} + R_{371}} \quad (4-4)$$

The gate drive H-level peak current I_{OPH} at turn-on is calculated by equation (4-5).

$$I_{OPH} = \frac{|V_{GS}|}{r_{ig} + R_{G(ON)}} \quad (4-5)$$

For I_{OPH} < 2.5A from Table 3.5, equation (4-4) can be transformed, and $R_{G(ON)}$ can be expressed as equation (4-6).

$$R_{G(ON)} > \frac{|V_{GS}|}{2.5A} - r_{ig} \quad (4-6)$$

In this design, $R_{G(ON)}$ is adjusted according to the following conditions.

$|V_{GS}|$ = | V_{CC2_HU} − V_{EE_HU}| = | 16V − (-8V)| = 24V
r_{ig} = 3.75Ω (Power Module internal-gate resistor)

From equation (4-6),

$$R_{G(ON)} > \frac{24V}{2.5A} - 3.75\Omega = 5.85\Omega$$

R321 = R331 = 10Ω, R361 = R371 = 5.6Ω is selected, and $R_{G(ON)}$ is adjusted to 7.8Ω according to the equation (4-4).
I_{OPH} is I_{OPH} = 2.08A (< 2.5A) from equation (4-5).

Fig. 4.7 shows the gate resistance configuration at turn-off. When the gate-control signal applied to HU (Pin 1 of CN11) goes to the L level, V_{OUT_HU} signal goes to the L level. The power module gate is discharged via the resistor configuration shown in Fig. 4.7 to turn off the power module.

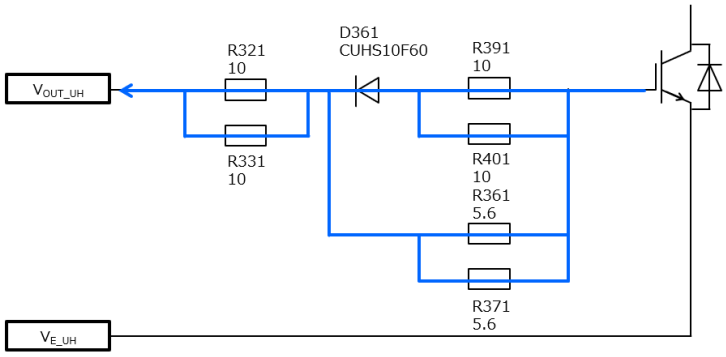

Fig. 4.7 Gate Resistance Configuration at Turn-Off

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The gate-resistance $R_{G(OFF)}$ at turn-off can be expressed by equation (4-7).

$$R_{G(OFF)} = \frac{R_{321} \times R_{331}}{R_{321} + R_{331}} + \frac{R_{361} \times R_{371} \times R_{391} \times R_{401}}{R_{361} \times R_{371} \times R_{391} + R_{371} \times R_{391} \times R_{401} + R_{391} \times R_{401} \times R_{361} + R_{401} \times R_{361} \times R_{371}} (4-7)$$

The gate drive L-level peak current I_{OPL} at turn-off is calculated by equation (4-8).

$$I_{OPL} = \frac{|V_{GS}|}{r_{ig} + R_{G(OFF)}} \quad (4-8)$$

I_{OPL} < |-2.5A| from Table3.5. To do so, we can transform equation (4-8) and express $R_{G(OFF)}$ using equation (4-9).

$$R_{G(OFF)} > \frac{|V_{GS}|}{|-2.5A|} - r_{ig} \quad (4-9)$$

In this design, $R_{G(OFF)}$ is adjusted according to the following conditions.

$|V_{GS}|$ = | $V_{EE\_TOP\_U}$ − $V_{CC2\_TOP\_U}$| = | (-8V) − 16V| = 24V
ri_g = 3.75Ω (Power Module internal-gate resistor)

From equation (4-9),

$$R_{G(OFF)} > \frac{24V}{2.5A} - 3.75\Omega = 5.85\Omega$$

R321 = R331 = R391 = R401 = 10Ω and R361 = R371 = 5.6Ω are selected, and $R_{G(OFF)}$ is adjusted to 6.8 Ω according to equation (4-7).
I_{OPL} is I_{OPL} = 2.27A (< 2.5A) according to equation (4-8).

In this design, gate-driven peak-current I_{OPH} < 2.5A (I_{OPL} < |-2.5A|). To do so, adjust $R_{G(ON)}$ and $R_{G(OFF)}$ to match the internal gate resistor of the power module actually used.

Generally, increasing RG(ON) results in a longer turn-on fall time for the collector-emitter voltage (VCE). Additionally, the DESAT detection for the short-circuit protection function, which will be described later, sets the threshold voltage (VDESAT) at VCE saturation plus a few volts. During turn-on, if the time for VCE to fall below VDESAT ($t_{on\_VCE\_DESAT}$) exceeds the sum of the DESAT leading edge blanking time of TLP5222(t_{desat_LEB}) and the DESAT capacitor charging time (t_{BLANK}) , DESAT detection will occur, causing the power module to soft shut down and fail to turn on properly.

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Adjust $R_{G(ON)}$ so that the tON_VCE_DESAT is shorter than the tDESAT_TOTAL.(Refer to Fig. 4.8)

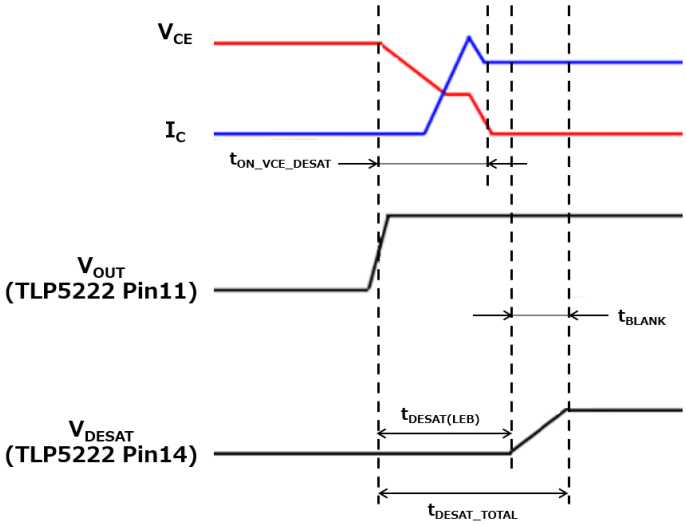

Fig. 4.8 Timing Chart at Turn-on

Since the gate resistance loss affects heat generation, use it within the rating by referring to the loss calculation below.

Gate Resistance Loss P_$R_{G(ON)}$ at turn-on and Gate Resistance Loss P_$R_{G(OFF)}$ at turn-off can be calculated by the following equation.

$$P\_R_{G(ON)} = \frac{R_{G(ON)}}{r_{ig} + R_{G(ON)}} \times P_{GATE(ON)} \quad (4-10)$$

$$P\_R_{G(OFF)} = \frac{R_{G(OFF)}}{r_{ig} + R_{G(OFF)}} \times P_{GATE(ON)} \quad (4-11)$$

Turn-on charging energy (PGATE_ON) can be calculated from the gate voltage VGS, the gate drive frequency f_{SW}, and the gate charge Qg of the power module.

$$P_{GATE(ON)} = \frac{1}{2} \times V_{GS} \times Q_g \times f_{SW} \quad (4-12)$$

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If expression (4-12) is assigned to expression (4-10), (4-11), then P_$R_{G(ON)}$ and P_$R_{G(OFF)}$ are as follows.

$$P\_R_{G(ON)} = \frac{R_{G(ON)}}{r_{ig} + R_{G(ON)}} \times \frac{1}{2} \times V_{GS} \times Q_g \times f_{SW} \quad (4-13)$$

$$P\_R_{G(OFF)} = \frac{R_{G(OFF)}}{r_{ig} + R_{G(OFF)}} \times \frac{1}{2} \times V_{GS} \times Q_g \times f_{SW} \quad (4-14)$$

As the loss of gate resistor is affected by r_{ig}・Q_g of power module used, use it within the rated value according to the actual specification.

Table 4.2 shows the gate resistance loss per wire calculated under the following conditions. The gate resistance loss per cycle is set within the rated 0.5W of the used resistance.

Gate voltage V_{GS} = 24V
Gated charge Q_g = 900nC of the Power Module
Internal gate-resistance of the power module r_{ig} = 3.75Ω
Gate-drive frequency f_{SW} = 20kHz

Table 4.2 Gate Resistance Loss

R#	Resistance value [Ω]	P_$R_{G(ON)}$ [W]	P_$R_{G(OFF)}$ [W]	Cycle by cycle [W]	Used resistor rating [W]
R321	10	0.069	0.079	0.148	0.5 (2012mm)
R331	10				
R361	5.6	0.025	0.010	0.035	
R371	5.6				
R391	10	-	0.018	0.018	
R401	10				

When adjusting the gate resistor according to the actual specifications, consider the heat generation, switching loss, V_{CE} surge voltage, etc. of the respective components. Refer to the data sheet and the related documentation of the power module, etc. to be used to select the gate resistance value.

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4.6. Protection Circuit

This section explains the protection circuit of the U-phase high side. V-phase/W-phase high-side, U-phase/V-phase/W-phase low-side and brake circuit are also the same as U-phase high-side.

4.6.1. DESAT (Desaturate) Detection Operation

DESAT detection function monitors the collector-emitter voltage (V_{CE}) of the power module that is turned on at the DESAT_HU pin, and protects the power module from being damaged by overcurrent.

If an overcurrent flows into the collector current (I_C) of the power module, the Collector Current (I_c) and the Collector-Emitter Voltage (V_{CE}) static curve will also raise V_{CE} along with I_C.

When V_{CE} is monitored by the DESAT_HU pin and DESAT threshold voltage of TLP5222 (V_{DESAT}) = 6.6V (typical) is exceeded, the operation of the power module is stopped and FAULT pin output of CN11 goes from H to L.

DESAT detection method is not precise because the collector current (I_C) cannot be directly monitored, but it is used for emergency-shutdown when a large current occurs because of its fairly simple configuration.

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Fig. 4.9 shows a current loop that monitors DESAT.

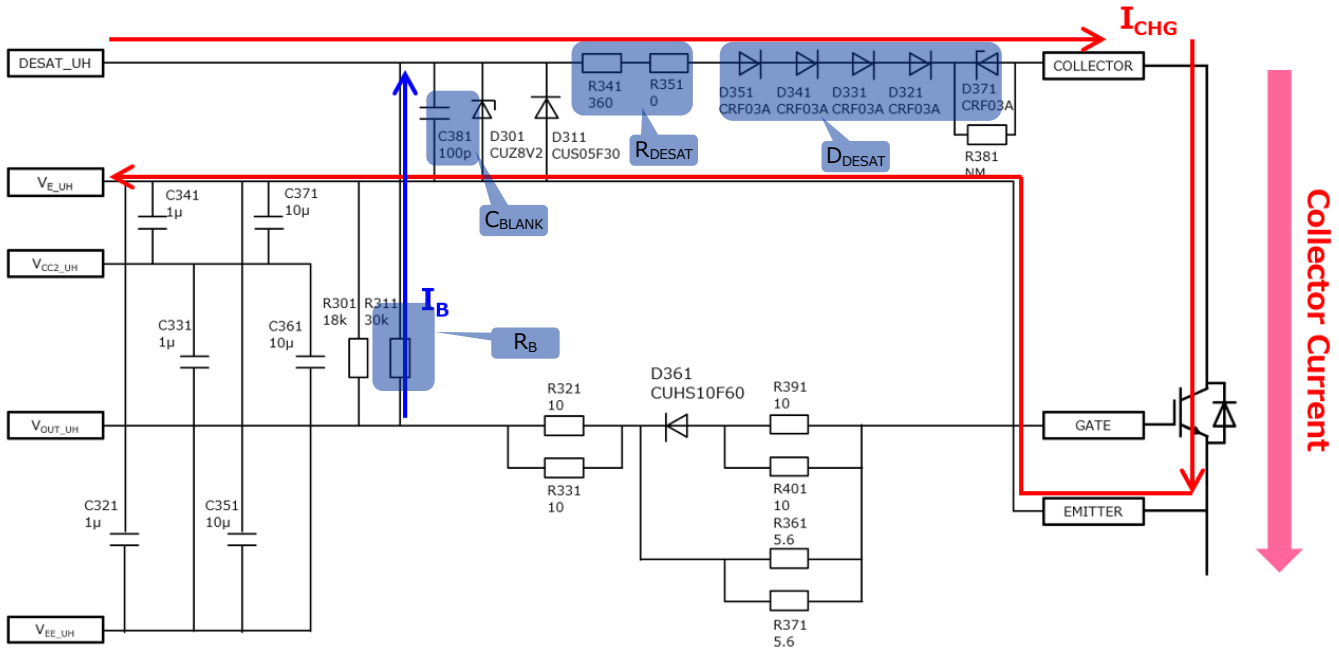

Fig. 4.9 DESAT Detection Operation

When the power module is on, the DESAT_HU pin outputs a blanking capacitance charge current I_{CHG} of approximately 0.26mA as a constant current source. A complementary current I_B flows through the resistor (R311) between V_{OUT_HU} pin and the DESAT_HU pin. This I_{CHG} and I_B charge the blanking capacitance C_{BLANK} (C381) connected to the DESAT_HU and V_{E_HU} pins. The voltage generated by C_{BLANK} is equal to the voltage dropped when I_{CHG} and I_B flow to the collector-emitter V_{CE} of the power module through the resistor R_{DESAT} (R341,R351), the high-voltage Diode D_{DESAT} (D321,D331,D341,D351), and the Zener Diode D_Z (D371).

The voltage between voltage DESAT_HU-V_{E_HU} at that time (VDESAT_HU(ON)) is expressed by the following equation.

$$V_{DESAT\_UH(ON)} = V_{CE} + VF(D_{DESAT}) + V_Z(D371) + (I_{CHG} + I_B) \times R_{DESAT}$$

$$V_{DESAT\_UH(ON)} = V_{CE} + VF(D321 + D331 + D341 + D351) + V_Z(D371) + (I_{CHG} + I_B) \times (R341 + R351)$$

I_B is the value obtained by dividing the voltage at both ends of R311 by R311, and can be expressed by the following formula.

$$I_B = \frac{V_{OUT\_UH} - V_{DESAT\_UH(ON)}}{R_{311}}$$

Since the power module is on, I_{CHG} is superimposed on the collector current I_C of tens of ampere., which flows between the collector and emitter.

For this reason, the above V_{CE} is a voltage generated according to I_C – V_{CE} static curve of the power module, and the voltage drop of the small current I_{CHG} is included in the voltage drop of I_C and is not visible.

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V_{CE} of the normally-on power module is voltage according to I_C, but V_{CE} increases when an overcurrent occurs. If the VDESAT_HU (ON) exceeds V_{DESAT} due to an increase in V_{CE}, it is judged to be an abnormal condition and a soft shutdown is initiated to protect the power module.
The condition for detecting DESAT is as follows because VDESAT_HU (ON) is equal to V_{DESAT}.

$$V_{DESAT} = V_{DESAT_{UH(ON)}} = V_{CE} + V_F(D321 + D331 + D341 + D351) + V_Z(D371) + (I_{CHG} + I_B) \times (R341 + R351) \quad (4-15)$$

If you transform equation (4-15) and assign an I_B, (R341+R351) can be expressed as equation (4-16).

$$R341 + R351 = \frac{(V_{DESAT} - V_F(D321 + D331 + D341 + D351) - V_Z(D371) - V_{CE})}{I_{CHG} + \frac{V_{OUT\_UH} - V_{DESAT}}{R_{311}}} \quad (4-16)$$

V_{CE} when DESAT is detected is determined from the collector-emitter voltage (V_{CE})-collector current (I_C) property of the power module.

In this design, to minimize set the Vce value for DESAT detection (R341+R351) is adjusted under the following conditions.

Power Module Collector-Emitter Voltage (V_{CE}) when DESAT is detected: 2.0V
DESAT Threshold Voltage V_{DESAT}: 6.0V (TLP5222 minimum value)
Blanking Capacitance Charge Current I_{CHG}: 0.33mA (TLP5222 maximum value)
High Voltage Diode D_{DESAT} (D321 to D351) Forward Voltage V_F: 1.96V
Zener Diode D_Z (D371) Voltage V_Z: 1.8V
V_{OUT_HU} terminal voltage (V_{OUT_HU}) : 16V (positive power supply voltage: V_{CC2_HU}-V_{E_HU})
Resistor (R311) between V_{OUT_HU} terminal and DESAT_HU pin: 30kΩ

R341+R351 from equation (4-15),

$$R341 + R351 = \frac{(6V - 1.96V - 1.8V - 2.0V)}{0.33mA + \frac{16V - 6V}{30k\Omega}} = 361.8\Omega$$

R341 = 360Ω and R351 = 0Ω are selected. V_{CE} of power modules is approximately 2.0V according to equation (4-15).

Perform a proper design according to the actual specifications and sufficiently check the operation on the actual machine.

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The DESAT_HU pin is connected to the collector terminal of the Power Module through high-voltage diodes (D_{DESAT}) and a Zener diode (D371). If the collector voltage of the power module fluctuates due to external noise while the power module is ON, the DESAT_HU voltage may fluctuate via the junction capacitance of D_{DESAT}. If the DESAT_HU voltage variation exceeds V_{DESAT}, the protective operation will be started, and the power module will be soft shutdown. The high-voltage inverter is noisy, so a blanking capacitor C_{BLANK_HU} (C381) is added to form a low-pass filter.
An additional trade-off for this C_{BLANK_HU} (C381) is t_{BLANK} of blanking times before VDESAT_HU (ON) reaches V_{DESAT}.

Increasing C_{BLANK_HU} for enhanced noise-immunity increases t_{BLANK}, but allows for a more flexible setting of blanking times by controlling the charge current to C_{BLANK_HU} by using a resistor R_B (R311) between V_{OUT_HU}-DESAT_HU.

Note that this design adds not only C_{BLANK_UH} but also the total capacitance (C_{t_D301} and C_{t_D311}) of the connected Diode D301 and D311, and those affect t_{BLANK}.

The blanking-time t_{BLANK} is given by the formula below.

$$t_{BLANK} = -(C_{BLANK} + C_{t\_D301} + C_{t\_D311}) \times R_B \times ln\left(1 - \frac{V_{DESAT}}{(V_{OUT} - V_E) + R_B \times I_{CHG}}\right)$$

$$t_{BLANK} = -(C318 + C_{t\_D301} + C_{t\_D311}) \times R311 \times ln\left(1 - \frac{V_{DESAT}}{(V_{OUT} - V_E) + R311 \times I_{CHG}}\right) \quad (4-17)$$

After the blanking-time t_{BLANK}, the power module performs a soft shutdown.

The time tDESAT_TOTAL from the occurrence of overcurrent to the soft shutdown is the sum of t_{BLANK} and $t_{DESAT(LEB)}$ (blanking time at DESAT rising edge of TLP5222).

$$t_{DESAT\_TOTAL} = t_{BLANK} + t_{DESAT(LEB)} \quad (4-18)$$

In this design, to maximize set the tblank value $t_{DESAT\_TOTAL\ (Max.)}$ is calculated using equation (4-18) under the following conditions:

Blanking capacitance C_{BLANK}: 100pF
D301 junction capacitance C_{t_D301}: 30pF
D311 junction capacitance C_{t_D311}: 120pF
Resistor R_B between V_{OUT_HU}-DESAT_HU: 30kΩ
DESAT Threshold V_{DESAT}: 7.5V (TLP5222 maximum value)
Blanking Capacitance Charge Current I_{CHG}: 0.13mA (TLP5222 minimum value)
V_{OUT_HU}-V_{E_HU} Voltage: 16V (Positive supply voltage: V_{CC2_HU}-V_{E_HU})
Blanking time at DESAT rising $t_{DESAT(LEB)}$: 1.4μs

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The maximum blanking-time tDESAT_TOTAL (Max.) is 4.95μs as shown in the following equation.

$$t_{DESAT\_TOTAL(MAX)} = -(100pF + 30pF + 120pF) \times 30k\Omega \times ln\left(1 - \frac{7.5V}{16V + 30k\Omega \times 0.13mA}\right) + 1.4\mu s = 4.95\mu s$$

Note that C_{BLANK_HU} (C381) and R_{DESAT_HU} (R341, R351) are also related to the power module V_{CE} and the DESAT_HU terminal noise immunity (CR filter) when DESAT is detected.

The tDESAT_TOTAL must be shorter than the short-circuit permissible duration of the power module.

Fig. 4.10 shows the DESAT detection timing chart.

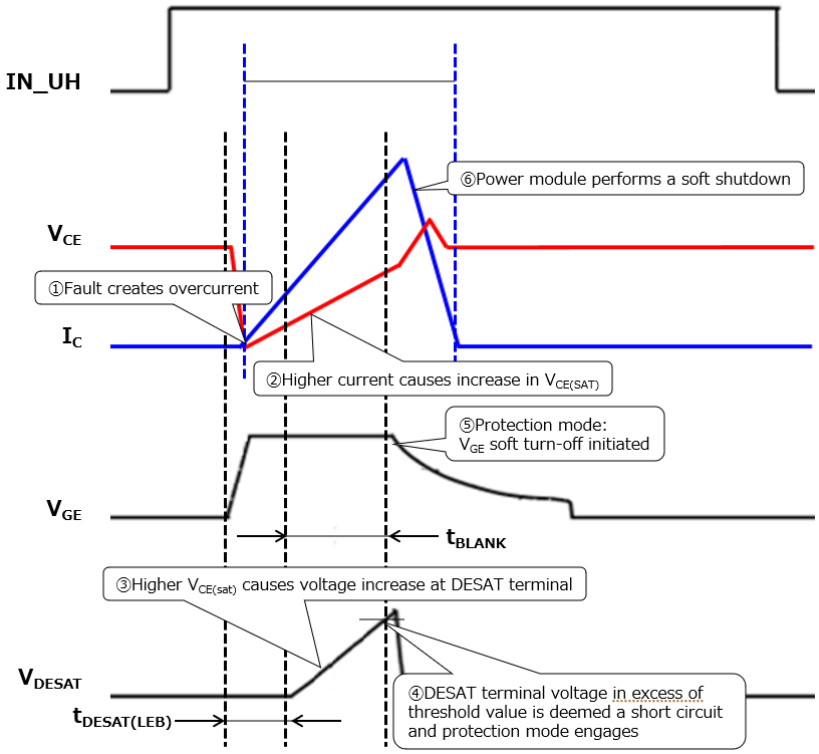

Fig. 4.10 DESAT Detection Timing Chart

Depending on actual use conditions, if the parasitic inductance (Ls) of the electric wiring generates a large surge voltage when current is interrupted, and exceeds the component rated voltage, damage may result. To reduce the surge-voltage due to Ls, the snubber circuit must be connected as close as possible to the power module. Be sure to fully verify DESAT detecting operation on the actual device.

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4.6.2. UVLO Function (Under Voltage Lock Out)

TLP5222 incorporated in this design has a built-in UVLO function. The voltage of the gate-power supply of the secondary positive power supply (V_{CC2_HU}–V_{E_HU}) is monitored and stopped when the operating threshold voltage UVLO threshold (V_{UVLO-_HU}) is dropped. It returns to normal operation when the positive power supply exceeds V_{UVLO+_HU}. This function prevents the power module from passing current between the collector and emitter at an insufficient gate voltage, and is intended to prevent damage caused by overheating.

Positive Supply Voltage Undervoltage Protection (UVLO)

When the secondary positive power supply voltage (V_{CC2_HU}-V_{E_HU}) of TLP5222 drops to the threshold voltage V_{UVLO-_HU}, the gate drive output is stopped. When the secondary positive power supply voltage (V_{CC2_HU}-V_{E_HU}) rises to the threshold voltage V_{ULVO+_HU}, gate-drive output is enabled.

UVLO threshold is shown in Table4.3.

Table 4.3 UVLO Threshold Voltage

UVLO threshold	V_{UVLO+_HU}	11.4V (Typ.)
	V_{UVLO-_HU}	10V (Typ.)

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4.6.3. Active Miller Clamp (AMC)

In a bridge configuration where the switching devices such as IGBTs etc. are connected in series one above the other, when one device turns on, the high dv/dt between the collector and emitter causes current to flow through the collector-to-gate capacitance of the other device in the off-state, raising the gate and potentially causing false firing.

This is called self-turn-on. Active Miller Clamp (AMC) is a function to prevent this.

TLP5222 in this design has a built-in AMC, so there is no need for an external clamping circuit. The miller clamp pin V_{CLAMP_HU} is connected to the gate terminal of IGBT.

When the gate control signal on IN_HU (Pin1 of CN11) is at the L level (V_{OUT_HU} is the L level), the gate voltage of the power module drops and MOSFET between V_{CLAMP_HU}-V_{EE_HU} goes ON and the gate is clamped to the emitter (VEE). This operation suppresses the rise in gate voltage and prevents self-turn-on.

Fig. 4.11 shows the active miller clamp operation.

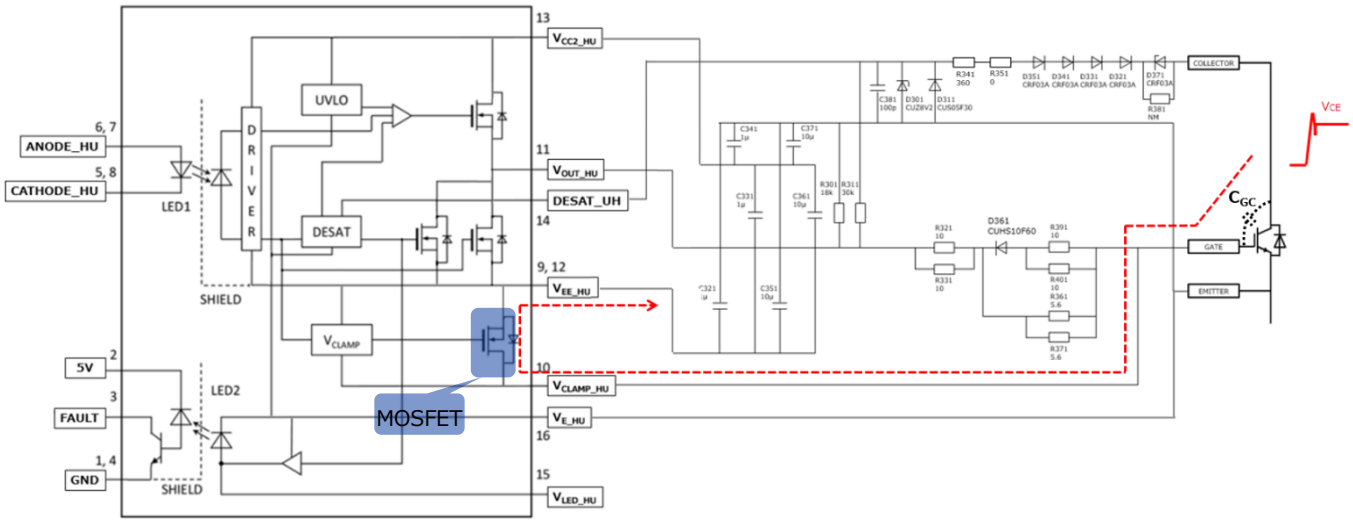

Fig. 4.11 Active Miller Clamp Operation

4.7. Temperature Detection Output

Pin19, Pin21 of CN11 in this design are connected to the outputs of the thermistors built into the power module. The connector CN12 on the back of the board can be connected to the power module to monitor the temperature. This design is not equipped with a temperature detection circuit, so add an external detection circuit if necessary.

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