# Automotive 3kW 48V-12V Bidirectional DC-DC Converter

# Design Guide

## RD210-DGUIDE-01

Toshiba Electronic Devices & Storage Corporation

# Table of Contents

# 1. Introduction

This design guide describes the circuit design of various sections of the Automotive 3kW 48V-12V Bidirectional DC-DC Converter (hereinafter referred to as “this Design”).

As a result of worldwide efforts to reduce greenhouse-gas emissions, the use of hybrid-electric vehicles and battery-powered electric vehicles called xEV is becoming increasingly popular instead of conventional vehicles which use only internal combustion engines as power sources. These xEVs are increasingly being equipped with 48V's Li ion battery to reduce power dissipation. However, 12V batteries must be installed when some existing 12V applications that require lead-acid batteries as power source are used. This design is a bidirectional converter that realizes step-down (buck) operation from 48V to 12V and step-up (boost) operation from 12V to 48V. And such a converter is essential in applications where 48V batteries and 12V batteries coexist.

From our automotive N-channel power MOSFET lineup with low on-resistance and high heat dissipation, 40V rated XPQR3004PB is used for the high-side MOSFETs, low-side MOSFETs of the switching section and the input/output switches of the 12V line, and 100V rated XPW4R10ANB is used for the input/output switches of 48V line to achieve high-efficiency operation.

The input/output circuit of 12V line also uses a high-side N-channel power MOSFET gate driver TPD7106F with a reverse-connection protection function, and by driving MOSFET with a back-to-back connection *, it protects against circuit destruction when the batteries are connected in reverse.

* A configuration in which two MOSFETs are connected in series with their drain or source pins connected. The positive and negative bidirectional currents can be cut off when the switch is off.

# 2. Main Components Used

This chapter describes the main components used in this design.

## 2.1. Power MOSFET XPW4R10ANB

A 100V withstanding voltage N-channel MOSFET XPW4R10ANB is used in the 48V line (high-voltage side) input/output switch section and DC-DC converter section. The main features of XPW4R10ANB are as follows.

- AEC-Q101 qualified
- Small size, thin and small mounting area.
- Low on resistance: $R_{DS(ON)}$ = 3.4mΩ (Typ.) ($V_{GS}$ = 10V)
- Low leakage current: $I_{DSS}$ = 10μA (Max.) ($V_{DS}$ = 100V)
- Enhancement mode: $V_{th}$ = 2.5 to 3.5V ($V_{DS}$ = 10V, $I_D$ = 1.0mA)

**Appearance and Pin Layout**

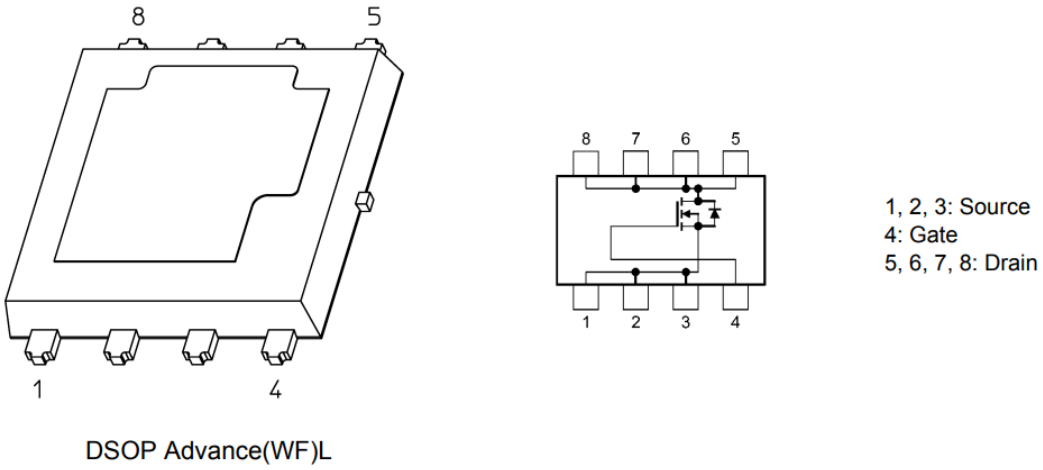


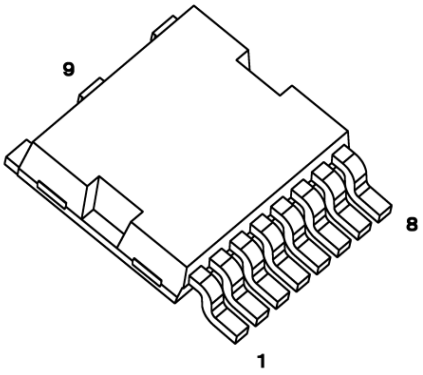

**Fig. 2.1 Appearance and Pin Layout of XPW4R10ANB**

## 2.2. Power MOSFET XPQR3004PB

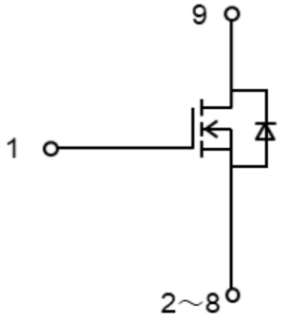
A 40V withstanding voltage N-channel MOSFET XPQR3004PB is used in the 12V line (low-voltage side) input/output switch section. The main features of XPQR3004PB are as follows.

- AEC-Q101 qualified
- Low on resistance: $R_{DS(ON)}$ = 0.23mΩ (Typ.) ($V_{GS}$ = 10V)
- Low leakage current: $I_{DSS}$ = 10μA (Max.) ($V_{DS}$ = 40V)
- Enhancement type: $V_{th}$ = 2.0 to 3.0V ($V_{DS}$ = 10V, $I_D$ = 1.0mA)

**Appearance and Pin Layout**




L-TOGL™




1: Gate
9: Drain (heatsink)
2 to 8: Source

Note: L-TOGL™ is a trademark of Toshiba Electronic Devices & Storage Corporation.

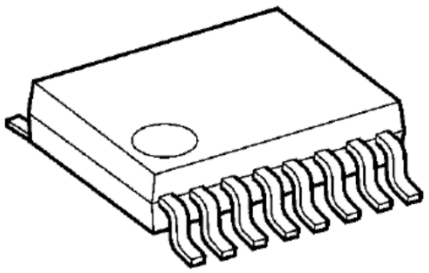
**Fig. 2.2 Appearance and Pin Layout of XPQR3004PB**

## 2.3. High-Side N-Channel MOSFET Gate Driver TPD7106F

This design uses a one-channel high-side N-channel MOSFET gate driver TPD7106F to drive MOSFET of the 12V line (low-voltage side) input/output switching section. The main features of TPD7106F are as follows.

- AEC-Q100 qualified
- Built-in charge pump circuit (charge pump capacitor is external)
- Output current is -10mA/+400mA and drive by parallel use of N-channel power MOSFET is possible
- Built-in protection for reverse connection of power supply
- Built-in diagnosis output for under voltage of charge pump circuit
- SSOP16 package for surface mounting

**Appearance and Pin Layout**



SSOP16-P-225-0.65B

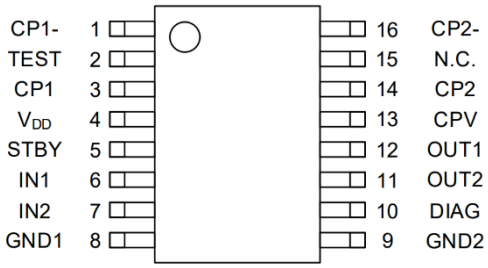



**Fig. 2.3 Appearance and Pin Layout of TPD7106F**

# 3. Basic Operation of Bidirectional DC-DC Converter

This chapter describes the basic concepts of bidirectional DC-DC converters. Fig. 3.1 (c) shows the configuration of a typical non-isolated bidirectional DC-DC converter used in this design. The inductor of the buck DC-DC converter shown in Fig. 3.1 (a) and the inductor of the boost DC-DC converter shown in Fig. 3.1 (b) are shared and combined. In Fig. 3.1 (c), when the flow of power is from $E_1$ to $E_2$, $Q_1$ is switched to operate as a buck DC-DC converter, and when the flow of power is from $E_2$ to $E_1$, $Q_2$ is switched to operate as a boost DC-DC converter.

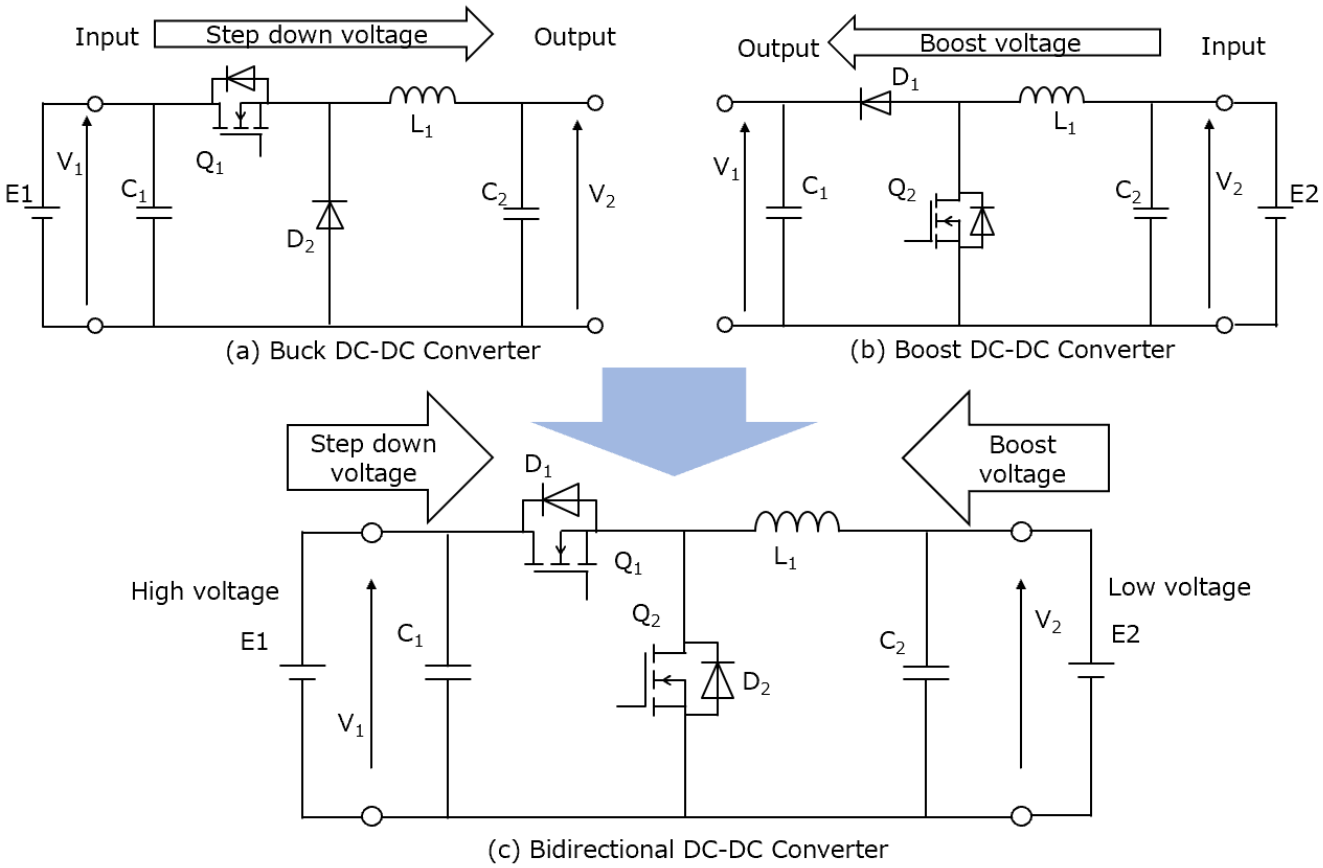



**Fig. 3.1 Bidirectional DC-DC Converter**

## 3.1. Buck DC-DC Converter Operation

In the buck DC-DC converter shown in Fig. 3.2, during $t_{ON}$, MOSFET Q is turned on, and ($V_{IN}$-$V_{OUT}$) voltage is applied to both ends of the coil L. The following ripple current flows around the output current $I_{OUT}$.

$$\Delta I_L = \frac{(V_{IN} - V_{OUT})}{L} \times t_{ON}$$

When Q is off i.e. $t_{OFF}$, to maintain the current flowing through coil L, the current flows to the load via diode D. The ripple current during this period is expressed by the following equation.

$$\Delta I_L = \frac{V_{OUT}}{L} \times t_{OFF}$$

In steady-state, $\Delta I_L$ when Q is on is equal to $\Delta I_L$ when Q is off. Therefore, if the switching period is set to T and the duty of the period when Q is on is set to D, the following equation is established.

$$V_{OUT} = \frac{t_{ON}}{(t_{OFF} + t_{ON})} \times V_{IN} = \frac{t_{ON}}{T} \times V_{IN} = D \times V_{IN}$$

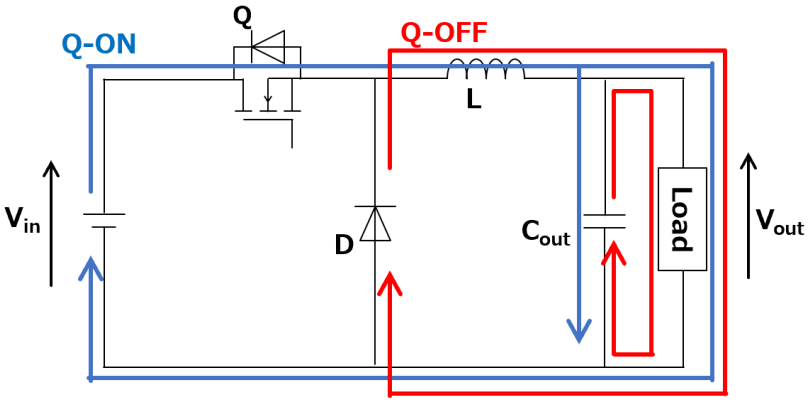



**Fig. 3.2 Buck DC-DC Converter Circuit**

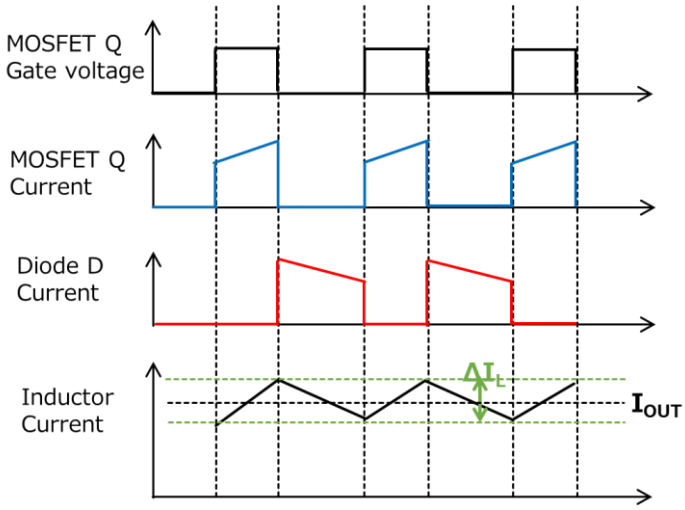



**Fig. 3.3 Buck DC-DC Converter Current Waveforms**

## 3.2. Boost DC-DC Converter Operation

In the boost DC-DC converter circuit shown in Fig. 3.4, during $t_{ON}$, MOSFET Q is turned on and the input voltage $V_{IN}$ is applied to the coil L. The following ripple current flows around the input current $I_{IN}$.

$$\Delta I_L = \frac{V_{IN}}{L} \times t_{ON}$$

When Q turns off, the energy stored in the coil is released during the on period, and a voltage higher than the input voltage is generated. During this duration $t_{OFF}$, to maintain the current flowing through coil-L, current flows to the load via diode D. The ripple current during this period is expressed by the following equation.

$$\Delta I_L = \frac{(V_{OUT} - V_{IN})}{L} \times t_{OFF}$$

In steady state, $\Delta I_L$ when Q is on is equal to $\Delta I_L$ when Q is off. Therefore, if the switching period is set to T and the duty of the period when Q is on is set to D, the following equation is established.

$$V_{OUT} = \frac{(t_{ON} + t_{OFF})}{t_{OFF}} \times V_{IN} = \frac{T}{T - T_{ON}} \times V_{in} = \frac{1}{1 - \frac{T_{ON}}{T}} \times V_{in} = \frac{1}{1 - D} \times V_{IN}$$

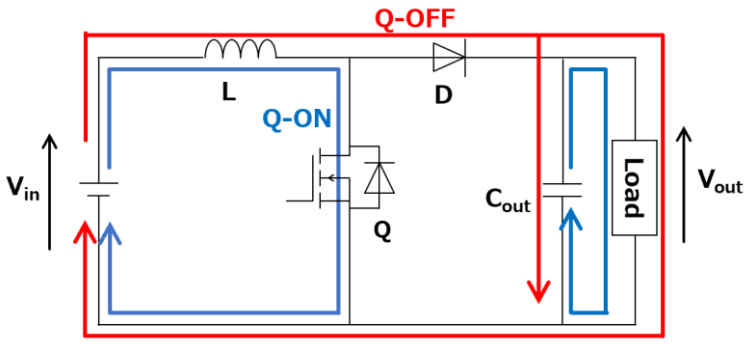



**Fig. 3.4 Boost DC-DC Converter Circuit**

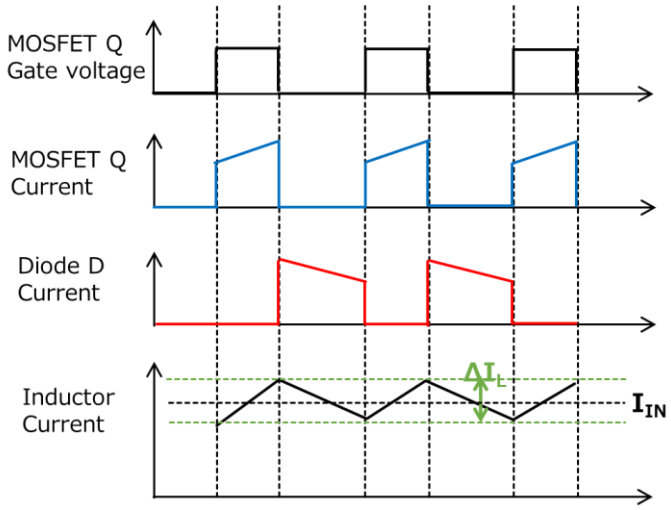



**Fig. 3.5 Boost DC-DC Converter Current Waveforms**

# 4. Automotive 3kW 48V-12V Bidirectional DC-DC Converter

This chapter provides an overview of the configuration of this design and the circuit design of each part. Fig. 4.1 shows the configuration of this design. Four blocks of non-isolated bidirectional DC-DC converter circuits in parallel.

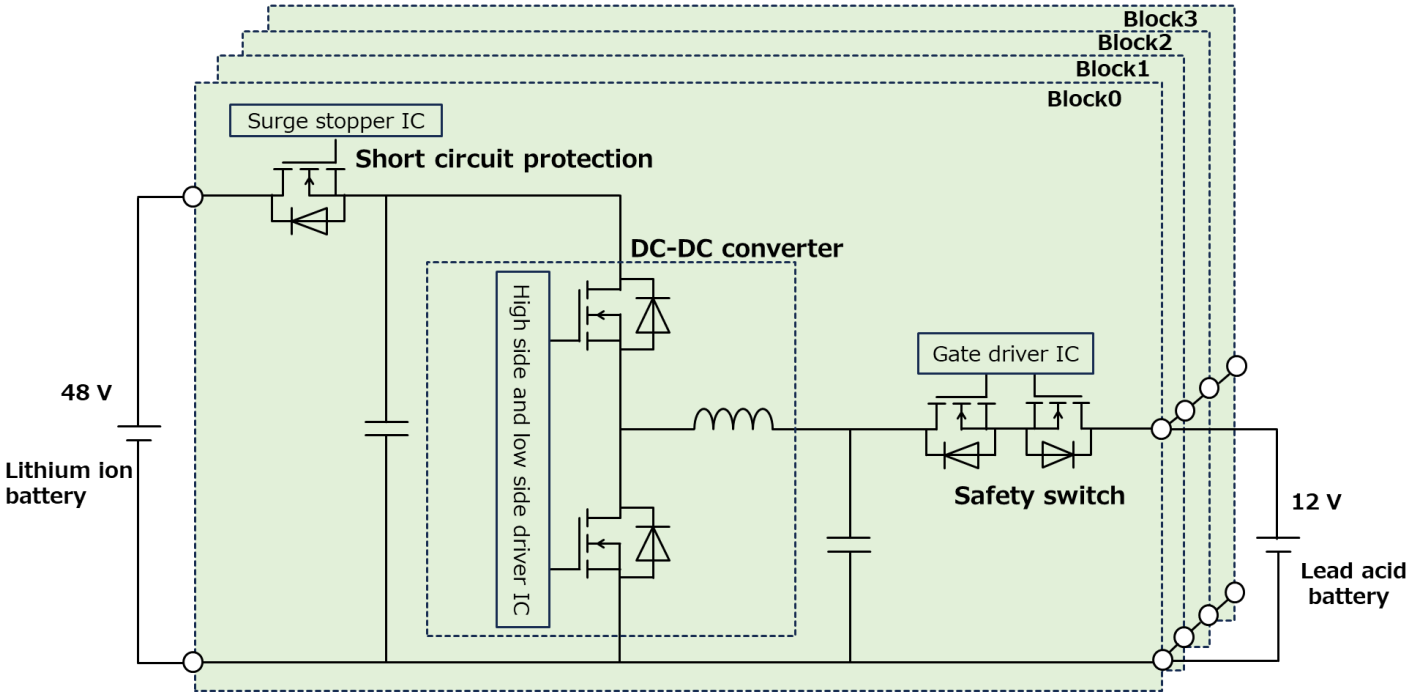



**Fig. 4.1 Configuration Diagram of This Design**

## 4.1. Specifications

Table 4.1 lists the main specifications of this design.

**Table 4.1 Specifications of This Design**

| Item | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **During buck operation** | | | | | |
| Input voltage | | 24 | 48 | 54 | V |
| Output voltage | | 11.85 | 12 | 12.15 | V |
| Maximum output power | 4-phase operation | | | 3 | kW |
| Switching frequency | | | 200 | | kHz |
| **During boost operation** | | | | | |
| Input voltage | | 5 | 12 | 16 | V |
| Output voltage | | 47.4 | 48 | 48.6 | V |
| Maximum output power | Vin = 12V or higher, 4-phase operation | | | 3 | kW |
| Switching frequency | | | 200 | | kHz |
| **Common items** | | | | | |
| Protection function | Input undervoltage protection, input overcurrent protection, input overpower protection, output overvoltage protection, output overcurrent protection, output short-circuit protection, and overheat protection | | | | |
| Board layer configuration | Main Board: FR-4 6-layer configuration, copper foil thickness of 105μm (surface layer) and 210μm (inner layer)<br><br>Control Board: FR-4 4-layer configuration, copper foil thickness of 35μm | | | | |

## 4.2. Circuit Configuration

Fig. 4.2 shows the circuit block configuration of this design. Input/output circuit (load switches) are provided for each block of a four-block bidirectional DC-DC converter. The system is designed to operate safely in the remaining three blocks even if a fault or fault occurs in one of the four blocks of bidirectional DC-DC converters.

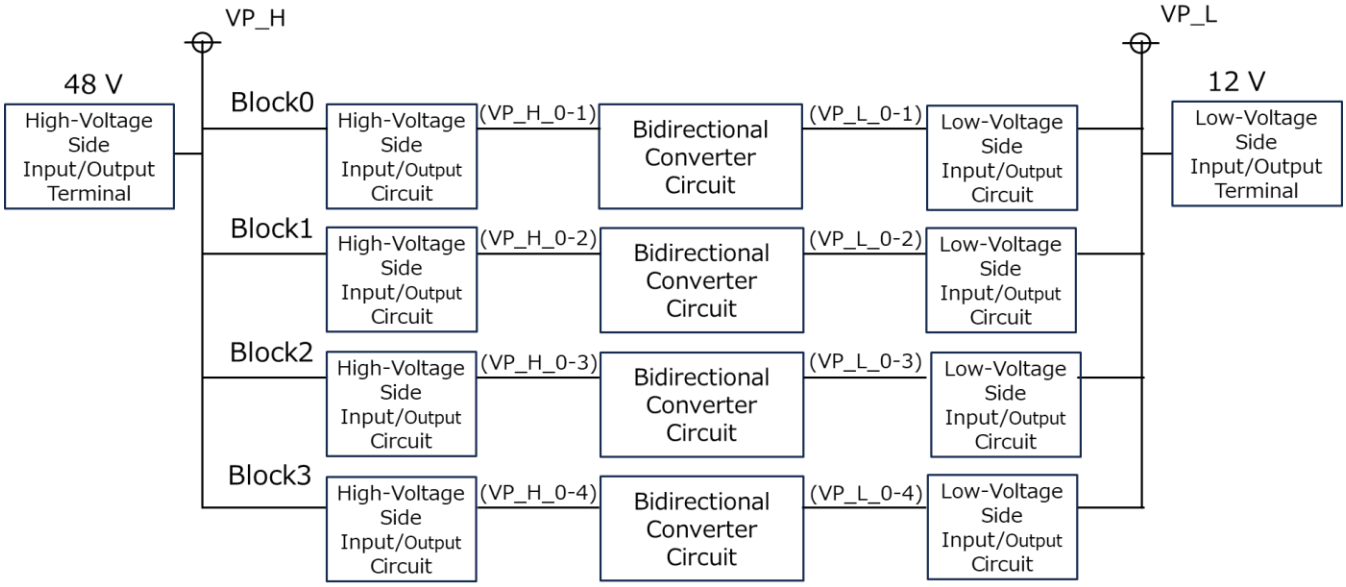



**Fig. 4.2 Circuit Block Configuration of this Design**

## 4.3. High-Voltage Side Input/Output Circuit

Fig. 4.3 shows one block of the high-voltage input/output circuit of this design. The power line capacitors ($C_1$ to $C_{12}$) are inserted into only Block0 circuit out of Bolck0 to 3. From the fail-safe point of view, two capacitors are arranged in series so that even if one capacitor is short-circuited, there is no problem. Two MOSFET XPW4R10ANB are inserted in parallel in 48V line. They are driven by the control IC LTC4364-2 (Analog Devices) (hereinafter referred to as “control IC”). This section explains the circuit of this block. For more information on the control IC, refer to LTC4364-2 datasheet and related documentation.

Typical application example of this IC is shown in Fig. 4.4. It drives the N-channel MOSFET (M1) on HGATE pin, limits the voltage/current to the load circuit during power transient or overcurrent events. DGATE pin is used to drive the second N-channel MOSFET (M2) as an ideal diode to protect the load from being damaged during reverse-polarity input conditions, and to prevent the generation of reverse current from the input voltage. In this design, M2 is not inserted because it is assumed that the high-voltage input/output terminal will not be touched or operated externally.

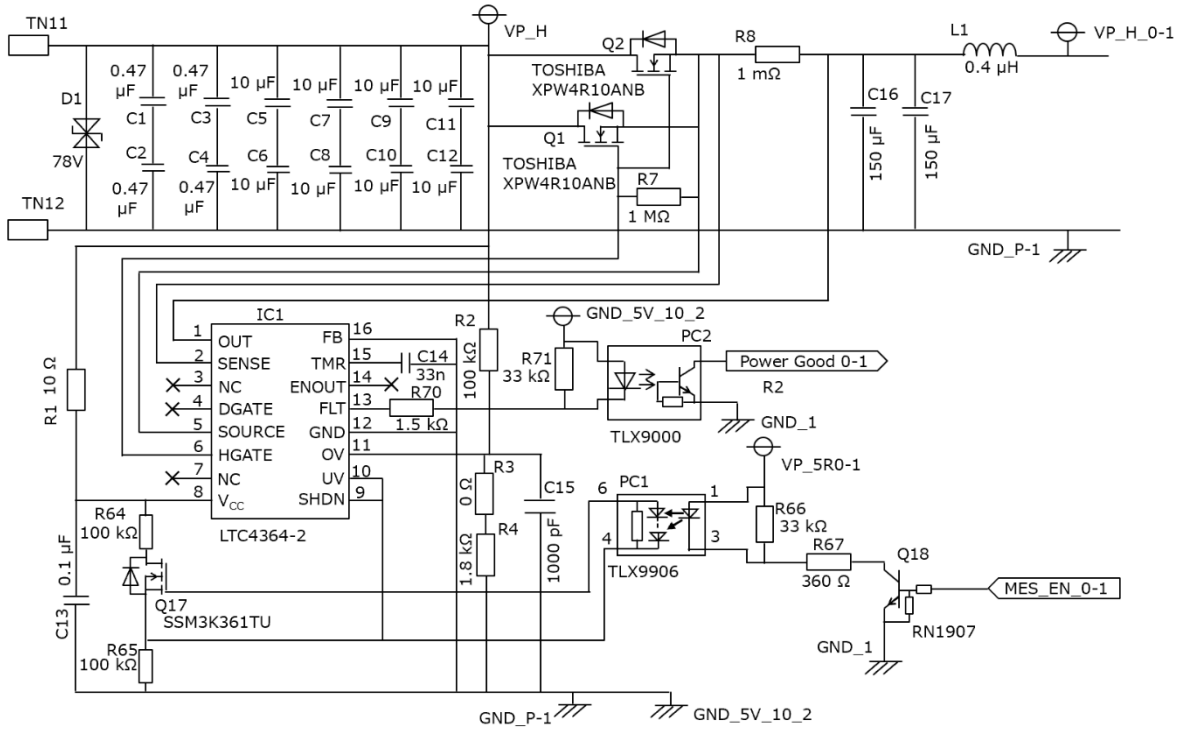



**Fig. 4.3 High Voltage Side Input/Output Circuit**

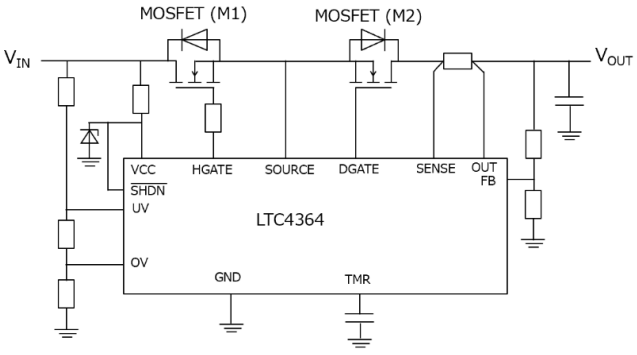



**Fig. 4.4 Control IC Typical Circuit**

### 4.3.1. Overcurrent Protection

The control IC has an adjustable current-limiting circuit that protects against short circuits and excessive load-currents. If the voltage on OUT pin is higher than 2.5V, HGATE pin is controlled during an overcurrent event, and the current sense voltage between SENSE pin and OUT pin ($\Delta V_{SNS}$) is limited to 50mV. If the voltage at OUT pin is lower than 1.5V, the current limit detect voltage is reduced to 25mV in order to add protection in case of an output-short circuit. The current-sensing resistor is placed between SENSE pin and OUT pin. $R_{SNS}$ is given by the following equation:

$$R_{SNS} = \frac{\Delta V_{SNS}}{I_{LIM}}$$

If OUT is higher than 2.5V in this design, $R_{SNS}$ (Fig. 4.3, R8) is 1mΩ, and $\Delta V_{SNS}$ is limited to 50mV, so $I_{LIM}$ per ladder is 50A. $I_{LIM}$ is 25A when OUT is lower than 1.5V.

### 4.3.2. Input Overvoltage Comparator

The overvoltage is detected using an external resistor divider (Fig. 4.3, R2 and R3+R4) connected to OV pin and line voltage. Upon power-up, prior to reaching the 100μs internal power-on reset deadline or prior to resolving the low-voltage status at UV pin, if OV pin's voltage is higher than its threshold (1.25V), HGATE pin is held at "L" until OV pin's voltage is lower than its threshold. In this design, the line-voltage is 71V when R2 is 100kΩ, R3+R4 is 1.8kΩ, and the voltage at OV pin is 1.25V. Therefore, when the input-voltage exceeds 71V, HGATE pin is "L".

### 4.3.3. Fault Timer

The control IC incorporates an adjustable fault timer. Connecting a capacitor C14 between TMR and GND sets the delay before MOSFET (Fig. 4.3, Q1, Q2) turns off in the event of an overvoltage fault condition or an overcurrent fault condition. The same capacitor also sets the duration of the cool-down to allow MOSFET to be turned on again after the fault condition has been cleared.

## 4.4. Bidirectional Converter Circuit

Fig. 4.5 shows the circuit for one block of the bidirectional converter in this design. Control signals from MCU TMS320F28377S (Texas Instruments) (hereinafter referred to as “MCU”) are fed to the gate driver IC UCC27211A (Texas Instruments) (hereinafter referred to as “driver IC”) via the isolator ISO6720 (Texas Instruments) (hereinafter referred to as “isolator”) and the buffer IC TC7PZ17FU to drive the high-side and low-side MOSFETs XPW4R10ANB. Three MOSFETs are used in parallel on both the high side and low side to reduce conduction loss. Sense resistors (R29, R38) are inserted between the high-voltage and low-voltage power lines, and the voltage across these is input to the current sense circuit. The inductor current at the inductor L2 is also detected by the current sensing circuit.

This section explains the circuit of each part of the bidirectional DC-DC converter. Refer to the device data sheet and related documentation for details of the devices used.

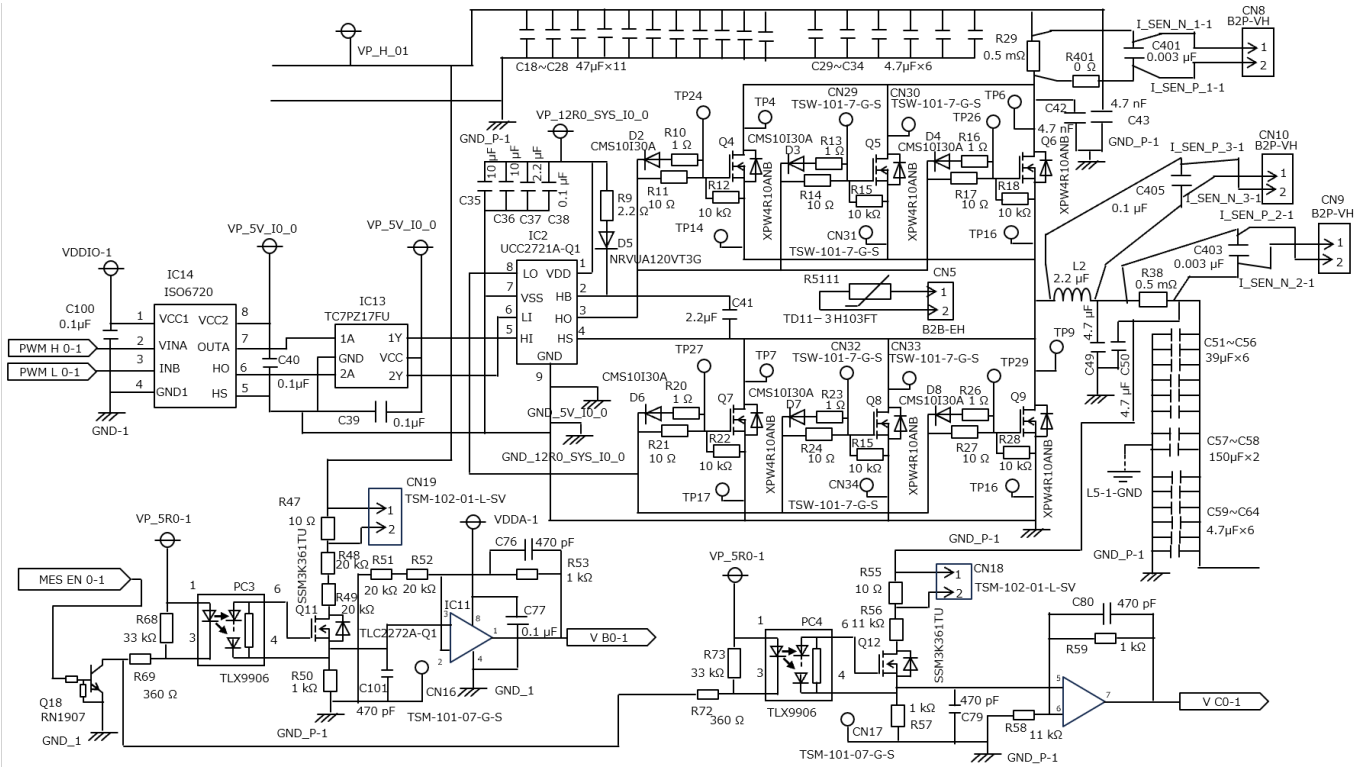



**Fig. 4.5 Bidirectional DC-DC Converter Circuit**

### 4.4.1. MOSFET Driver

The high-side and low-side MOSFETs are driven by the driver IC. Fig. 4.6 shows the internal circuit of the driver IC and an external connection example. This driver IC receives the high-side and low-side PWM. The high-side signal is a signal that is referenced to the switch node (HS) by a level-shifting circuit, enabling control of HO signal.

The high-side driver is powered by a bootstrap circuit. The bootstrap diode is built-in, and the bootstrap capacitor is externally connected between HB and HS terminal and is charged from $V_{DD}$ when the low-side MOSFET is on. The high-side driver is referenced to the switch-node (HS) where the source of the high-side MOSFET and the drain of the low-side MOSFET are connected, while the low-side driver is referenced to $V_{SS}$, which is normally ground.

This driver IC has a UVLO function for the drive power supply of high-side and low-side drivers to monitor $V_{DD}$ and $V_{HB}$-$V_{HS}$. $V_{DD}$ UVLO disables both drivers if $V_{DD}$ drops below a specified threshold. $V_{DD}$ threshold is 7.0V and the hysteresis is 0.5V. $V_{HB}$ UVLO disables only the high-side driver when $V_{HB}$-$V_{HS}$ drops below a specified threshold. $V_{HB}$ UVLO rise threshold is 6.7V and the hysteresis is 1.1V.

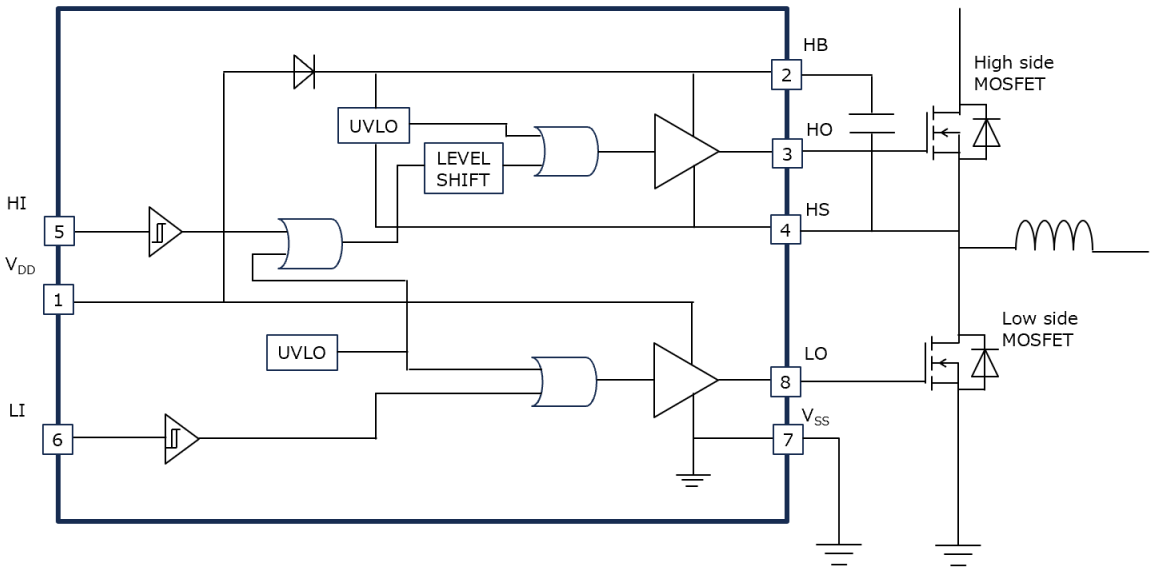



**Fig. 4.6 Gate Driver IC Connection Example**

### 4.4.2. Current Sense Circuit

Current is detected by sense resistors inserted at the high-voltage and low-voltage sides of the bidirectional DC-DC converter. The inductor current of the circuit is also detected. Fig. 4.7 shows the current sense circuit on the high-voltage side, Fig. 4.8 shows the current sense circuit on the low-voltage side, and Fig. 4.9 shows the current sense circuit for the inductor.

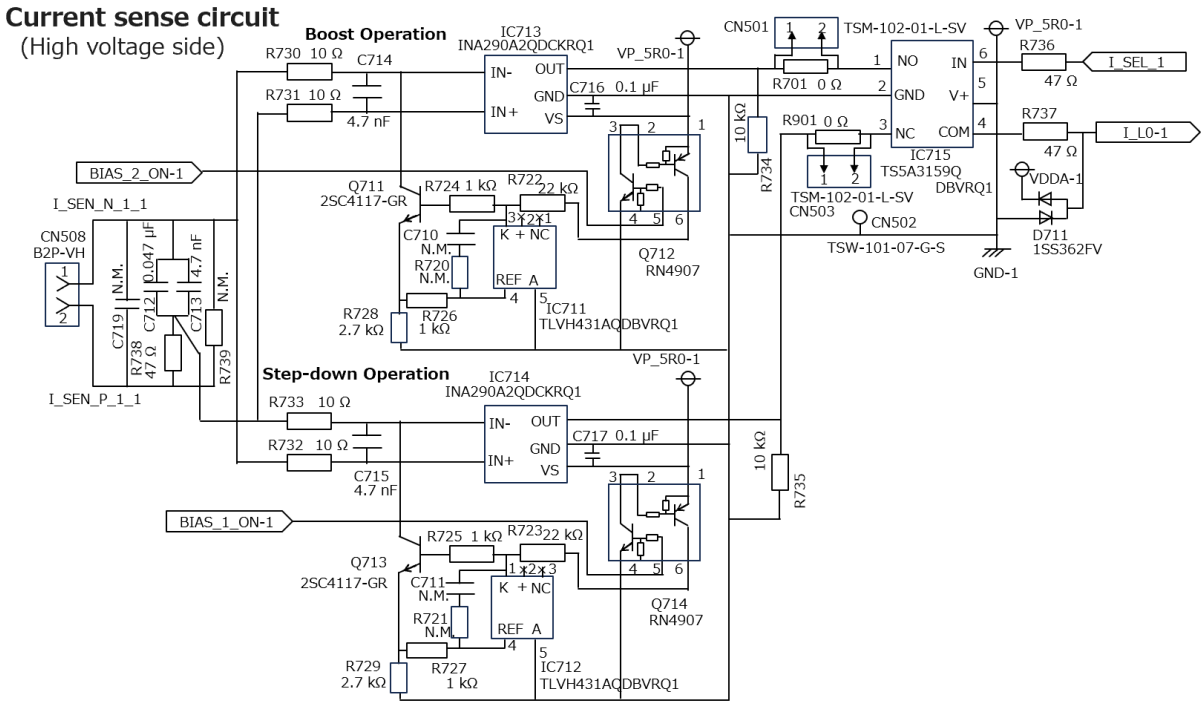



**Fig. 4.7 High-Voltage Side Current Sense Circuit**

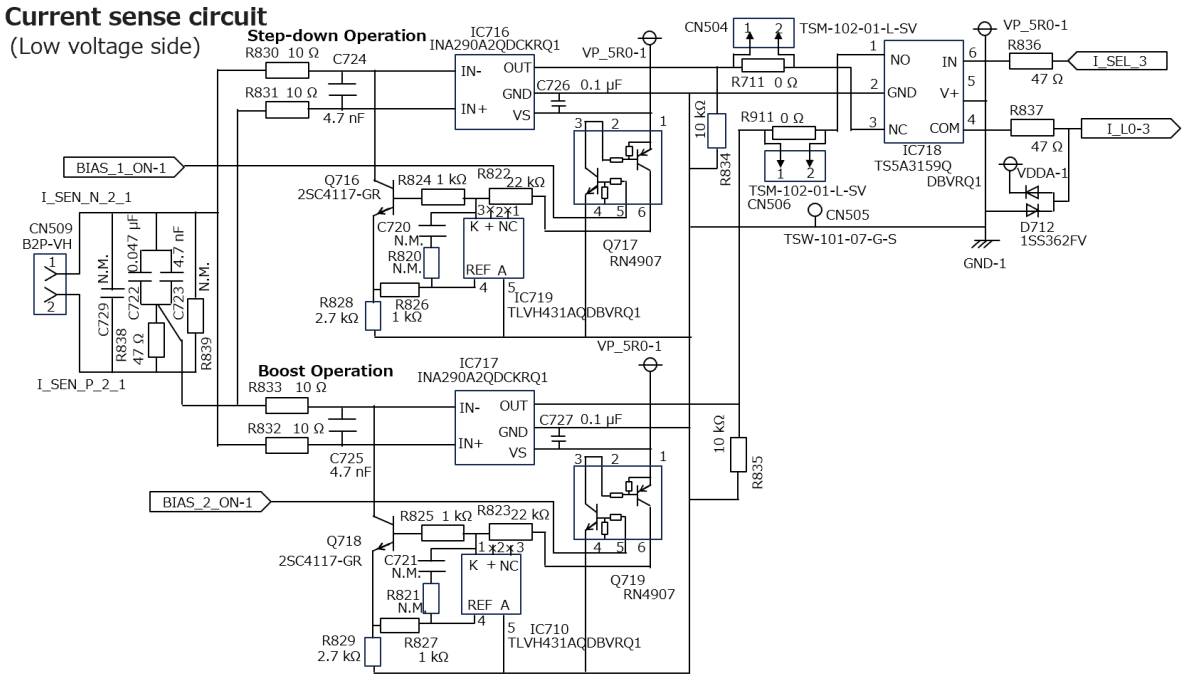



**Fig. 4.8 Low-Voltage Side Current Sense Circuit**

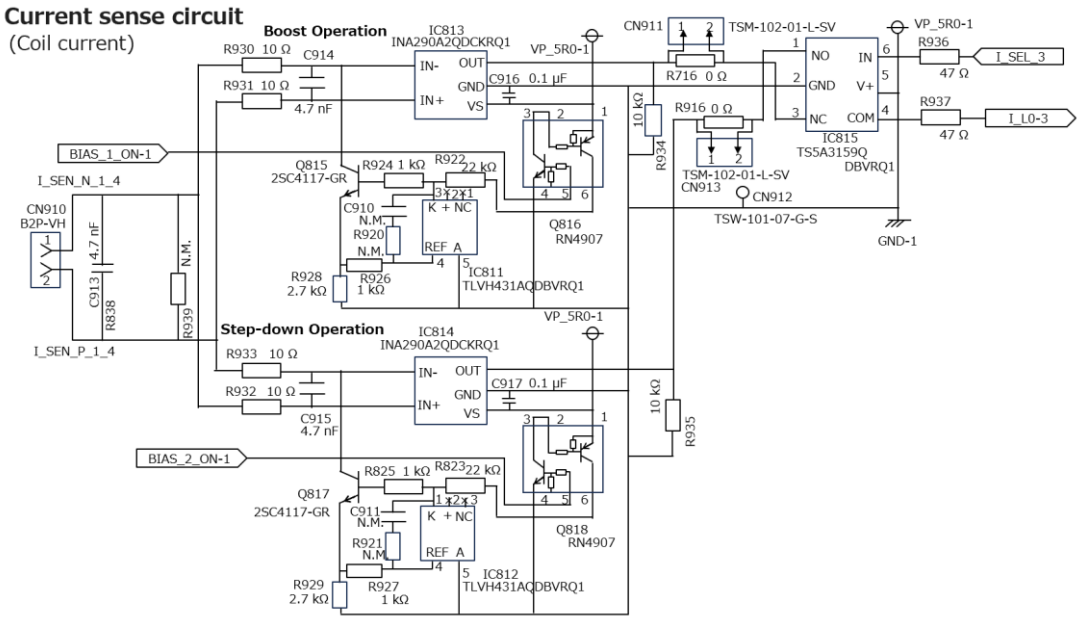



**Fig. 4.9 Inductor Current Sense Circuit**

Current of sense resistors and the inductor are sensed by the current sense amplifier INA290 (Texas Instruments) (hereinafter referred to as “current sense amplifier”). The current sense amplifier measures the voltage drop generated by the current flowing through the current sensing section, such as the current sense resistor. The current sense amplifier detects only the current that is supplied from the power supply to the system load because it is only in unidirectional mode. The gain G of the current sense amplifier is 50V/V, and the output-voltage $V_{OUT}$ of the current sense amplifier is as follows, where I is the current flowing through the sense resistor $R_{SENSE}$.

$$V_{OUT} = I \times R_{SENSE} \times G$$

This design uses two unidirectional current sense amplifiers to measure bidirectional current. Filters are also arranged in the input section. Fig. 4.10 shows the internal block diagram of the current sense amplifier and the input filter circuit. Refer to INA290 data sheet and related documentation for more information on filter resistances.

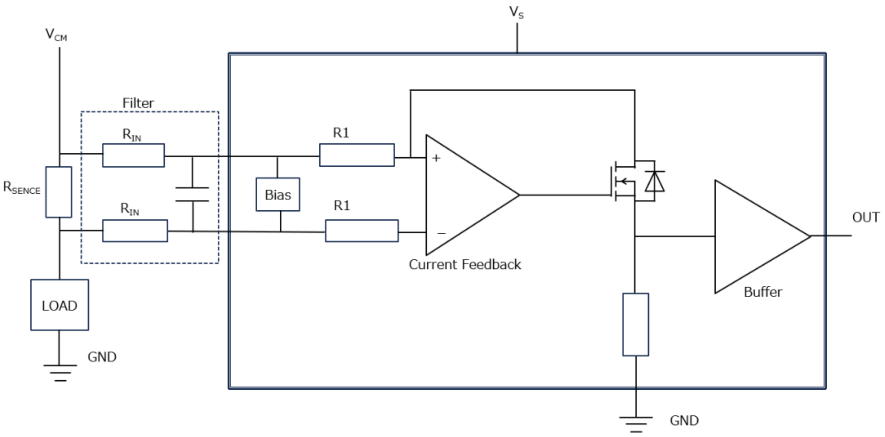



**Fig. 4.10 Current Sense Amplifier Circuit**

The output of the current sense amplifier is connected to an analog switch TSA3159 (Texas Instruments) (hereinafter referred to as “analog switch”). Analog switch is an SPDT (Single Pole Double Throw) switch that is designed to operate from 1.65V to 5.5V. A SPDT is a type of electric switch that has two input terminals and one output terminal. It can switch the input and output connection. Fig. 4.11 shows the internal configuration of the switch.

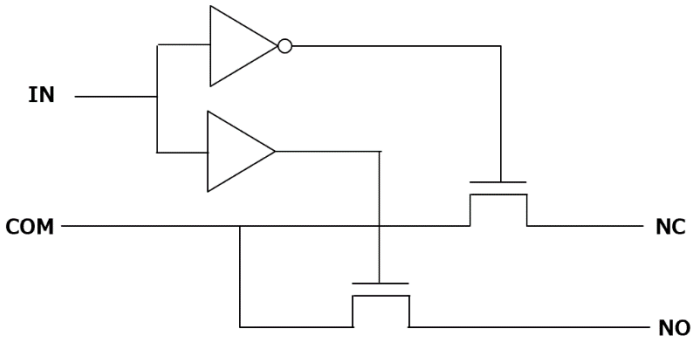



**Fig. 4.11 Analog Switch Internal Configuration**

When power is applied, COM pin is connected to NC pin. Where NC represents normally closed and NO represents normally open. If IN is Low, COM is connected to NC. If IN is high, COM is connected to NO. In this design, the operation state (buck or boost operation) is input to IN, the buck operation input/output current information of NC pin is output to COM pin during buck operation, and the boost operation input/output current information of NO pin is output to COM pin during boost operation.

## 4.5. Low-Voltage Side Input/Output Circuit

Fig. 4.12 shows one block of the low-voltage side input/output circuits in this design. The power-line capacitors (C85 to C96) are inserted only into Bolck0 circuit. From the fail-safe point of view, two capacitors are arranged in series and designed so that even if one capacitor is short-circuited, there is no problem. Two MOSFETs are inserted on the 12V line as the protection switches with their drain terminals connected (back-to-back connection). These MOSFETs is controlled by the high-side gate driver TPD7106F. To reduce power dissipation, two sets of switching MOSFETs XPQR3004PB are used in parallel.

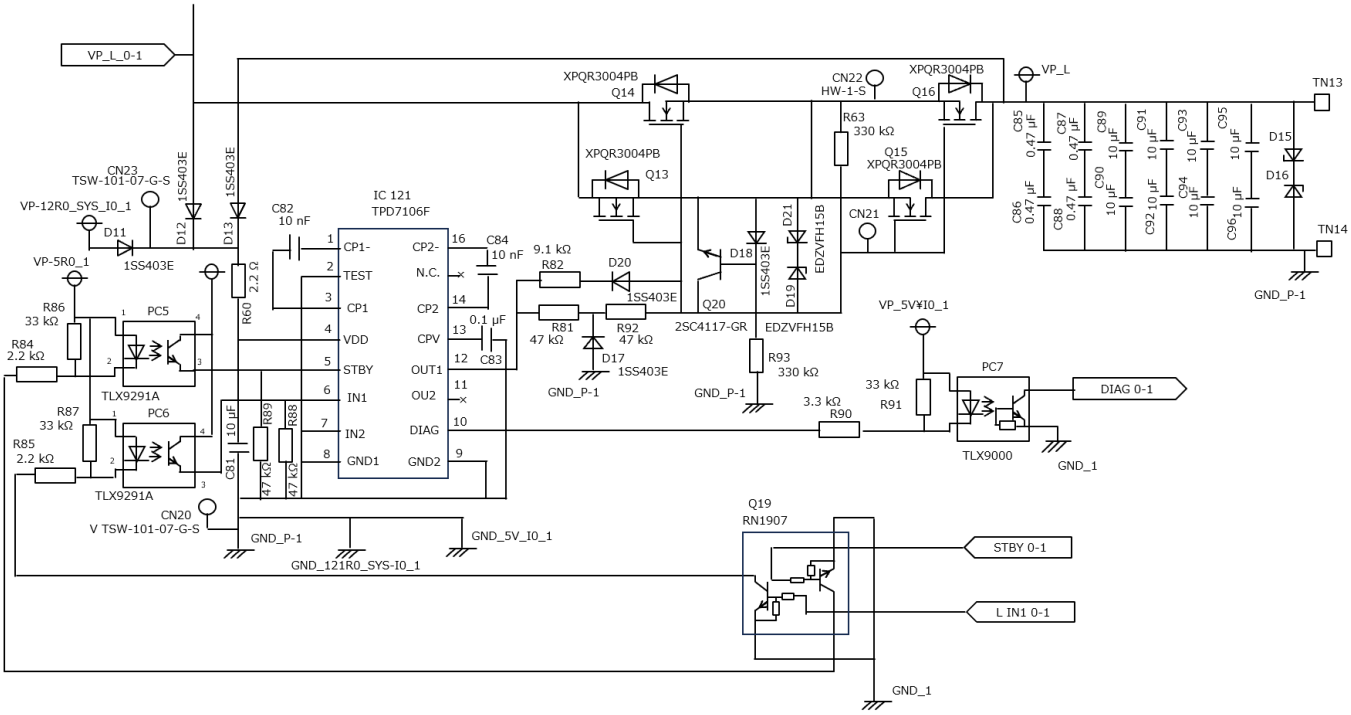



**Fig. 4.12 Low-Voltage-Side Input/Output Circuit**

In the back-to-back connection shown in Fig. 4.13, the body diode of MOSFET is reversed so that when the battery is connected in reverse, current can be prevented from flowing back through the body diode.

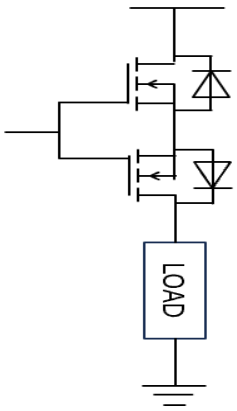



**Fig. 4.13 Back-to-Back Connection**

### 4.5.1. MOSFET Control for Switching

The protection and reverse connection protection switch (XPQR3004PB) is controlled by TPD7106F which is an N-channel power MOSFET gate driver for one channel high-side switch.

The functions of TPD7106F include on/off control and quick off control of external MOSFET by input signal. It also has built-in features like charge pump, voltage drop detection and power reverse connection protection. Fig. 4.14 shows the internal-block diagram of TPD7106F.

The operation using TPD7106F is outlined below.

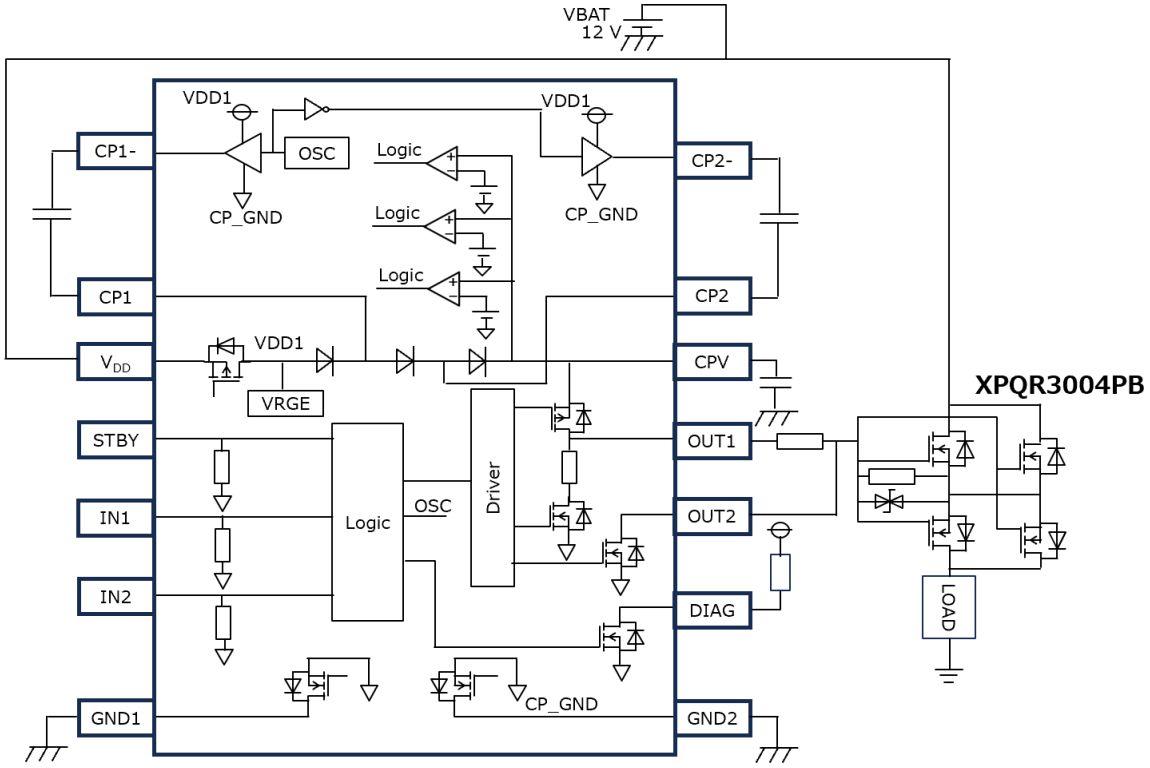



**Fig. 4.14 TPD7106F Internal Block Diagram**

### 4.5.2. Power MOSFET Gate Drive

**On-Driver Section**

TPD7106F receives a MOSFET turn-on command ($V_{IN1}$ = $V_{IH}$) from the input-pin IN1 (for normal on/off control), and the charge pump and drive circuit operate to drive MOSFET with enough voltage boosted by the charge pump. ($V_{OUT1}$ = $V_{DD}$+12V(Typ.))

* $V_{IN1}$: IN1 pin input voltage $V_{IH}$: High-level input voltage $V_{OUT1}$: OUT1 pin output voltage

**Off-Driver Section (Normally Off)**

In normal operation, IN1 receives a MOSFET turn-off command ($V_{IN1}$ = $V_{IL}$) from the input pin, and the external MOSFET is turned off by M2 shown in Fig. 4.15 (driver on resistance = 630Ω (Typ.).

* $V_{IL}$: Low-level input voltage

**Off-Driver Section (Rapid Off)**

When an external MOSFET or a short circuit around the load is detected and MOSFET needs to be turned off within a short time, IN2 of the input terminal receives MOSFET rapid off command ($V_{IN2}$ = $V_{IH}$), and M3 shown in Fig. 4.15 operates to quickly turn off the external MOSFET. (Driver on-resistor $R_{ONL2}$ = 5Ω (Typ.) The quick off driver operation duration ($t_{O2ON}$) is up to 200μs.

* $V_{IN2}$: IN2 pin

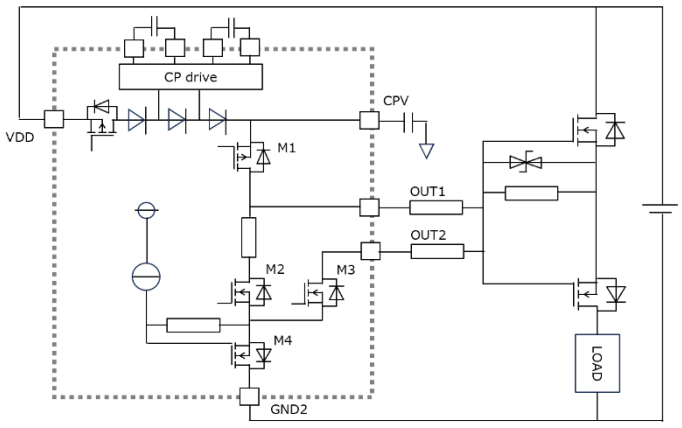



**Fig. 4.15 Configuration of TPD7106F Output Section**

**Operation Truth Table**

Table 4.1 shows the truth table of operation.

**Table 4.1 Truth Table**

| IN1 | IN2 | STBY | OUT1 | OUT2 | state |
|---|---|---|---|---|---|
| X | X | L | Hiz | Hiz | Stand-by mode |
| L | L | H | L | Hiz | Normal operation |
| H | L | H | H | Hiz | |
| L | H | H | L | L | Rapid off mode |
| H | H | H | L | L | |

### 4.5.3. Power Supply Reverse Connection Protection

When the power supply is connected in the reverse-polarity, the current from GND terminal is cut off by M4, M5, and the external MOSFETs are turned off.

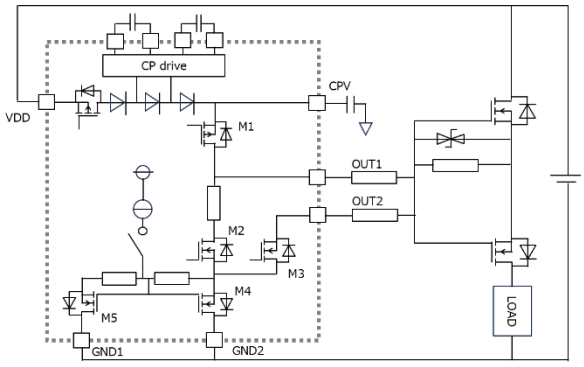



**Fig. 4.16 Power Supply Reverse Connection Protection**

### 4.5.4. Charge Pump Voltage Drop Detection

Fig. 4.17 shows the timing chart of charge pump voltage drop detection operation. This device monitors the CPV (Charge Pump Voltage Output Pin) voltage and detects any charge pump voltage drops. When the voltage falls below the charge-pump low judging voltage VCPL, DIAG pin becomes Low. Output-pin OUT1, OUT2 keeps operating. When STBY is set to the L state, the charge pump is stopped.

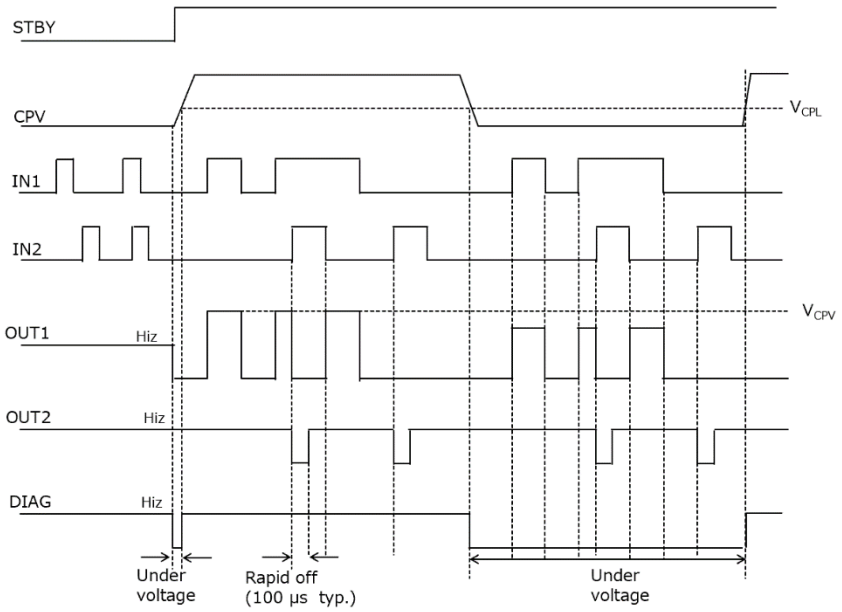



**Fig. 4.17 Timing Chart**

## 4.6. Control Power Supply

The basic block diagram of control power generation for this design is shown in Fig. 4.18. The control power supply circuit is shown in Fig. 4.19 and Fig. 4.20. The control power is generated from both input and output (12V, 48V) of the bidirectional DC-DC converter. As shown in Fig. 4.18, when 48V line voltage or 48V voltage is not supplied, 12V voltage is generated from 16.4V boosted from 12V line. This 12V is used as the power supply for MOSFET drive, and it is also used to generate 5V for each power board control and 5V for the MCU. 5V for MCU is also used to generate 1.2V and 3.3V for MCU.

This section provides an overview of each power supply circuit. Refer to the respective data sheets and related documents for the detailed description of the IC used for power generation.

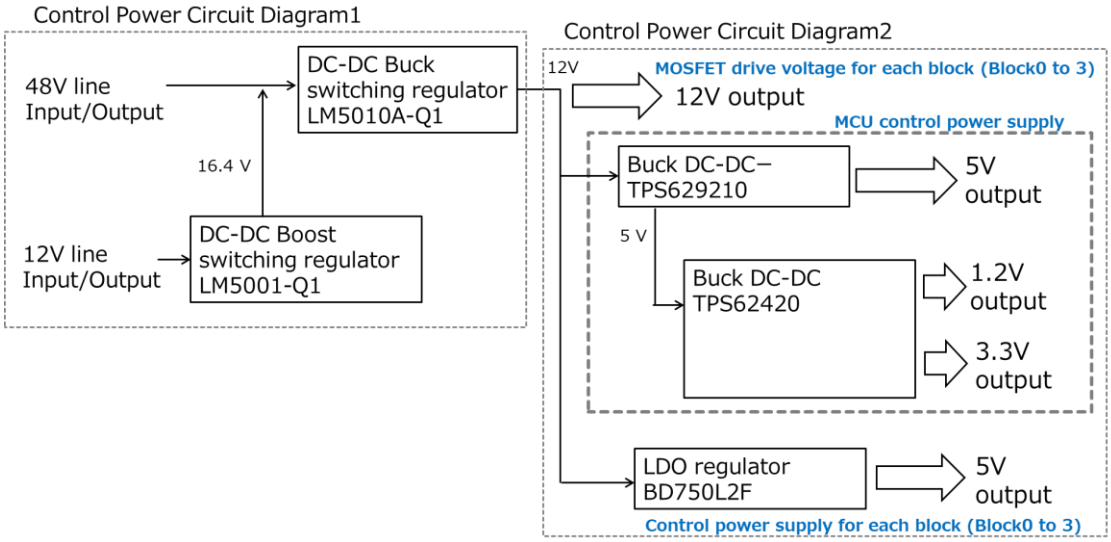



**Fig. 4.18 Control Power Configuration Diagram**

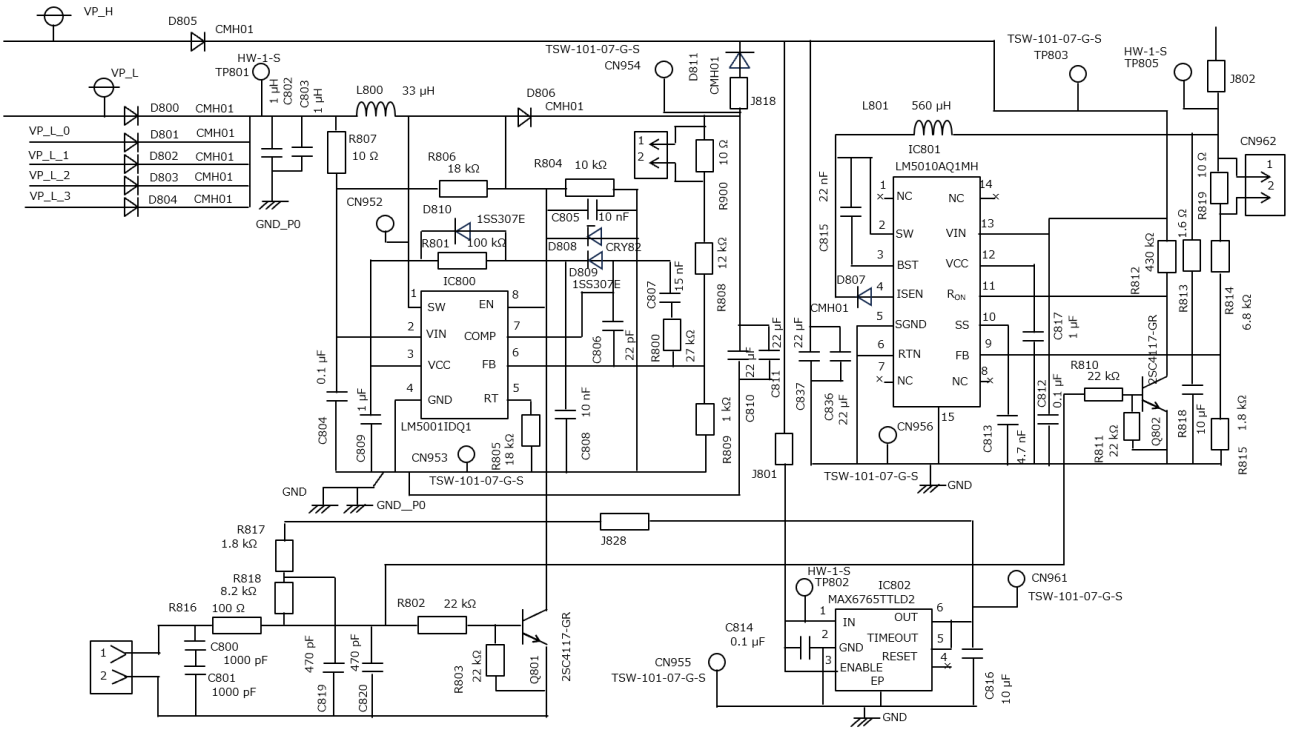



**Fig. 4.19 Control Power Circuit Diagram 1**

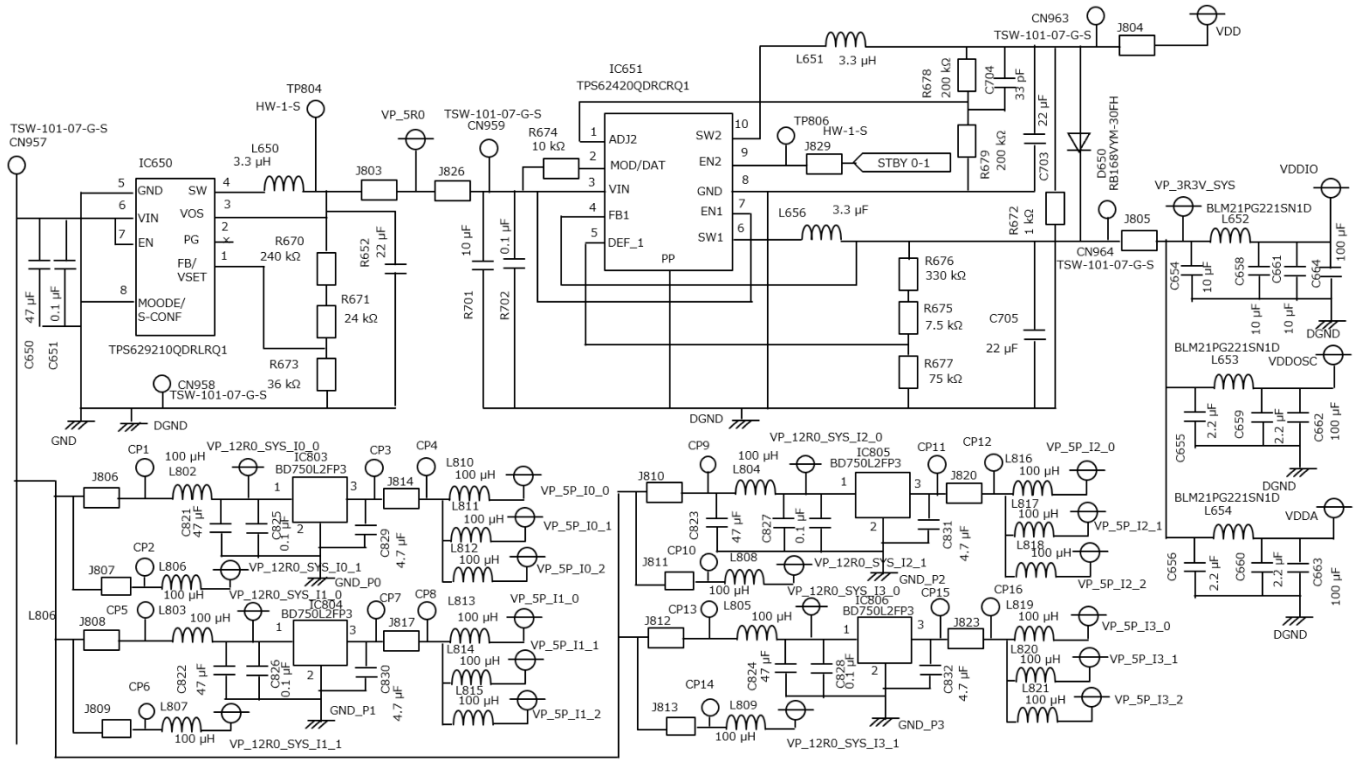



**Fig. 4.20 Control Power Circuit Diagram 2**

## 4.6.1. Boosting From the 12V Line Voltage

Boost converter IC LM5001-Q1 (Texas Instruments) (hereinafter referred to as “boost converter IC”) is used to boost from 12V. A typical basic configuration using a boost converter IC is shown in Fig. 4.21. Refer to LM5001 datasheet and related documentation for detailed circuit description.

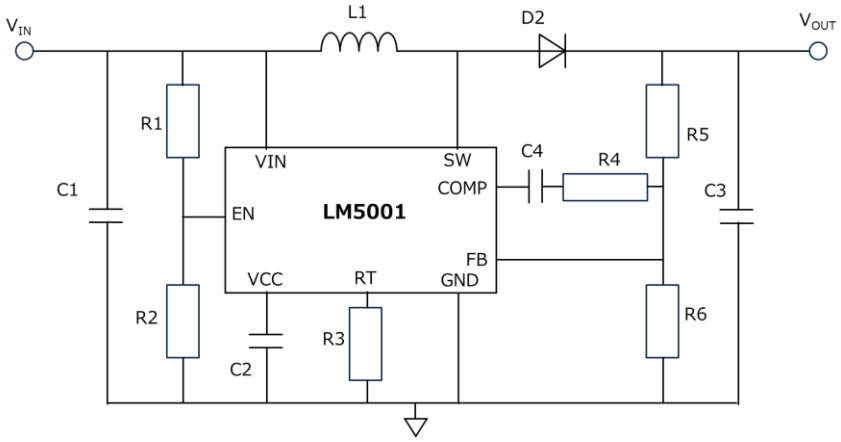



**Fig. 4.21 Boost Converter**

FB pin is the output-voltage feedback pin. This pin is connected to the inverting input of the internal error amplifier. 1.26V reference is internally connected to the non-inverting input of the error amplifier. The output voltage $V_{OUT}$ is calculated by the following equation.

$$V_{OUT} = 1.26V \times (R5 + R6)/R6$$

R5 in Fig. 4.21 corresponds to 12.01kΩ (R900+R808) of this design as shown in Fig. 4.19, and similarly R6 corresponds to 1kΩ (R809) of this design, and therefore $V_{OUT}$ is 16.4V.

### 4.6.2. 48V or 16.4V to 12V Step Down

12V power generation from 48V or 16.4V uses a buck switching regulator IC LM5010A-Q1 (Texas Instruments) (Hereinafter referred to as "12V generation IC"). Fig. 4.22 shows the basic circuit using the 12V generation IC. Refer to LM5010A datasheet and related documentation for more information on 12V generation IC.

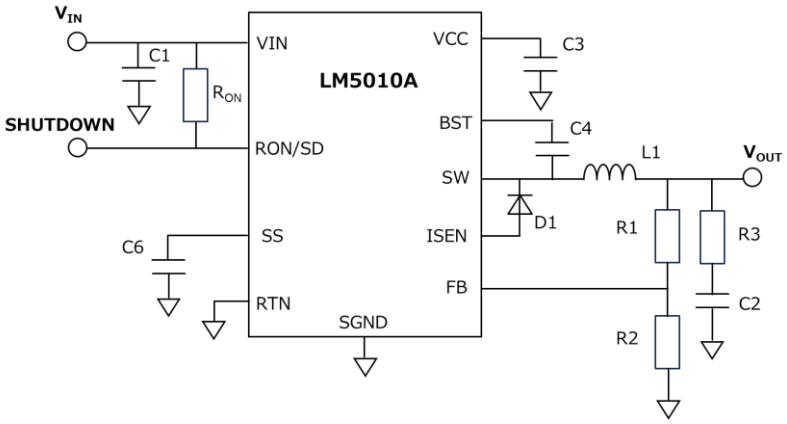



**Fig. 4.22 12V Generation IC Basic Circuit**

The power supply $V_{OUT}$ is calculated by R1 and R2 in Fig. 4.22 using the following equation.

$$V_{OUT} = 2.5V \times (R1 + R2)/R2$$

R1 in Fig. 4.23 corresponds to 6.81kΩ (R814+R819) of this design as shown in Fig. 4.19 and R2 corresponds to 1.8kΩ (R815) of this design, and therefore $V_{OUT}$ is 11.96V.

### 4.6.3. 5V Power Generation for MCU

From the above 12V, a buck converter IC TPS629210 (Texas Instruments) (hereinafter referred to as "5V generation IC") is used to generate 5V power supply for MCU. Fig. 4.23 shows the basic circuit using 5V generation IC. Refer to tps629210 datasheet and related documentation for more information on 5V generation IC.

The voltage at FB pin is adjusted to 600mV and the output voltage $V_{OUT}$ is calculated by the following equation.

$$V_{OUT} = 0.6V \times (R1 + R2)/R2$$

R1 in Fig. 4.23 corresponds to 264kΩ (R670+R671) of this design as shown in Fig. 4.20, R2 corresponds to 36kΩ (R673) of this design, and therefore $V_{OUT}$ is 5V.

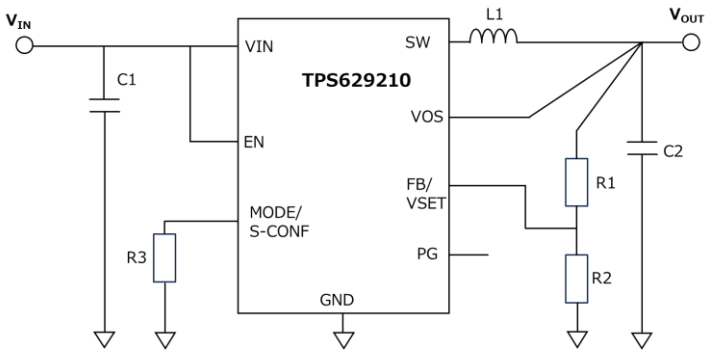



**Fig. 4.23 5V Generation IC Basic Circuit**

### 4.6.4. 1.2V, 3.3V Power Generation for MCU

Converter IC TPS62420 (Texas Instruments) (hereinafter referred to as "1.2V/3.3V generation IC") with two built-in synchronous buck converters is used to generate 1.2V and 3.3V power supply for MCU from the above 5V. Fig. 4.24 shows the basic circuit using 1.2V/3.3V generation IC. Refer to TPS62420 datasheet and related documentation for more information on 1.2V/3.3V generation IC.

The output voltage $V_{OUT1}$ of converter 1 is calculated by the following equation.

$$V_{OUT1} = 0.6V \times (R11 + R12)/R12$$

The output voltage $V_{OUT2}$ of converter 2 is calculated by the following equation.

$$V_{OUT2} = 0.6V \times (R21 + R22)/R22$$

R11 in Fig. 4.24 corresponds to 337.5kΩ (R675+R676) of this design as shown in Fig. 4.20, equivalent to, R12 corresponds to 75kΩ (R677) of this design, and therefore $V_{OUT1}$ is 3.3V.
Similarly, R21 corresponds to 200kΩ (R678), R22 corresponds to 200kΩ (R679), and therefore $V_{OUT2}$ is 1.2V.

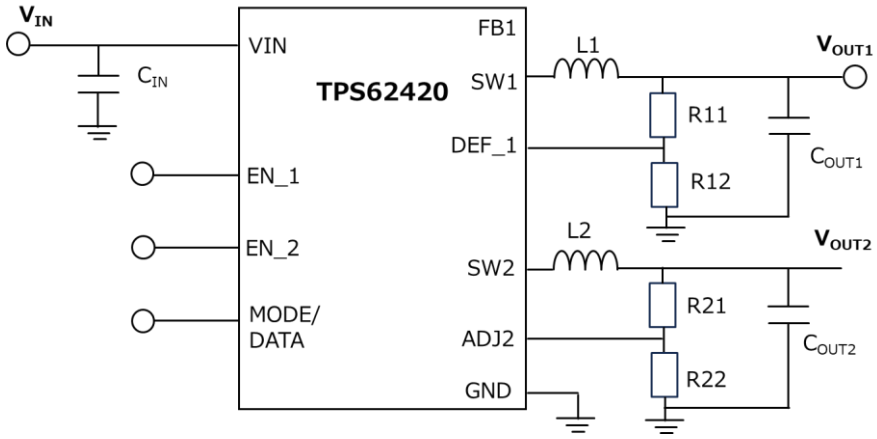



**Fig. 4.24 1.2V/3.3V Generation IC Basic Circuit**

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