TC78B002FTG/FNG
Usage considerations

Rev. A

Summary

The TC78B002FTG/FNG is a single phase full-wave driver for fan motor. It has a DMOS device in an output transistor.

A highly effective drive is possible by adopting a DMOS output driver with low ON resistance and a PWM drive system.

This is a reference.
Please do not determine the final equipment design by this material.

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1. Power Supply Voltage

Power supply voltage should be applied to VM terminal of the IC in using the TC78B002FTG/FNG.
Please use the IC within the range of 3.5 to 16V although the absolute maximum rating of VM power supply voltage is 18V.

Table 1.1 Power supply voltage usage range

Characteristic	Symbol	Operating voltage range	Unit
Normal operating voltage range	VM_{opr1}	5.5 to 16	V
Low voltage operating voltage range	VM_{opr2}	3.5 to 5.5	V

Note: The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.

Output incorporates the PWM control function. Duty of the output PWM is controlled by VSP voltage, and the rotation speed of the motor can be controlled. In using the PWM control function, please configure the VM power supply voltage within the "normal operation voltage range".
In case of using the IC for the application that adjusts the rotation speed of the motor by power-supply-voltage control, not using the PWM control, the "low voltage operating voltage range" is provided in order to take the wider range of adjustable power supply voltage. In using the VM power supply voltage in the "low voltage operating voltage range", please pull-up the VSP terminal to Vreg.

[Notes in using the IC in the range of power supply voltage for low-voltage operation]
In low-voltage operation, electrical characteristics, such as output resistance, change compared with those under the condition that VM is 12 V. For details, please refer to the applicable portion of the reference data of the electrical characteristics in the technical data sheet.
In low-voltage operation, the reference voltage of the A/D conversion circuit inside the IC also becomes low with the fall of Vreg power supply voltage. When the voltage for IC control terminal is provided by resistive dividing from Vreg voltage, the result of A/D conversion has almost no change. However, when the voltage is inputted directly from the outside, the result of the conversion may change. Especially, when the VSP terminal voltage is inputted externally, output duty may change in the low-voltage operation. In case of pulling-up the VSP terminal voltage to Vreg, the output duty is fixed to the full duty and there is no problem.
Because output duty in the startup of the IC is fixed to 50%, there is a possibility not to start if the power supply voltage is low and the torque in startup is not enough. In that case, please increase the power supply voltage and start up.

[Measure against rise of VM terminal voltage by motor regeneration current]
VM terminal voltage may rise by the regeneration current of the motor. Especially, when the reverse connection preventive diode is applied, VM terminal voltage rises because the current cannot be regenerated to the power supply. Please use the IC in paying attention that VM terminal voltage does not exceed the absolute maximum rating including the voltage rise by regeneration current.
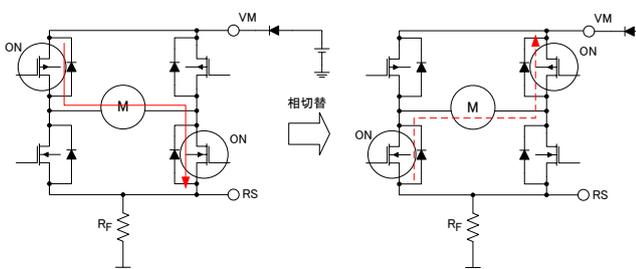
Figure 1.1 Rising VM terminal voltage by the motor regenerating current in phase shift
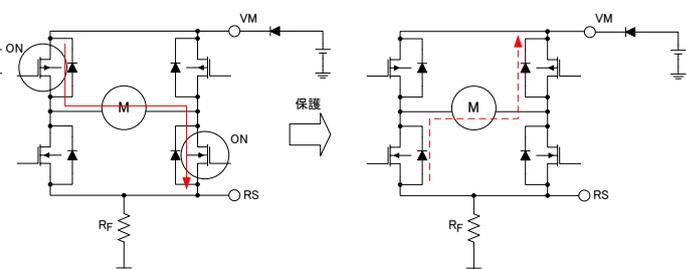
Figure 1.2 Rising VM terminal voltage by the motor regenerating current when all output stages are off by protection function

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The current flowing through the motor can be reduced before the phase shift by using the soft switching function. The voltage rise in the phase shift can be suppressed by reducing the regeneration current to zero.

Moreover, the term of PWM OFF is provided before all output stages are turned off in order to suppress the voltage rise by regeneration current. The regeneration current of the motor is decayed by low side regeneration during the term of PWM OFF. However, when abnormalities, such as power supply shutdown, occur during motor rotation, regeneration current cannot decay. In this case, please add a capacitor, a zener diode, or both to VM terminal in order to absorb the regeneration current to the power supply line and suppress the voltage rise by regeneration current up to 16V. Zener diode can suppress the voltage rise by the regeneration current and also can protect the circuit even when the external input voltage is over voltage. In case of using the zener diode, the range of the zener voltage should be normal operation voltage to 16V. So, the current does not flow into the zener diode in normal operation.

Add capacitor   Add zener diode   Add both capacitor and zener diode
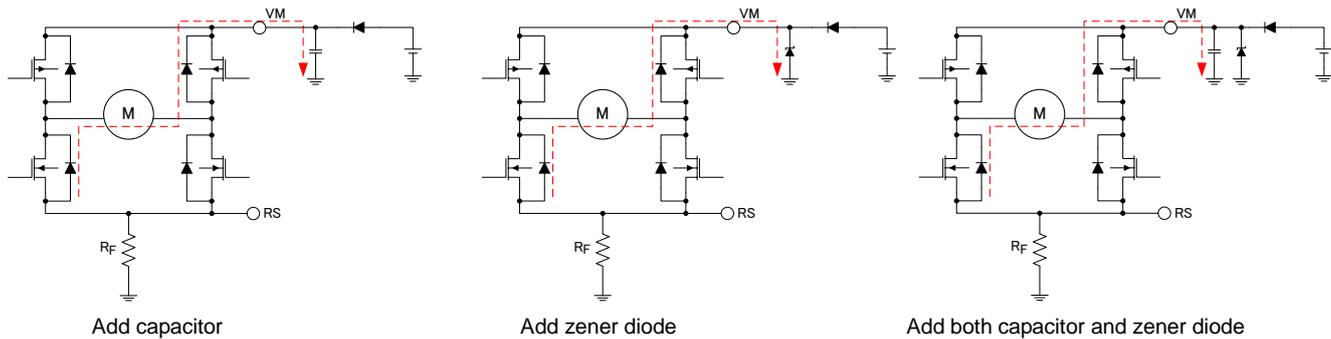
Figure 1.3 Measure for rise of VM terminal voltage

This IC is a single power supply and there is no procedure in particular for applying power supply or for shutting down. When the rotation speed of the motor is controlled by inputting VSP voltage from the exterior, it will become a cause of abnormal operation if the motor is operated under unstable power supply voltage. So, it recommends inputting VSP voltage and operating the motor after VM power supply voltage becomes stable.

When the motor operates by pulling up VSP voltage to Vreg, there is no problem since VSP voltage is generated inside the IC.

It is recommended to shut down the power supply after the motor stops because the voltage of VM terminal from the regeneration current of the motor may rise at the time of power-supply shutdown. When the motor is used by pulling up the VSP voltage to Vreg, or when the minimum output duty is configured, please check that the voltage of VM terminal does not exceed absolute maximum rating at the time of power supply shutdown.

Please do not apply voltage from the exterior since Vreg power supply voltage is generated from the regulator inside the IC. Please connect the capacitor for power supply stable of 0.1μF to a Vreg terminal. Moreover, in operating the IC, please ensure Vreg voltage is 5.5V or less on the basis of the GND terminal of the IC. Please place the capacitor for power supply stable near the IC. Please wire not to exist route of switching current between GND of the capacitor and IC GND terminal. Please refer to "7. Notes in designing board" for details.

Although Vreg power supply voltage can be used as the bias voltage of a hall device, or voltage of IC control terminal by resistive dividing, please do not draw the current beyond the capability of an internal regulator. Please use output current within 10 mA of absolute maximum rating.

2. Output Current

The absolute maximum rating is 1.5A. It is a set of rating that must not be exceeded, even for a moment. As for the rush current in starting up motor, the current in lockout, and so on, do not exceed any of these absolute maximum ratings. Available average output current changes depending on the usage conditions (ambient temperature, mounting board method, and so on). Design the IC with the margin that T_j does not exceed 150°C. Please refer to "8. Power consumption" and "9. Power dissipation".

3. Input Signal

3.1. VSP and VMI input

Output Duty is controlled by the voltage of VSP and VMI terminals through 7-bit AD convertor.

The voltage of VSP terminal is digitized by 7-bit AD and controls the output PWM duty with the internal logic by using the data. The relation between the input voltage of VSP terminal and the output duty is shown below.

0	≤ VSP ≤	$V_{AD (L)}$	→	Duty = 0%	(VSP, Result of AD conversion 0 to 16)
$V_{AD (L)}$	< VSP ≤	$V_{AD (H)}$	→	Figure3.1	(VSP, Result of AD conversion 17 to 116)
$V_{AD (H)}$	< VSP ≤	V_{REG}	→	Duty = 100%	(VSP, Result of AD conversion 117 to 127)
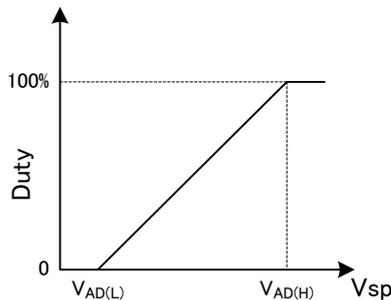
Note: The output duty changes in steps of 1% corresponding to 100 steps of the voltage from V_{SP} ($V_{AD (L)}$ to $V_{AD (H)}$).

Figure 3.1 Relation between the voltage of VSP and output duty

VAD (L) =0.55V (typ.) VAD (H) =3.9V (typ.)

When the voltage of VAD (L) or more is applied to VMI terminal, the minimum output duty is configured. The relation between input voltage of VSP terminal and output duty is shown below.

0	≤ VSP ≤	VMI	→	Gained duty under the condition that VSP equals VMI in Figure3.1
VMI	< VSP ≤	$V_{AD (H)}$	→	Figure3.1
$V_{AD (H)}$	< VSP ≤	V_{REG}	→	Duty = 100%
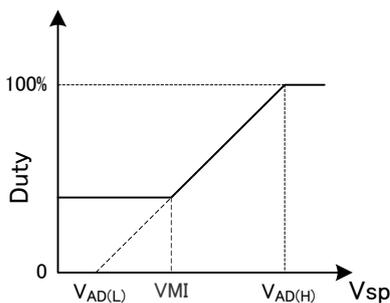
Figure 3.2 Relation between the voltage of VSP terminal and output duty in VMI setting

Input voltage of VMI terminal should be provided from divided voltage of VREG terminal.

A motor starts when either VSP terminal voltage or VMI terminal voltage exceeds 0.55V.
In starting, output duty is fixed to 50% until the frequency of the hall signal becomes 5Hz or more. If it becomes 5Hz or more, output duty changes by VSP voltage and VMI voltage. The example of a waveform in startup is shown in Figure. 3.3.

Rush current can be also suppressed in motor startup even when VSP voltage is high because the output duty in startup is fixed to 50%. Moreover, when power supply voltage is low, starting torque is not enough and may be unable to start although it has some starting torque. In case of starting with low power supply voltage, please evaluate enough.

Figure 3.3 Operation waveform in output start (Output in startup Duty=50%)

If both VSP terminal voltage and VMI terminal voltage become 0.55V or less, the output for driving the motor is turned off. The term of PWM OFF is provided before all output stages are turned off. During the term of PWM OFF, the regeneration current of the motor is decayed at bottom regeneration. Therefore, when all output stages are turned off, the regeneration current to a power supply can be reduced. The example of a waveform is shown in Figure. 3.4.
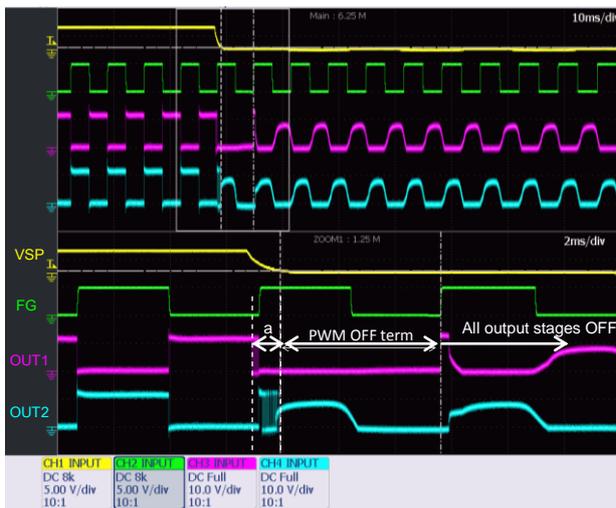
Figure 3.4 Operation waveform in output OFF

Note: Output duty changes with fall of VSP terminal voltage during term of 'a'

3.2. VSOFT and VOFF input

Soft switching function of the IC can be controlled by the voltages of VSOFT and VOFF terminals.

Soft switching function inserts OFF term and soft switching term before and after the conductive-phase switching. Soft switching function is effective to reduce motor vibration and reduce the VM voltage rise in phase shift.

When the voltage of VSOFT terminal is higher than that of VOFF terminal, the electrical angle of all terms (OFF term and soft switching term) are determined by the voltage of VSOFT terminal. The electrical angle of OFF term is determined by the voltage of VOFF terminal.

When the voltage of VSOFT terminal is lower than that of VOFF terminal, soft switching term is not provided. Only the OFF term is provided. The electrical angle of OFF term is determined by the voltage of VOFF terminal.

The voltages of VSOFT and VOFF terminals are digitized through 7-bit AD convertor. Soft switching is controlled by digitized values in the internal logic IC.

Input voltage to VSOFT terminal and VOFF terminal should be supplied by resistive dividing voltage from VREG terminal voltage.

Example 1: VSOFT=0, VOFF=0V
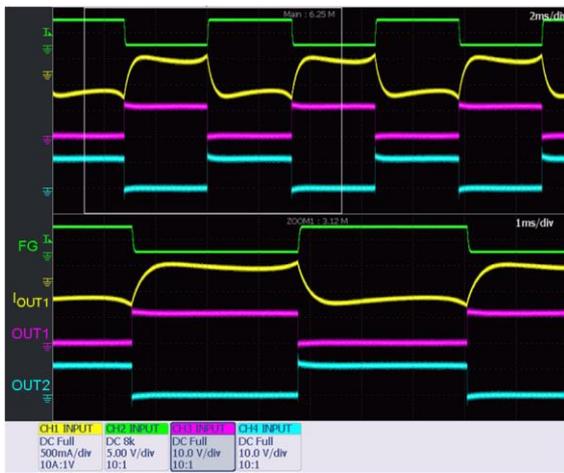
Figure 3.5 Operation waveform of the IC (Without soft switching)

Example 2: VSOFT=1.55V, VOFF=0V

Figure 3.6 Operation waveform of the IC (Soft switching term: 30.9°)

Example 3: VSOFT=0V, VOFF=1.55V
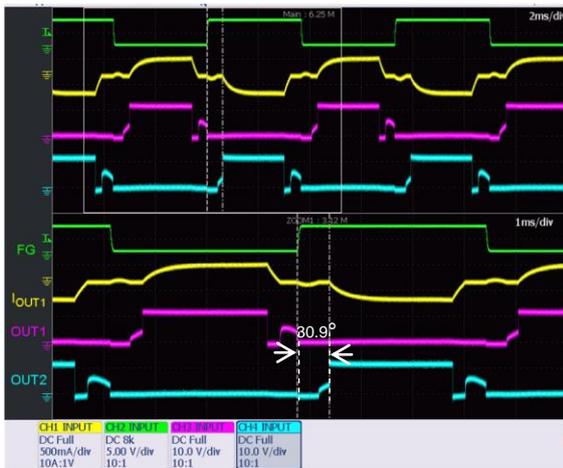
Figure 3.7 Operation waveform of the IC (OFF term: 30.9°)

Example 4: VSOFT=2.40V, VOFF=0.9V
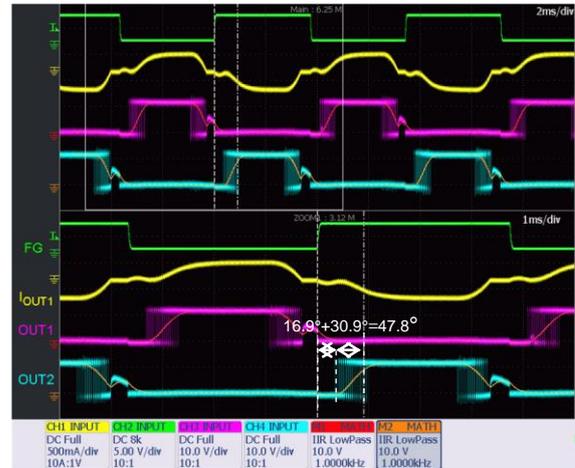
Figure 3.8 Operation waveform of the IC (Soft switching term: 30.9°, OFF term: 16.9°)

3.3. LA input

Lead angle of the conducting signal can be set in up to 22.5° against the hall signal. The phase of motor current and the phase of motor induction voltage can be matched by lead control. The efficiency of the motor can be improved.

Example 1: LA=0.9V
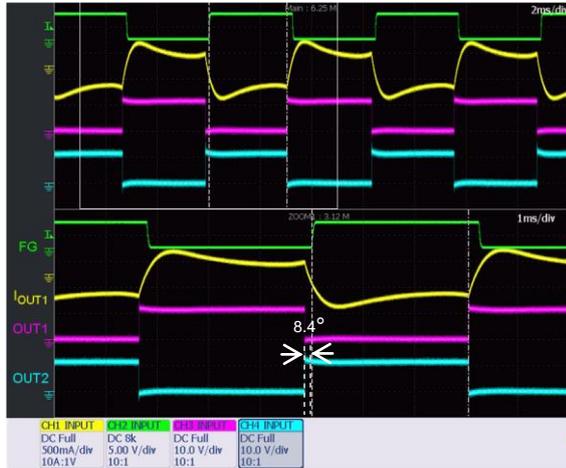
Example 2: LA=2.2V

Figure 3.9 Operation waveform of the IC (Lead angle: 8.4°)
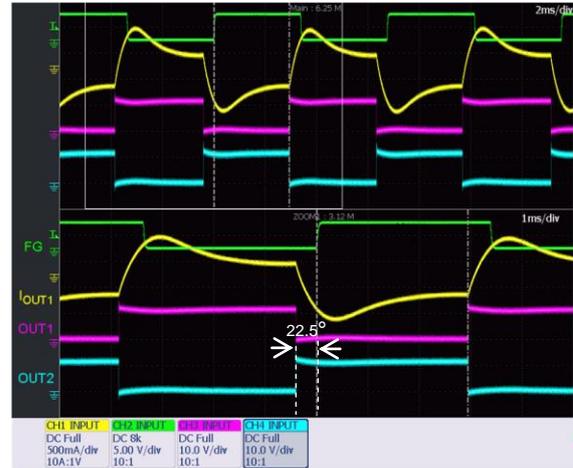
Figure 3.10 Operation waveform of the IC (Lead angle: 22.5°)

By combining the soft switching term and OFF term, the regeneration current before switching conduction phase is reduced by the configuration of the lead angle, and the current flows through the motor immediately after switching phase.

Example 3: VOFF=0.9V, LA=1.7V
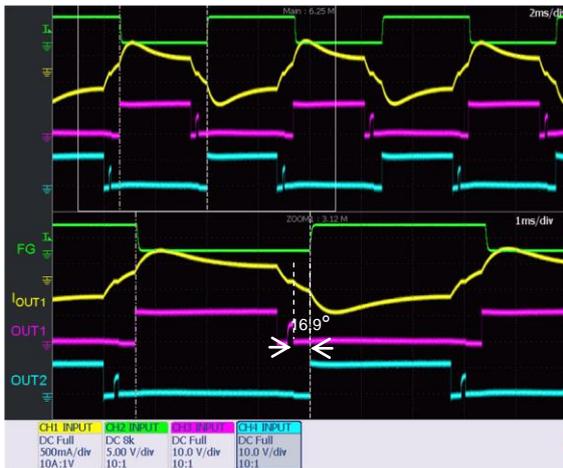
Figure 3.11 Operation waveform of the IC (OFF term: 16.9°, Lead angle: 16.9°)

Input voltage for LA terminal should be provided from divided voltage of VREG terminal.

4. Protection circuit

This IC builds in the following functions. The IC is not protected by any cases.
Please be sure to use the IC within the absolute maximum rating. The IC may be destroyed by short-circuiting between outputs, air contamination faults, or faults due to improper grounding before circuit operation.

4.1. Lock protection (Internal oscillation frequency: 10MHz, Normal rotation)

It operates when the zero cross of the hall signal cannot be detected for 0.4s or more in motor rotation. Whether the zero cross of the hall signal is detected or not is monitored by FG signal. When the zero cross is detected, output level of FG signal changes. When the level of FG signal does not change for 0.4s or more, the motor operation state is considered as lock.

The state of FG signals changes when the zero cross of the hall signal is detected regardless of the lock protection.

The output for driving the motor turns off after lock protection. It restarts automatically 4 seconds after lock protection. In automatic restart, it starts from 50% of the output duty which is the same as the normal startup. When it restart automatically without lock released, the lock protection operates again 0.4 second after output start, and the operation of 4s-stopping and 0.4s-operating is repeated until the lock is released.

RDO signal indicates the lock state of the motor. It outputs "H" in recognizing the lock state. When the zero cross of the hall signal is detected twice after the output starts by automatic restart, RDO signal outputs "L."

Lock detection time and the time for automatic restart depend on the internal oscillating frequency. Please refer to "5. Oscillating circuit" for details.

During the lock protection, quick start is performed when VSP voltage is set 0.55V or less and set 0.55V or more again after 10ms of VSP signal response time (max) externally.
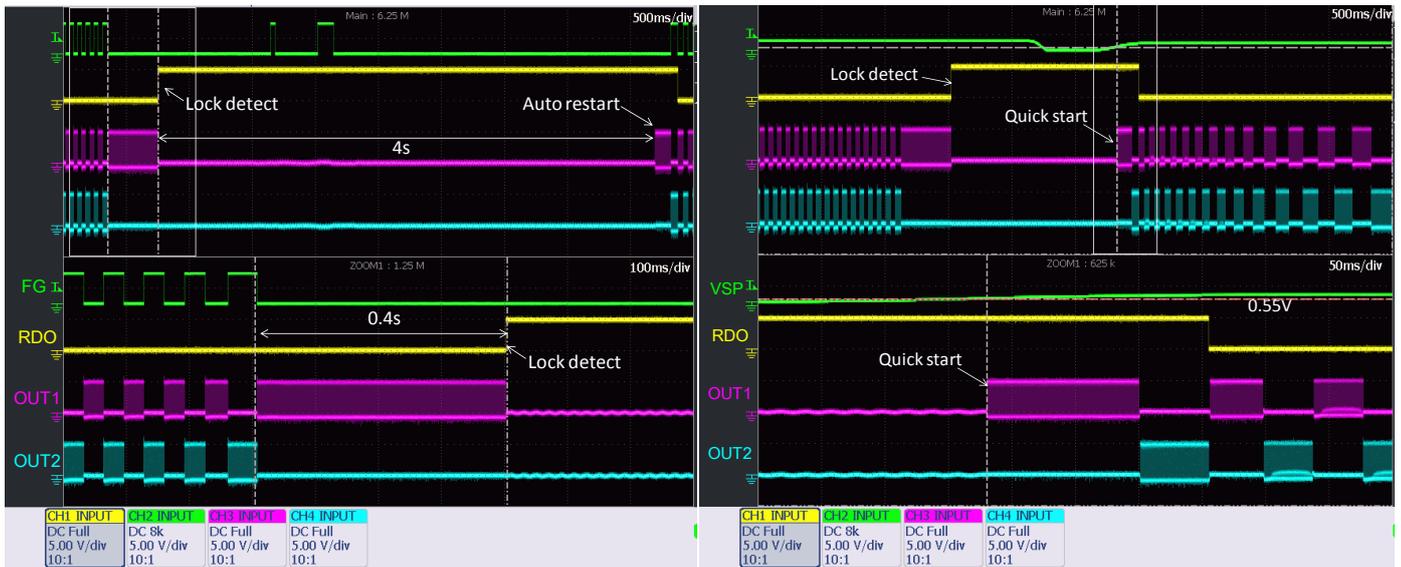
Figure 4.1 Operation waveform of lock protection   Figure 4.2 Operation waveform of quick start

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4.2. Lock detection time (Internal oscillation frequency: 10MHz)

In normal rotation, internal counter is reset at the edge of FG and the lock detection is performed after 0.4 second.
Only in starting, the lock protection may operate in 0.2 second (min) because no reset signal from FG.
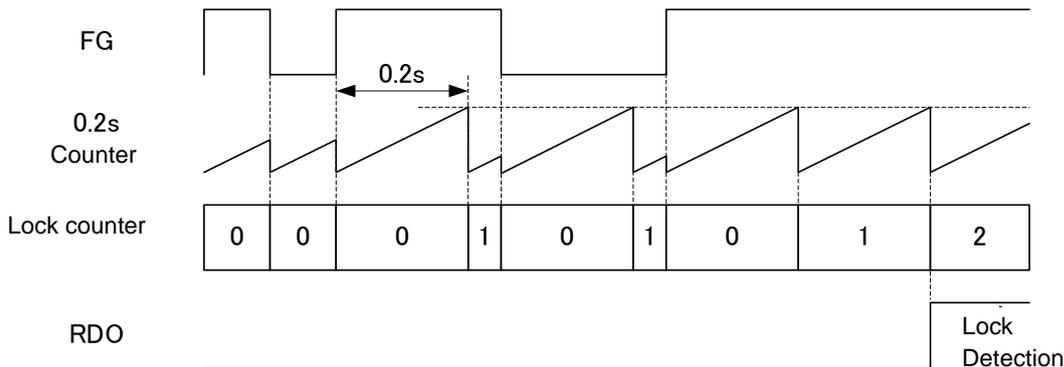
Figure 4.3 Lock detection time in normal rotation

When lock detection does not work in normal rotation, the counter for 0.2s is reset at the edge of FG.
When the edge of FG is not recognized, the counter for 0.2s overflows after 0.2 second. If the counter for 0.2s overflows, the lock counter counts up. Lock detection is performed when the counter value of the lock counter becomes 2. Therefore, the timing of lock detection becomes 0.4 second after the last edge of FG.
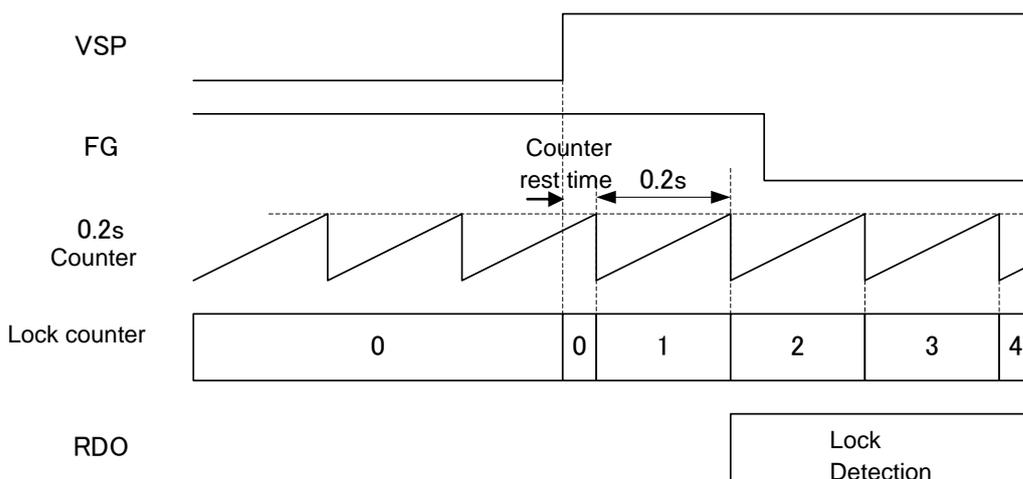
Figure 4.4 Lock detection time in startup

When VSP is 0.55V or less and the output for the motor drive stops, the lock counter is fixed to 0, but a counter for 0.2s is counted up normally.
The lock counter can be counted up if VSP rises 0.55V or more. Since the count of the counter for 0.2s has already progressed at the timing which VSP rises 0.55V or more, the lock detection time is as follows; counter remaining time (0 to 0.2 second). + 0.2 second. When the edge of FG is not recognized by the lock detection time, the lock protection operates.
After the lock protection, when it starts again automatically, lock detection time is 0.4 second because the rebooting timing is interlocked with the counter for 0.2s.
In using a quick start, lock detection time is 0.2 to 0.4 second equivalent to that of startup.
When lock detection time is too short to startup, starting function can be improved by increasing the power supply voltage in starting, or setting up internal oscillating frequency low. Please refer to "5. Oscillating circuit" for the details of internal oscillating frequency.

4.3. Current Limit

Resistance (R_F) detects the motor current. When the voltage of resistance (R_F) corresponds to the current limit detection voltage (V_{RS}=0.3V (typ.)), the current limit circuit works.

Current value in which the current limit circuit operates (I_{OUT}) = Over-current detection voltage (V_{RS})/Detection resistance (R_F)

Current limit circuit operates under the following condition; I_{OUT}=0.3V (typ.)/0.62Ω=484mA when R_F=0.62Ω

However, the mask term is provided for 1.5µs since output PWM has turned on for the measure against a noise of RS terminal. Even if RS terminal voltage exceeds 0.3V during the mask term, the current limit circuit does not operate.

When the current limit circuit operates, an upper output power transistor is turned off and the output PWM is turned off. A current limit is canceled in the timing of the peak of the following internal triangular wave, an upper output power transistor is turned on in the timing of the internal PWM ON, and output returns.
When output duty is less than 100%, the duty of the output PWM may be seemed to change depending on the operation of the current limit circuit. An image of operation is shown in Figure 4.5.
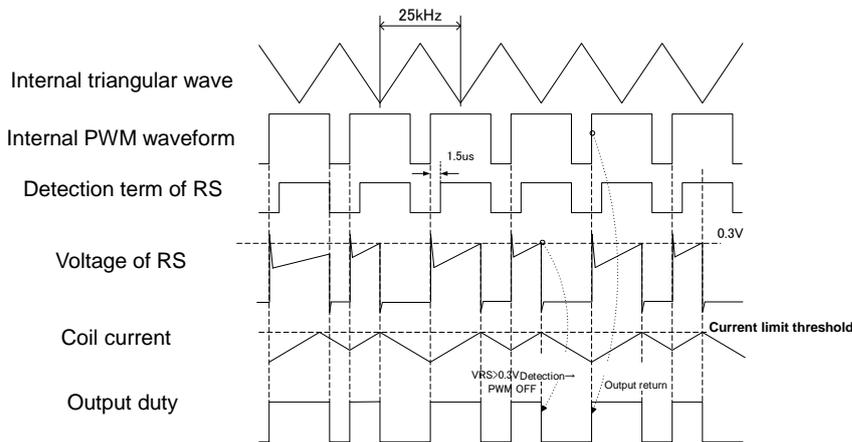
Figure 4.5 Operation image of current limit in case output duty is less than 100%

When the output duty is 100%, the timing of an output return corresponds to the timing of the peak of an internal triangular wave. The frequency of the output PWM may be seemed to change by the timing of current limit detection and the timing of recovering.
As shown in Figure 4.7, PWM frequency is set to 12.5 kHz (or 1 for the integer of 25 kHz) when the time from a return to current limit detection is longer than one cycle of the internal triangular wave. When the frequency of PWM is 20 kHz or less, it becomes a cause of an audible noise because it is in the auditory range.
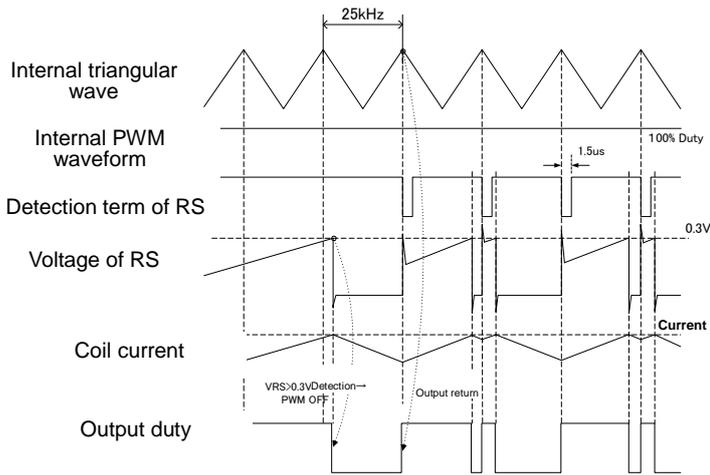
Figure 4.6 Operation image of current limit when output
        duty is 100% (1)
        Duty of the output PWM changes.
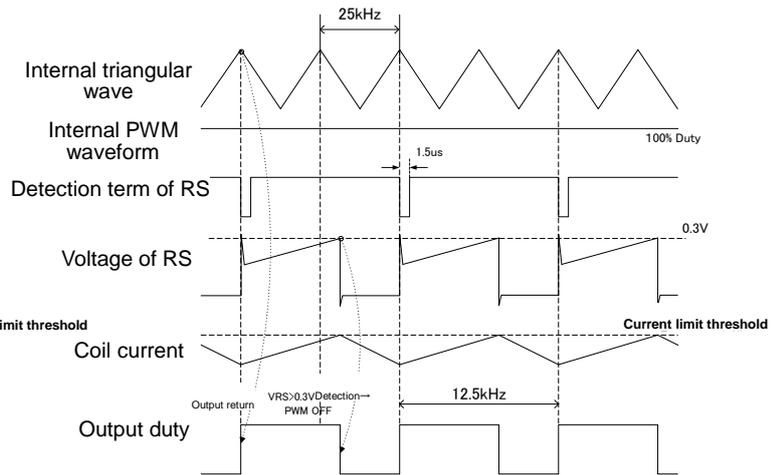
Figure 4.7 Operation image of current limit when output
        duty is 100% (2)
        The frequency of the output PWM changes.

ON term may be changed with the integral multiple of the switching cycle by the operation of the current limit circuit. This is called a subharmonic oscillation.

(Reference)
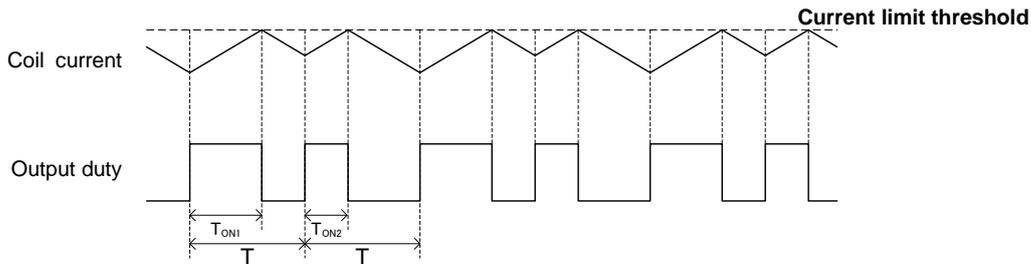
Figure 4.8 Image of output waveform in generating subharmonic oscillation

The subharmonic oscillation is based on the principle of current limit operation, and is not abnormal operation. By subharmonic oscillation, the frequency component of one for the integer of PWM frequency may generate, and it may become a cause of an audible noise.

Please judge the influence of the audible noise generated by the current limit operation on actual use after evaluation.

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4.4. Over Current Protection (ISD)

Each current flowing through four power transistors is detected individually. When the current exceeds the detection value, all output power transistors are turned off 1ms (typ.) after the related output power transistor is turned off.

<Outputs short to power supply>
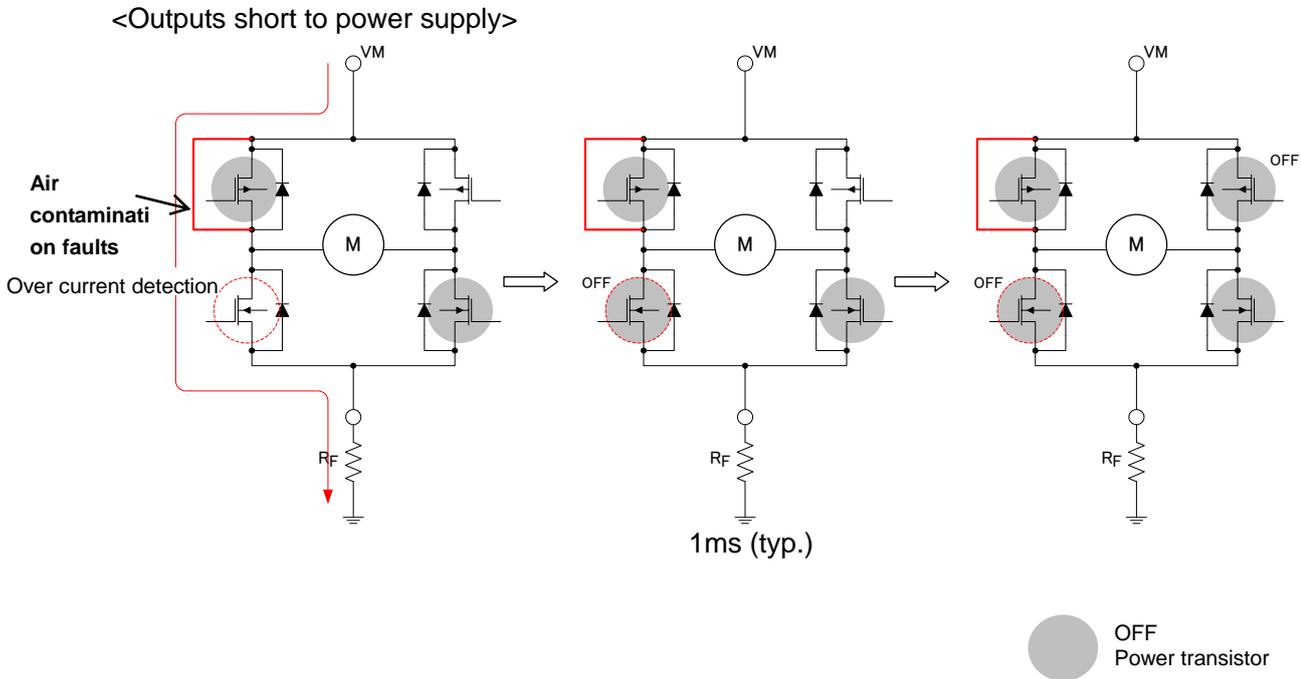
Figure 4.9 Operation image of outputs short to power supply

<Outputs short to ground>
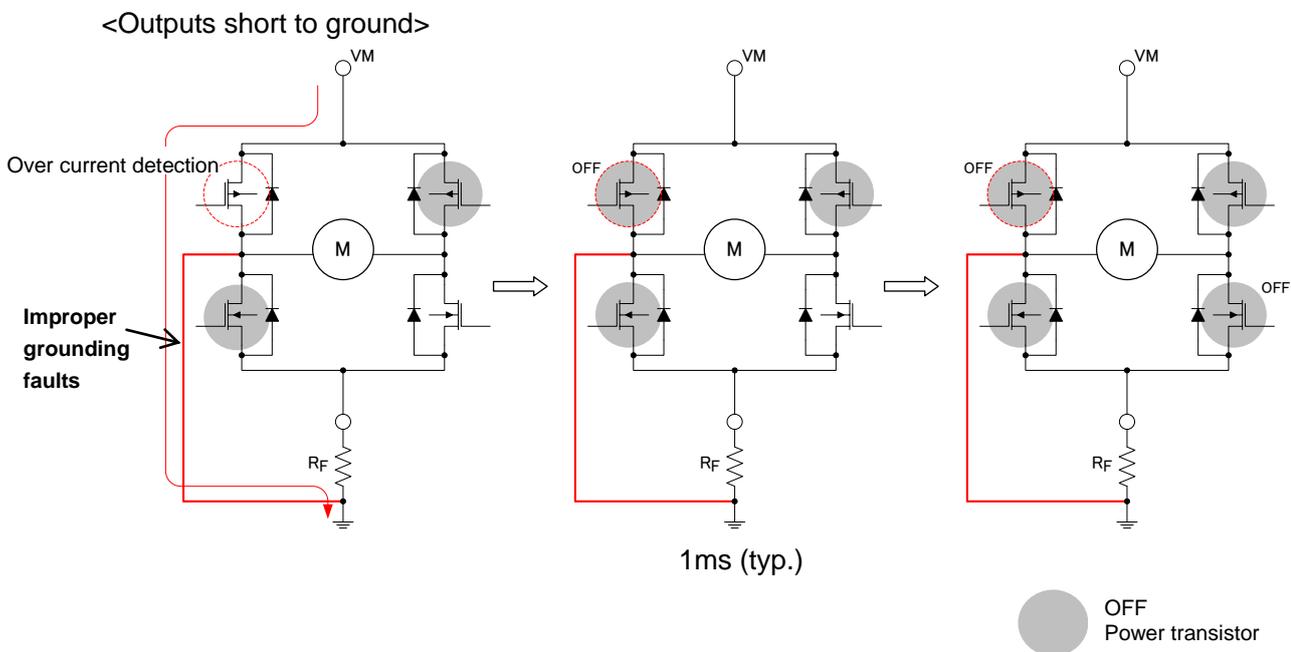
Figure 4.10 Operation image of outputs short to ground

Timer is incorporated in this circuit. The motor operation resumes from OFF state 100ms (typ.) after the over current is detected. When state of over current continues, the operation of OFF and auto-resume repeat. In case this protection (ISD) operates 8 times repeatedly, the motor operation does not resume automatically. The output power transistor keeps turned off. In order to clear this state, VSP or the power supply should be applied again.

<Operation of outputs short to power supply (Example)>
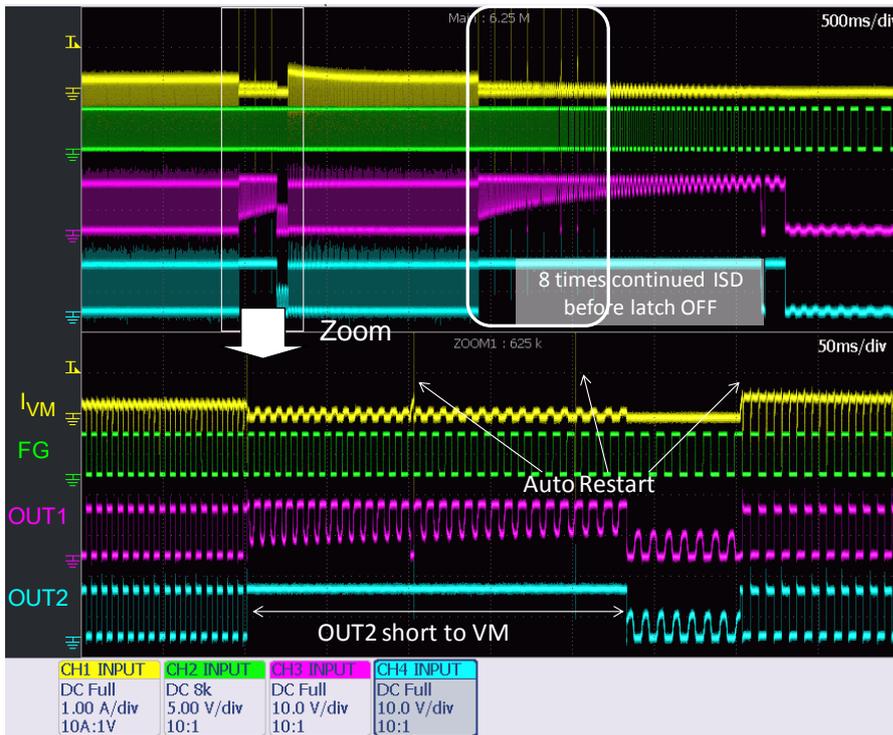
Figure 4.11 Operation example of outputs short to power supply

< Operation of outputs short to ground (Example)>
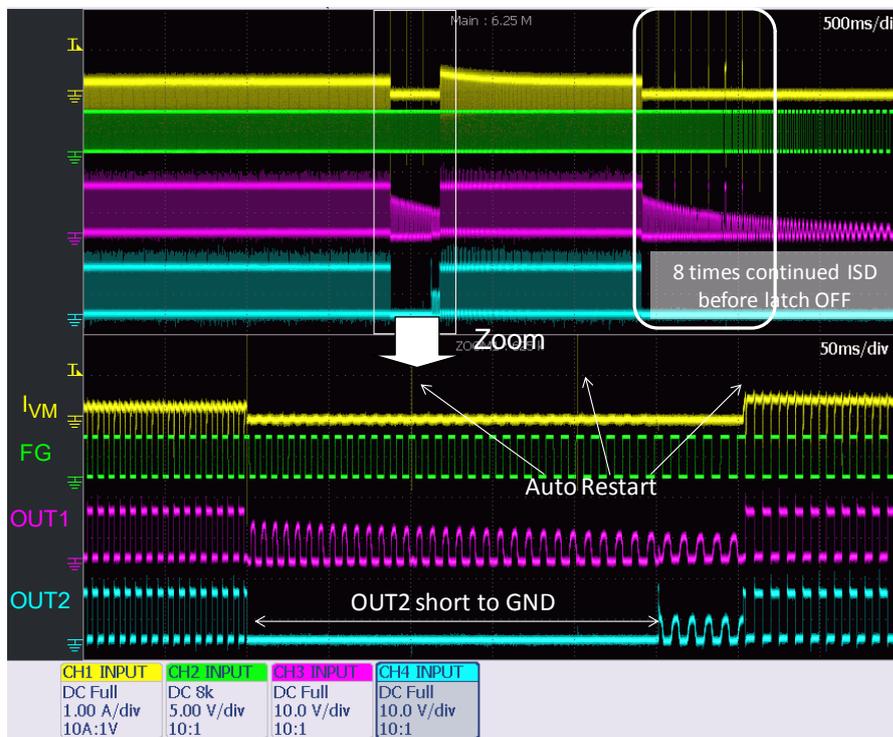
Figure 4.12 Operation example of outputs short to ground

4.5. Thermal Shutdown Circuit (TSD)

Thermal shutdown circuit (TSD) operates when T_j rises to 170°C (typ.) or more. All output power transistors are turned off after a 1ms (typ.) PWM OFF term during which upper output power transistor is turned off.

The operation resumes when the temperature falls to 130°C (typ.) or less.

4.6. Under Voltage Lockout Protection (UVLO)

The power supply voltage of VM and the voltage of VREG are monitored. When each of them falls to 2.9V (typ.) or less, it is recognized as low voltage and the circuit is turned off. The normal operation resumes when both voltage recovers to 3.2V (typ.) or more.

5. Oscillation Circuit (OSC)

Reference clocks are generated internally by connecting the external resistance (R_{OSC}) to OSCR terminal and oscillating CR.
Equivalent circuit of oscillation circuit is shown in Figure5.1.
Oscillation frequency is approximated by below formula.

$$f_{OSC} = Iref/ (2 \times C \times Vref) = (Vref/R_{OSC}) / (2 \times C \times Vref) = 1/ (2 \times C \times R_{OSC})$$

C: Equivalent capacitor of internal IC C=2.08pF (typ.)
$R_{OSC:}$ External resistance of OSCR terminal

When external resistance is 24kΩ, oscillation frequency is calculated as follows;
f_{OSC} = 1 / (2 × 2.08e-12 × 24000) = 10MHz (typ.)
When external resistance is 39kΩ, oscillation frequency is calculated as follows;
f_{OSC} = 1 / (2 × 2.08e-12 × 39000) = 6.2MHz (typ.)
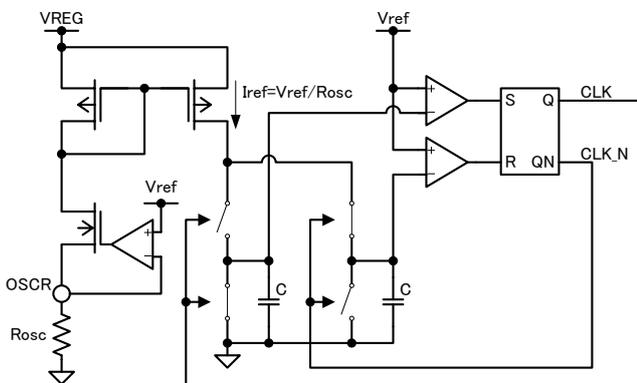
Figure 5.1 Equivalent circuit of oscillation circuit
Note: The equivalent circuit diagrams may be simplified or
some parts of them may be omitted for explanatory purposes.
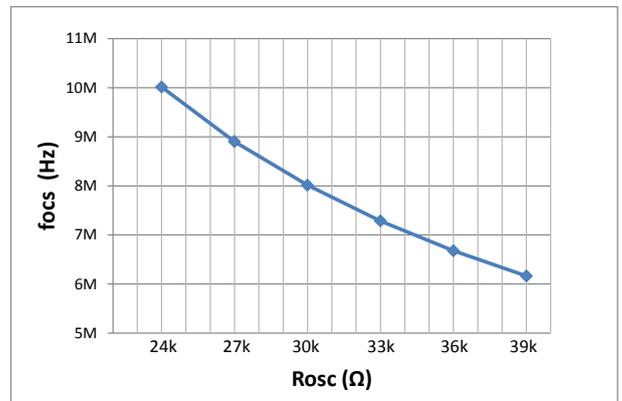
Figure 5.2 Relation between external resistance and
oscillation frequency (typ.)

The operation range of the IC is 5 to 12 MHz. The variation in the oscillation circuit inside the IC is about ±20%. Please configure the external resistance between 24kΩ to 39kΩ in consideration of this variation. Accuracy of the applied external resistance should be less than ±1%.
When the value of the external resistance is large, please connect the resistance to the IC as close as possible not to be influenced by the noise from the outside. Please refer to "7. Notes in designing board" for details.
When oscillation frequency is changed by changing the constant value of the external resistance, the characteristic depending on internal clocks, such as output PWM frequency and lock detection time, is also changed. Please refer to Table 5.1 for the characteristic changed when Rosc is 24kΩ and 39kΩ.

Table 5.1 Characteristics changed by Rosc

Changing characteristics		Rosc = 24kΩ			Rosc = 39kΩ		
		min	typ.	max	min	typ.	max
Internal oscillating frequency	f_{OSC}	8MHz	10MHz	12MHz	5.0MHz	6.2MHz	7.4MHz
PMW frequency	f_{PWM}	20kHz	25kHz	30kHz	12.5kHz	15.5kHz	18.6kHz
ON term of lock detection	T_{ON}	0.32s	0.4s	0.48s	0.5s	0.65s	0.8s
OFF term of lock detection	T_{OFF}	3.2s	4s	4.8s	5s	6.5s	8s
ON term of lock detection in starting.	$T_{ON(min)}$	0.16s	0.2s	0.24s	0.25s	0.32s	0.4s
VSP signal response time	T_{VSP}	—	—	10ms	—	—	20ms
Mask time of current limit detection	T_{mask}	1.2μs	1.5μs	1.8μs	1.9μs	2.4μs	3.0μs
Mask term of over-current shutdown circuit	$T_{ISDMASK}$	1.6μs	2μs	2.4μs	2.5μs	3.2μs	4.0μs
OFF term of over-current shutdown circuit	T_{ISDOFF}	80ms	100ms	120ms	125ms	160ms	200ms
Soft switching frequency		4Hz	5Hz	6Hz	2.5Hz	3.1Hz	3.7Hz
PWM OFF term for boosting prevention		0.8ms	1ms	1.2ms	1.3ms	1.6ms	2ms
Digital filter time of hall input		20μs	25μs	30μs	32μs	41μs	50μs

When low internal oscillating frequency is applied, please use the motor after enough check because the following characteristics are changed especially.

- PWM frequency becomes low. If it falls in the auditory range of 20kHz or less, it becomes a cause of an audible noise.

- ON term of the lock detection becomes long. Please check whether the rise in heat of a motor causes a problem or not in lock protection because the conducting time till the lock protection becomes long. The rise in heat of a motor can be suppressed by setting up a current limit threshold low.

- Mask time of current limit detection becomes long. In the mask term, even if the current exceeds the current limit threshold, the current limit circuit does not operate.

- Digital filter time of the hall input becomes long. Digital filter time is provided for the measure against a noise of a hall signal. Delay of a phase generates until the phase switching is recognized by the digital filter. This phase delay is dependent on the rotation speed of the motor.

When Rosc=24kΩ, Filter time is 25μs (typ.).
When 4-pole motor, and rotation speed is 3000RPM, phase delay is 0.9°.
When 4-pole motor, and rotation speed is 6000RPM, phase delay is 1.8°.
When Rosc=39kΩ, Filter time is 41μs (typ.).
When 4-pole motor, and rotation speed is 3000RPM, phase delay is about 1.5°.
When 4-pole motor, and rotation speed is 6000RPM, phase delay is about 3.0°.
When motor rotation speed is high, please use the motor by fully evaluating the influence of the phase delay.

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6. Application circuit (Example)
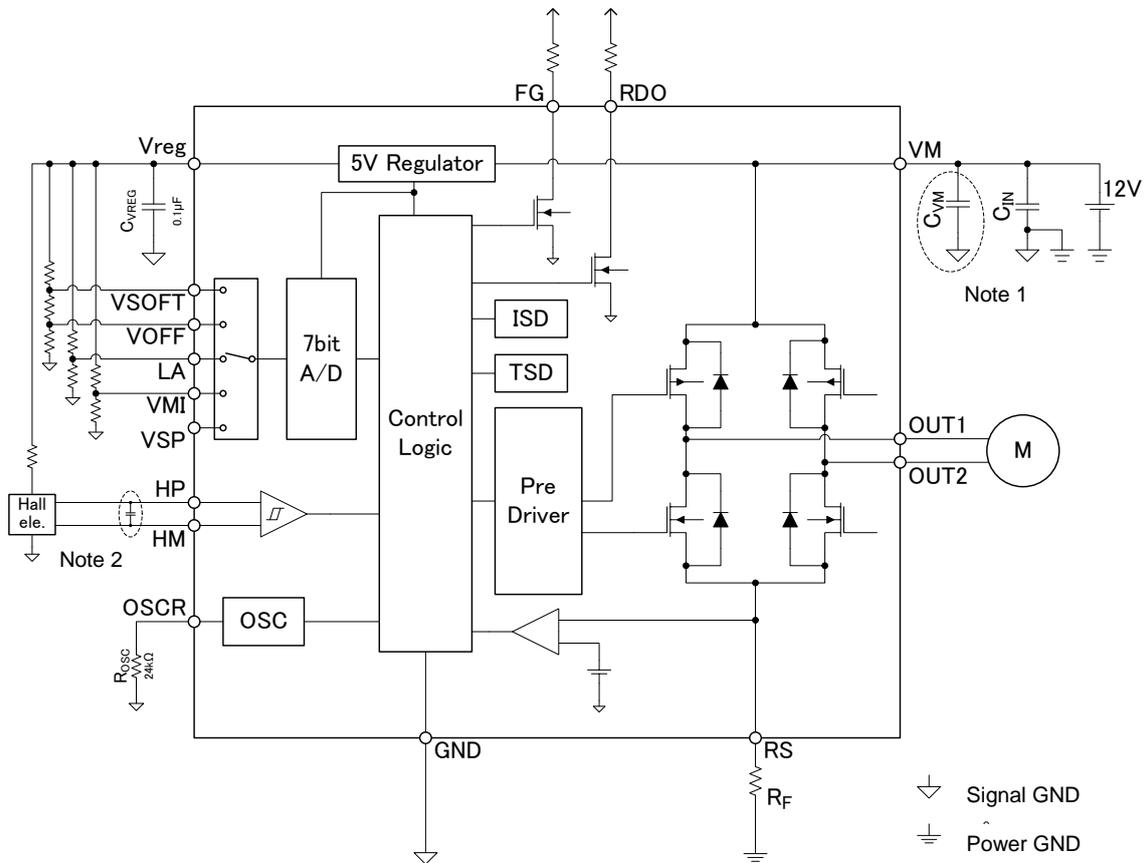
Notes 1: Please connect capacitor C_{VM} if needed for measuring for a high frequency noise.

Notes 2: Please connect the input capacitor of a hall signal if needed for preventing error detection by a noise.

Figure 6.1 Example of an application circuit

(1) Capacitor for power supply terminals

Please connect the appropriate capacitor to each terminal for power-supply-voltage stabilization and a noise reject. In addition, please connect the capacitor to the IC as close as possible. Especially, it is effective for the power supply variation in the high frequency range and the noise control by connecting a ceramic capacitor near the IC.

Item	Parts	Typ.	Recommended range
VM to GND (C_{IN})	Ceramics/electrolytic capacitor	10µF	2.2 to 22µF
Vreg to GND (C_{VREG})	Ceramic capacitor	0.1µF	0.1 to 0.47µF

Notes: It is possible using capacitors other than a recommendation value which exclude each part depending on the motor load conditions and the board pattern, etc.

It recommends arranging the capacitor between VM and GND within 10mm from the IC.
When the capacitor between VM and GND is arranged far from the IC on the board layout, and it cannot reduce the power supply variation generated in high frequency enough, it is recommended to add the capacitor (C_{VM}) of about 0.1µF near the VM and GND terminals of the IC.
Please design not to exist any route which flows switching current between the GND of the capacitor (between Vreg and GND) and the GND terminal of the IC. Please refer to "7. Notes in designing board" for details.

(2) GND

Please connect the GND terminal of the IC to signal GND. Please also connect the capacitor of Vreg terminal and the resistance of OSCR terminal to signal GND at the shortest. When the voltage of VSOFT, VOFF, LA, and VMI terminals are supplied from resistive divided voltage from Vreg voltage, please connect GND of divided resistance to the signal GND.

Please connect GND of shunt resistance (R_F) to the power GND.

Please one-point ground the signal GND and the power GND with the capacitor (C_{IN}). Please arrange the capacitor (C_{IN}) as close to the IC. Please refer to "7. Notes in designing board "for details.

(3) Shunt resistance

Pay attention for the ratings and select the appropriate resistor, which has enough margins because large current flows in the shunt resistor (R_F).

The maximum electric power on the shunt resistance during the motor operation is as follows; $P=0.3V \times 0.3V/R_F$.

For example, $P=0.145W$ when $R_F=0.62\Omega$. Please apply the appropriate resistance to gain the rated power of 0.25W or more.

(4) Resistance for setting VMI, VSOFT, VOFF, and LA

Configure VMI, VSOFT, VOFF, and LA by divided resistance voltage from VREG.

Adopting the resistor of 1% accuracy is recommended because VSOFT and VOFF can be controlled by 32 steps.

In case the resistance is large, using the resistor of 300kΩ or less is recommended because the IC is easily influenced by the noise under the large resistance

(5) Pull-up resistance of FG/RDO

Because FG terminal and RDO terminal are open drain, in order to output high level, it is necessary to pull-up them to the external power supply. The recommendation range of the pull-up resistance is 10 to 100 kΩ. However, please select pull-up resistance to keep high voltage by checking the input current of the input terminal of the reception side of FG and RDO signals.
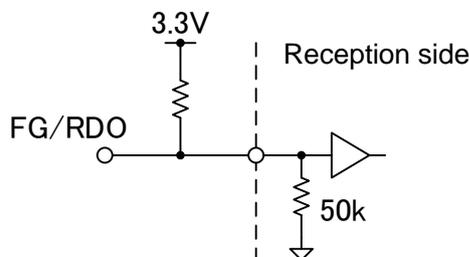
Figure 6.2 Example of pull-up of FR/RDO terminal

For example, as shown in Figure. 6.2, if the input terminal of the reception side is pulled-down with the resistance of 50kΩ, when the FG/RDO terminals are pulled-up to 3.3V with the resistance of 100kΩ, the voltage in high level is as follows; 3.3V/(100 kΩ+50 kΩ) x50 kΩ=1.1V. So, it may become impossible to recognize high level at the reception side. In order to configure the voltage in high level 2V or more, please use the resistance of 30kΩ or less.

When FG terminal and RDO terminal are not used, please set them open.

(6) Resistance of hall device

In case the power is supplied from 5V-power of VREG to the hall device, connect the current-limit resistor to the power terminal of the hall device not to exceed the maximum input current of the hall device. Design the circuit by considering the temperature characteristics of the input resistor of the hall device and having enough margin. For example, the maximum input current of the hall device is 10mA, the resistor of 510Ω is recommended.

Amplitude of the hall device changes depending on the resistance of the hall device. The voltage range that recognizes the hall signal correctly is shown in Figure 6.3.
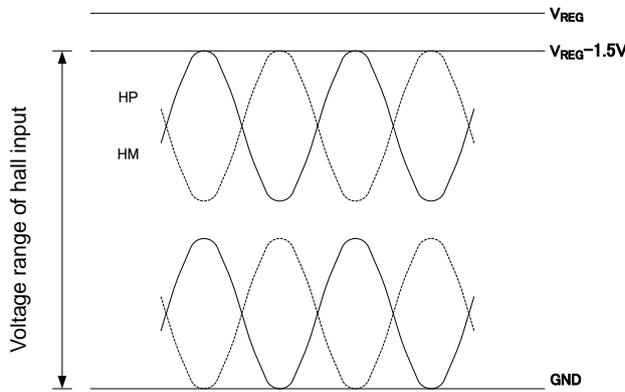
Figure 6.3 Voltage range of hall input
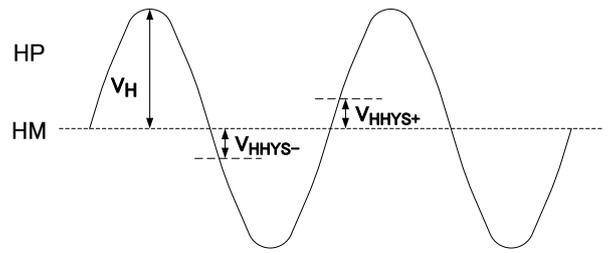
Figure 6.4 Hall signal, amplitude, and hysteresis

To recognize the switch of the hall signal correctly, amplitude of the hall device (V_H) should be 40mV or more. Hall amplifier has a hysteresis. The waveform of the hall signal is sine wave. When the amplitude (V_H) is 100mV, the phase-switching delay by hysteresis is about 5.7° (typ.). When the amplitude (V_H) is 200mV, the phase-switching delay by hysteresis is about 2.9° (typ.). Widen the amplitude of the hall device as possible because the phase gap of switching timing becomes larger when the amplitude of the hall is small.

Amplitude of the hall signal changes depending on the temperature characteristics of the hall.
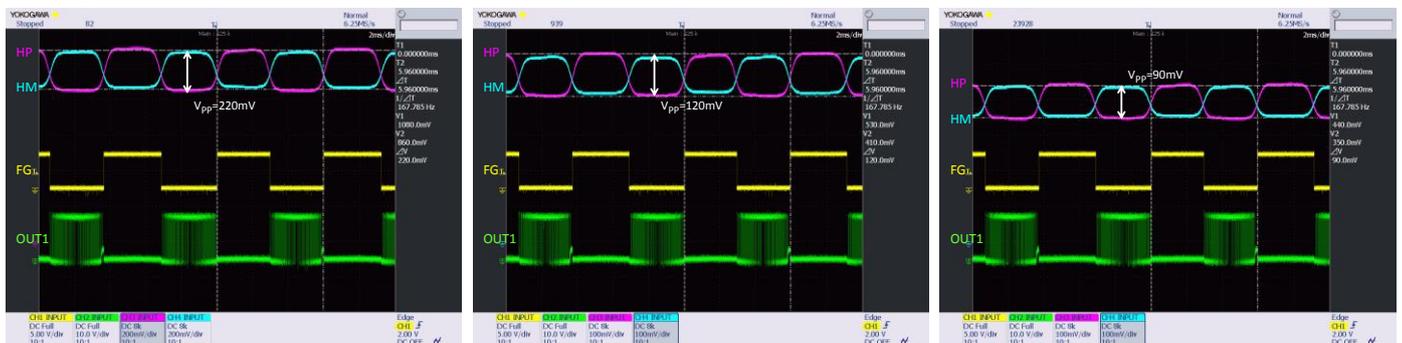
| a. Low temperature: | b. Ambient temperature: | c. High temperature: |
| Amplitude of hall signal: 220mV | Amplitude of hall signal: 120mV | Amplitude of hall signal: 90mV |

Figure 6.5 Example of hall-signal amplitude change depending on the temperature

The soft switching term of this IC is determined by the cycle of a hall signal. The amplitude of the hall signal does not affect the soft switching term. Please enlarge amplitude of a hall signal as much as possible.

Heat generation of the IC is reduced by supplying the power to the hall device from VM power supply. In this case, design the IC paying attention to the influence of the maximum ratings of the hall device, the voltage range of the hall signal, variation of VM power supply, and the noise.

(7) Conversion circuit between pulse duty input and analog voltage

When the speed control signal from exterior corresponds to pulse duty signal (not analog voltage), pulse duty should be converted to analog voltage by applying conversion circuit. When high-side of pulse duty signal (PWM in) is 5V, pulse duty signal can be converted to analog voltage (VSP out) by RC filter. When high-side of the pulse duty signal is 3.3V, level shifter circuit is necessary.

Example of level shifter circuit is shown in Figure 6.6. Threshold of PWM signal can be configured by the divided resistance voltage of R1 and R2. Output voltage when PWM Duty is 100% can be configured by the divided resistance voltage of R3 and R4. The relation of Duty and the output voltage can be approximated in the following formula.

$$VSP = 5V \times R4 / (R3 + R4) \times Duty$$

R5 and C1 works as RC filter to smooth the voltage. Adjust it depending on the frequency of the input PWM.

The circuit constant number in one example is shown in the Figure 6.7.
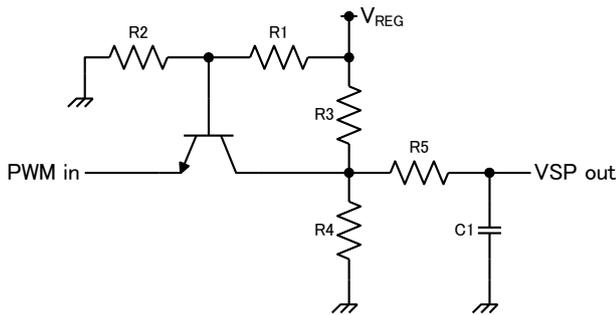
Figure 6.6 Example of level shifter circuit
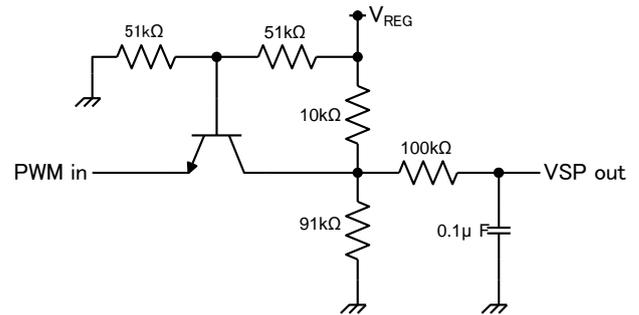
Figure 6.7 Example of constant number of level shifter circuit

7. Notes in designing board

   Please pay enough attention in designing the circuit pattern not to be influenced by wiring impedance etc. because it is assumed that large current flows into VM, RS, and a GND pattern especially. In addition, fully keep in mind that a power supply and GND become unstable easily by the inductance of the wiring impedance of the board since the output slew rate is fast when the output stage of the IC performs PWM switching.

【Example of board layout 1】
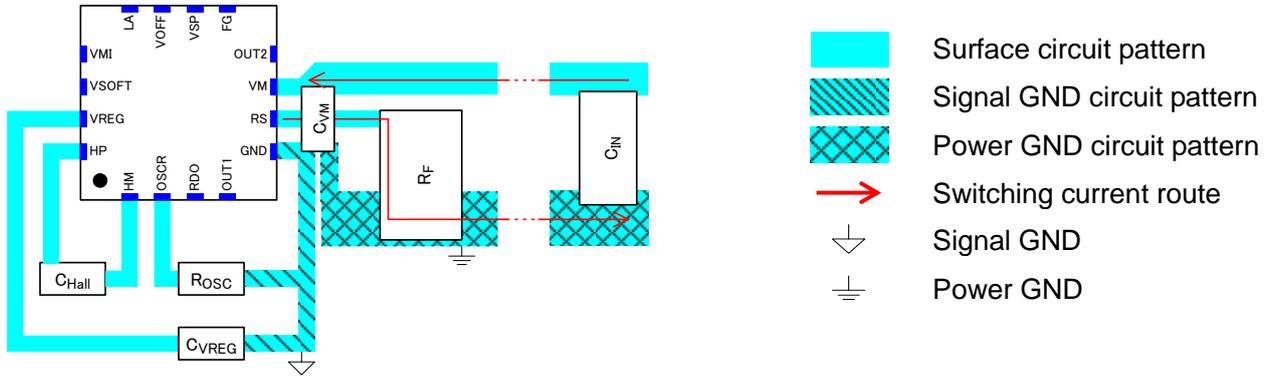
Figure 7.1 Board layout image of QFN package
        Notes: The figure is not drawn on a fixed scale.

・Thicken and shorten the line which flows switching current as much as possible.
・Arrange the capacitor between VM and GND near the IC terminal as close as possible. Even if a capacitor for smoothing input voltage is located at the entrance of the board power supply, when the capacitor is far from the IC, neither VM power-supply-voltage variation nor the GND voltage variation of the IC may fully be suppressed under the influence of L ingredient of wiring impedance in PWM switching. Be sure to arrange the capacitor near the VM and GND terminals of the IC. In this case, please select the most appropriate capacitor after enough evaluation though some effects are acquired also by the capacitor of small capacity (0.01μF to 0.1μF).
・Arrange the capacitor between Vreg and GND near the IC. In order to stabilize Vreg voltage, shorten the wiring distance between the capacitor GND and the IC GND to reduce route which flows switching current. Please confirm that the voltage of Vreg terminal is 5.5V or less on the basis of the GND terminal of the IC in operating. Please strengthen the capacitor between VM and GND when the voltage between the GND terminal of the IC and Vreg terminal is larger than 5.5V because GND of the IC sways to the minus side in PWM switching.
・Arrange the resistance for setting the reference current of oscillating circuit (Rosc) near the IC. Please design to reduce the route which flows switching current between the GND of Rosc and the GND terminal of the IC.
・When a jumper is required, the influence on the circuit operation is decreased by using output line (not GND line).
・In case of attaching the capacitor for reducing the noise of the hall signal, arrange it near HP and HM terminals of the IC. Recommend value of the capacitor is 0.01 μF to 0.1μF.

In designing the board with SSOP package, pay enough attention to the circuit pattern surrounding the GND.

【Example of board layout 2】
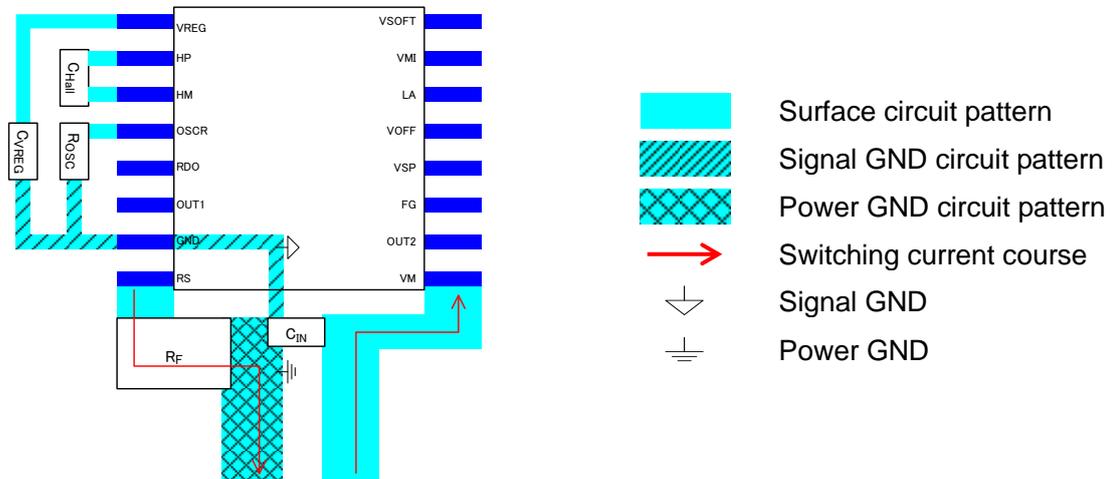
Figure 7.2 Board layout image of SSOP package
Notes: The figure is not drawn on a fixed scale.

In designing board, the land pattern size for reference is shown below.

Unit: mm

P-WQFN16-0303-0.50-002

SSOP16-P-225-0.65B
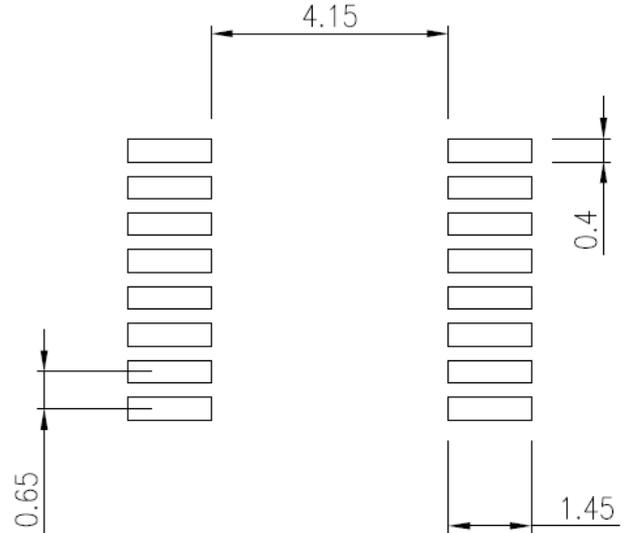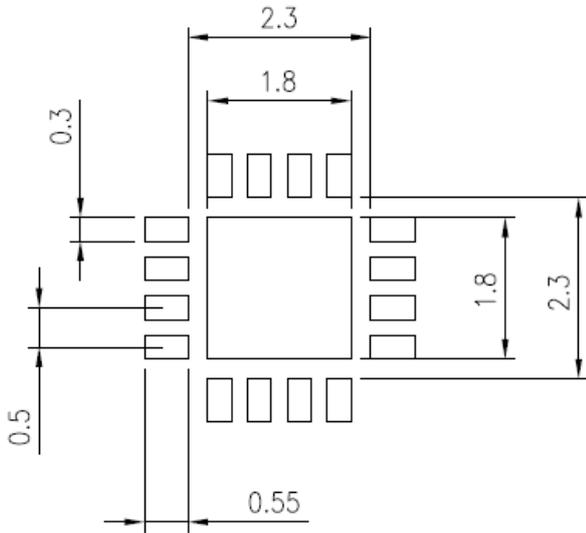
Cautions
- As long as there is no indication in particular, the unit of the size is a millimeter.
- The figures are for reference according to JEITA ET-7501 Level 3.
  The accuracy of figures and information, and completeness are not guaranteed.
- Please evaluate various conditions (soldering conditions etc.) enough, and adjust them in a customer's responsibility.
- The figures of this document do not show actual form or size correctly. Please do not design estimating the size by measurement etc. with the value from figures.
- In designing and using, please confirm the newest information and the operation manual of this product and follow them.

　Heat generated in the IC can be released efficiently by releasing it from the heat dissipation pad on the back of IC to the GND pattern of the board. Therefore, please arrange the GND area near the IC circumference as close as possible. In the case of a multilayer board, please arrange thermal via in order to lower the heat resistance between layers.

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8. Power consumption of the IC

Power of the IC is consumed mainly by the logic block, the internal regulator, and output stages.

P(total) = P(logic) + P(reg) + P(out)   ······ (Formula 1)

P (total):   Power consumption of IC

P (logic):   Power consumption of logic block

P (reg):   Power consumption of internal regulator

P (out):   Power consumption of outputs

・Power consumption of logic block
It can be calculated as follows;

P(logic) = V_M × I_{VM} ······ (Formula 2)

When VM=12V, I_{VM}=3mA (typ.). From (Formula 2), P (logic) =12V × 3mA = 36mW

・Power consumption of internal regulator
When using Vreg power supply as a power supply of external parts, such as a hall device, the power consumption of an internal regulator can be calculated as follows.

P(reg) = (V_M – Vreg) × I_{Vreg} ······ (Formula 3)

When VM=12V, I_{Vreg}=5mA (typ.). From (Formula 3), P (reg) = (12V-5V) × 5mA = 35mW

・Power consumption of the outputs
    PWM ON: Power consumption of the upper and lower sides of MOSFET
    PWM OFF: Power consumption of lower side of regeneration diode and lower side of MOSFET.
    And power consumption according to the bias current inside IC in the current regeneration. Bias current contains the parasitism current by a monolithic. The bias current in current regeneration is about 6% of regeneration current.

P(out) = I_{out}×I_{out}×$R_{on(H+L)}$×Duty + (I_{out}×V_F+I_{out}×I_{out}×$R_{on(L)}$ +VM×I_{bias}) × (1-Duty) ······ (Formula 4)

The power consumption of the outputs depends on the conditions, such as the control method, output peak current, and output duty.

When output current is rectangle wave of 400mA, output duty=80%. From (Formula 4),
P(400mA,80%)=0.4A×0.4A×1.6Ω×0.8 + (0.4A×1V + 0.4A×0.4A×0.8Ω + 12V×400mA×6%) ×0.2
        =0.368W

When using a soft switching function, output current can become close to a sine wave. Soft switching has maximum of 16 steps. The output PWM Duty ratio of each step is shown in Table 8.1.

Table 8.1 The relation of step of soft switching and output duty ratio

Step	Output ratio (%)	Step	Output ratio (%)	Step	Output ratio (%)
1	4	7	59	13	94
2	14	8	67	14	97
3	25	9	74	15	99
4	34	10	80	16	100
5	42	11	86		
6	52	12	91		

Under the condition that output current corresponds to sine wave (peak: 400mA) and the output PWM duty is 80% (max), a rough calculation shown below is gained.

P(sin)={ P(400mA× 4%,80%× 4%) +P(400mA×14%,80%×14%)+P(400mA×25%,80%×25%)
      + P(400mA×34%,80%×34%)+P(400mA×42%,80%×42%)+P(400mA×52%,80%×52%)
      + P(400mA×59%,80%×59%)+P(400mA×67%,80%×67%)+P(400mA×74%,80%×74%)
      + P(400mA×80%,80%×80%)+P(400mA×86%,80%×86%)+P(400mA×91%,80%×91%)
      + P(400mA×94%,80%×94%)+P(400mA×97%,80%×97%)+P(400mA×99%,80%×99%)
      + P(400mA×100%,80%×100%)} / 16
    =0.270W

P(400mA×4%,80%×4%) is the power consumption under the condition that drive current is 400mA×4% and output duty is 80%×4% in rectangle-wave drive. It is calculated from (Formula 4).

The power consumption of the output stages depends on conditions, such as the control method, output peak current, and output duty. Figure 8.1 shows the power consumption of the outputs in rectangle-wave drive, and Figure 8.2 shows the approximate calculation result of the power consumption of the outputs in sine-wave drive.
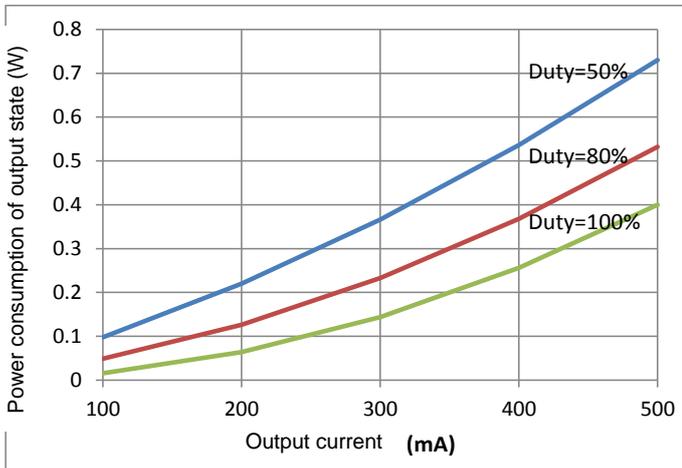
Figure 8.1 Power consumption of output stages in rectangle-wave drive
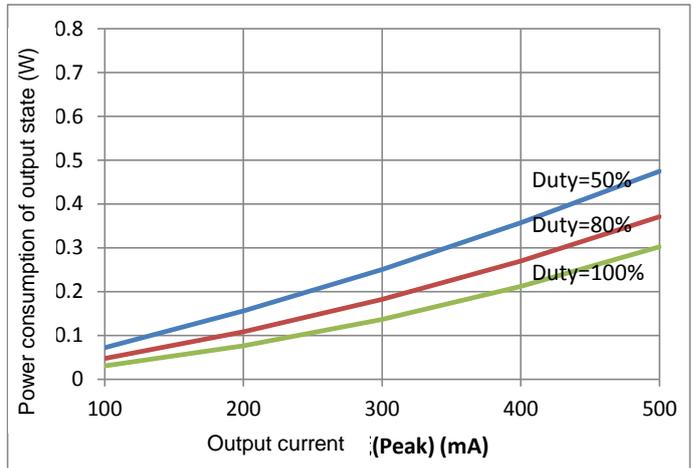
Figure 8.2 Power consumption of output stages in sine-wave drive

・Power consumption of IC
The final power consumption P (total) is calculable as follows.

When output current corresponds to the rectangle wave of 400mA, and the output duty is 80%,
    P (total) = P (logic) + P (reg) + P (out)
            = 0.036W+0.035W+0.368W
            = 0.439W

Please design heat dissipation after evaluating the thermal design for the board by referring to the above calculated values.

9. Power dissipation

The relation of the ambient temperature (T_a), the junction temperature (T_j), and the heat resistance ($R_{th\,(j-a)}$) between the ambient temperature and the junction is as follows.

$$T_j = T_a + P_{(total)} \times R_{th\,(j-a)}$$

The absolute maximum rating of junction temperature (T_j) is 150°C. Permissible power consumption ($P_{(total)}$) depends on T_a and $R_{th\,(j-a)}$. When ambient temperature is high, permissible power consumption becomes small accordingly. When heat resistance is high, permissible power consumption becomes small accordingly.

(Reference) Relation of power dissipation and ambient temperature

TC78B002FNG (SSOP16)
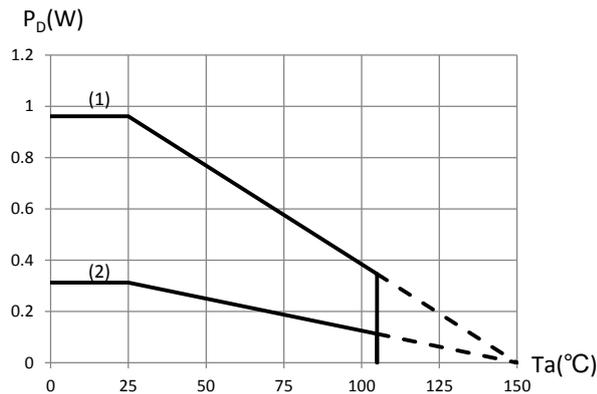
TC78B002FTG (QFN16)

(1) In mounting on board $R_{th(j-a)}$=130°C/W
    (40mm×30mm×1.6mm   2-layer FR-4 board)

(2) IC only
    $R_{th(j-a)}$=400°C/W
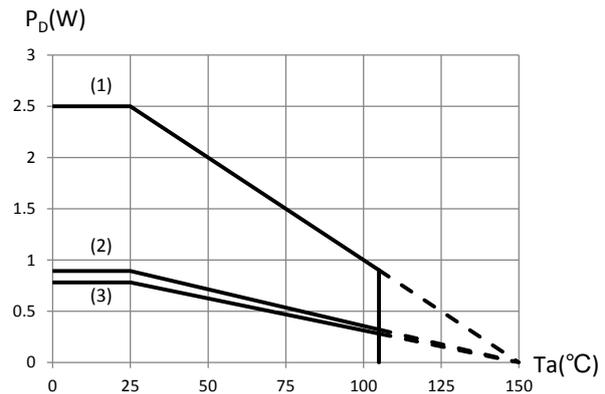
(1) In mounting on board $R_{th(j-a)}$=50°C/W
    (74mm×74mm×1.6mm   4-layer FR-4 board)

(2) In mounting on board $R_{th(j-a)}$=140°C/W
    (74mm×74mm×0.6mm   2-layer FR-4 board)

(3) In mounting on board $R_{th(j-a)}$=160°C/W
    (φ40mm×1.6mm   1-layer FR-4 board)

When QFN package is mounted on one side board assuming $R_{th\,(j-a)}$ is 160°C/W), T_j which corresponds to each T_a is calculated as follows. The usage condition is above-mentioned $P_{(total)}$ is 0.439W.

・When a motor is used at the ambient temperature of 0℃,
   T_j = 0℃ + 160℃/W × 0.439 (W) = 70℃
・When a motor is used at the ambient temperature of 25℃,
   T_j = 25℃ + 160℃/W × 0.439 (W) = 95℃
・When a motor is used at the ambient temperature of 60℃,
   T_j = 60℃ + 160℃/W × 0.439 (W) = 130℃
・When a motor is used at the ambient temperature of 80℃,
   T_j = 80℃ + 160℃/W × 0.439 (W) = 150℃

Table 9.1 In rectangle-wave drive of 400mA, relation between T_j and T_a

QFN package $R_{th(j-a)}$=160°C/W

T_j (℃) / T_a (℃)	Duty=80%	Duty=100%
0	70	52
25	95	77
60	130	112
80	150	132

To reduce heat generation of the IC,
  - Use a multilayer board instead of one-side board to reduce heat resistance.
  - Supply a power supply to the hall device from VM power supply to reduce the power consumption of an internal regulator.

Degradation of the IC becomes fast if the junction temperature is high. In order to provide higher reliability, please use the IC under the condition that $T_{j\,(ave)}$ is 105°C or less.

$$T_{j\,(ave)} = T_{j\,(ON)} \times \text{ON Duty} + T_{j\,(OFF)} \times \text{OFF Duty}$$

In case of operating the IC at the ambient temperature of 60°C for 8 hours (average) per one day,
$T_{j\,(ave)}$ = 130°C x (8hr/24hr) + 60℃x (16hr/24hr) = 83.3°C

Please design heat dissipation with enough margin after evaluating the thermal design for the board by referring to the above calculated values.

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IC Usage Considerations

Notes on handling of ICs

    (1)   The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

    (2)   Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

・   Points to remember on handling of ICs

    ・(1) Over current Protection Circuit

        Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the over current protection circuits operate against the over current, clear the over current status immediately.

        Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

    ・(2) Thermal Shutdown Circuit

        Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.

        Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

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