

Package Mounting Guide

QFN

Revision 1.0

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TOSHIBA CORPORATION

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Preface

Purpose of this document

This document describes design techniques and mounting methods for improving the solder ability and heat dissipation of our products, and aims at producing the the printed circuit board assembly (PCBA) with high manufacturability.

Intended Audience

This document is to be intended for use as a guide for those who are involved in the printed wiring board design and soldering process. The knowledge of heat dissipation and package mounting methods is required for use.

References for package

This document describes the printed wiring board design and the PCBA guidelines. Since each package has a different land pattern dimension, refer to the following documents for each package when you design the printed wiring board.

Document	Note
Package Mounting Guide	This document
Technical data sheet	Package information (dimensions)
Land pattern dimensions for reference	Land patterns for each package

Abbreviation

Some of the abbreviations used in this document are shown below.

SMD	Surface Mount Device
QFN	Quad Flat Non-Leaded Package
CAD	Computer Aided Design

1. QFN

Recently, many circuits are integrated in semiconductor devices by refinements and advanced features, and also calorific values are increasing due to high-speed operation. Moreover, the structure is difficult to radiate heat due to miniaturization and increased density of electric devices. Then, the heat problems of the semiconductor are an important factor in electronic device development because it affects the operation speed and the product life. On the other hand, poor-wetting of solder such as voids may occur in the case of conventional lead-free soldering, and heat dissipation or reliability of the soldering may be spoiled. As an example which solves these problems, the design technique and the mounting method of improving the heat dissipation and the reliability are explained.

2. Package structure

Packages are divided into two types by the mounting method; the pin insertion type and surface-mount type (hereinafter SMD). This document is targeted to the QFN in SMD packages. The package characteristics are as follows.

Table 2.1 Package characteristic

Name	Figure	Characteristic
QFN		A package having single-inline terminal pads along four edges of the bottom face. The terminal pads may or may not be exposed on the package sides. (Quotations from: JEITA ED-7303C, Names and Codes for Integrated Circuit Packages)

In the QFN package, a metallic pad is exposed from the center of the package bottom, and the pad is called Exposed pad (hereinafter E-Pad). The heat dissipation and soldering intensity are high by soldering E-Pad to the printed wiring board.

3. Design guide for printed wiring board

3.1. Lead design

For the lead shapes and dimensions, refer to the land pattern dimensions for reference. The dimensions are compliant with JEITA ET-7501 Level3. The CAD data of these dimensions are available on the Toshiba website.

3.2. Design around E-Pad

Form the land pattern for the E-Pad on the package with E-Pad, and solder to the printed wiring board. Since the land pattern for the E-Pad has the large soldering area, air bubbles remain easily and they cause voids. Moreover, since the lead-free soldering used in many solders is poor-wetting and high surface tension at dissolution, voids tend to occur. Therefore, measures to prevent voids are required. In the next sections, the design is explained with the Figure of QFN48-P-0707-0.50.

3.2.1. Land pattern and solder resist design

Soldering area where E-Pad is soldered is made by dividing a land pattern by a solder resist. Generally, the smaller number of divisions makes a soldering area larger, and which makes voids more likely to occur. On the contrary, if the number of division is large, a solder resist area becomes large, and a soldering area becomes small, then the solder intensity tends to be weak. To keep the stable solder intensity, it is important to arrange the solder area with few deviations, in sufficient balance. The solder area with the solder resist is recommended about 50% or more of area to the E-Pad.

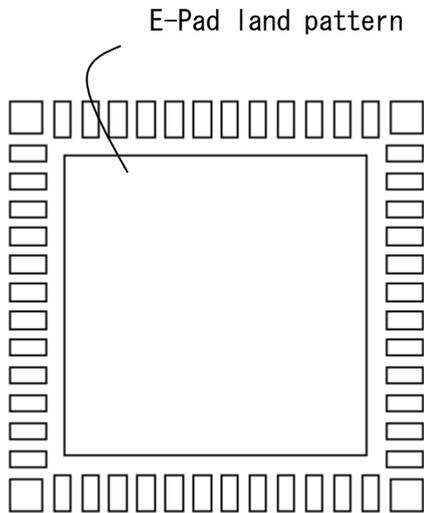


Figure 3.1 Land pattern example of E-Pad

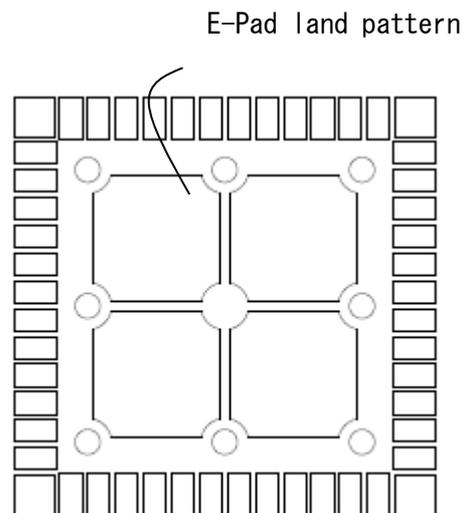


Figure 3.2 Design example of solder mask

3.2.2. Arrangement and number of thermal via

Thermal vias are through holes that go through a printed wiring board, and raise heat dissipation of the package. It is recommended that the thermal vias are arranged to the perimeter of the E-Pad land pattern. Connect the one side of a thermal via to the E-Pad land pattern, and the other side to the copper plane of the internal layer. This copper plane serves as heat diffusion. The optimum number of thermal vias is determined by thermal and electric analysis or measurement with consideration of the power consumption of products.

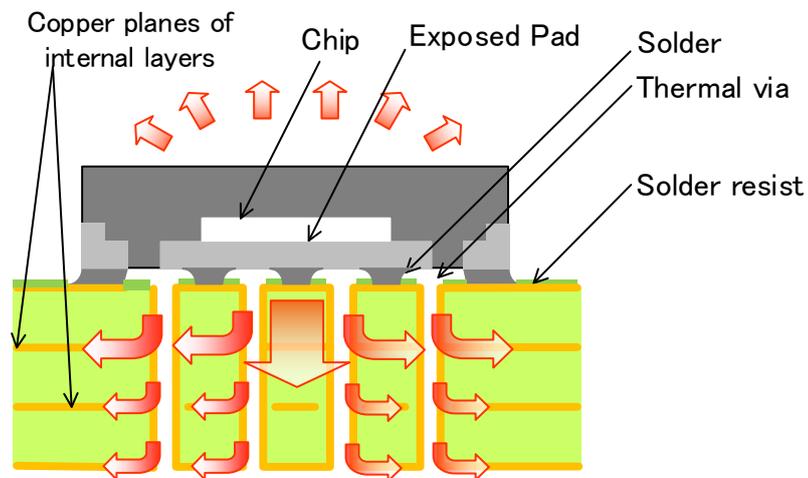
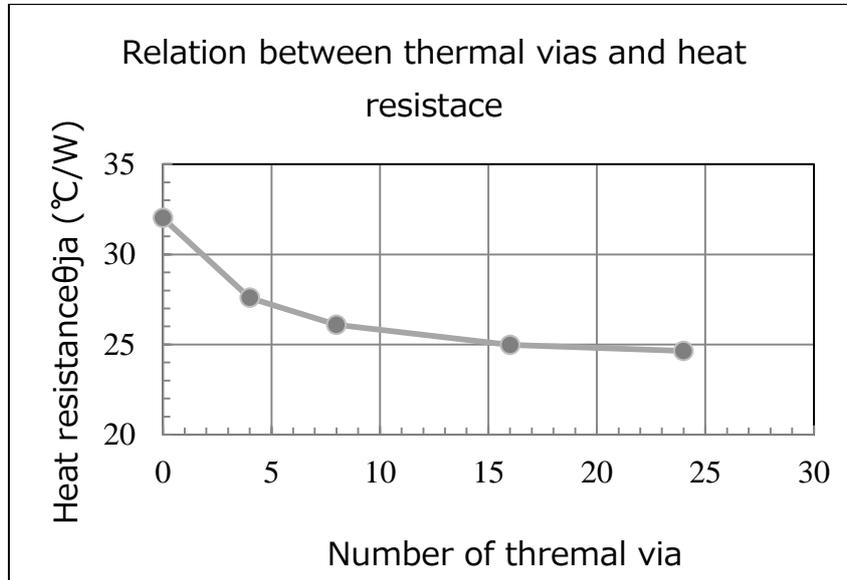


Figure 3.3 Heat dissipation image

Figure 3.4 shows a simulation result of heat resistance simulation for the thermal via arrangement and number of thermal vias. Figure 3.5 shows images of relationship between the number of thermal via and arrangement. Since heat is accumulated directly under the package even if many thermal vias are set in the E-Pad, heat dissipation cannot be expected. Arranging thermal vias evenly on the edge of the E-Pad land pattern can diffuse heat and lowers heat resistance with the small number of those. The recommended optimum thermal vias dimension is about 3 mm long according to the simulation result and the land pattern dimensions. Number of thermal via should be calculated with the perimeter length of a package to be used and the recommended interval.



Simulation conditions

- Verification package: P-VQFN48-0707-0.50-004 (E-Pad: 5.54 mm × 5.5 mm)
- Chip: 2.8 mm × 2.8 mm × 0.29 mm
- PCBA: Equivalent for 4-layer board of JEDEC (width: 76.2 mm, length: 114.3 mm)
- Ambient air temperature: 25°C
- Wind velocity: 0m/s

Figure 3.4 Relation between thermal via and heat resistance

Number of thermal via and arrangement	1	4	8	16	24
Inside of land pattern for Exposed Pad					

Figure 3.5 Images of land pattern and thermal via arrangement

3.2.3. Thermal via dimensions

Thermal vias are arranged outside of the E-Pad, and take intervals from the land pattern. This interval prevents soaking up solder to the thermal vias and solder ball generation. The diameter of the thermal via is about 0.30 to 0.33 mm, and copper via plating about 20 μm is recommended for the inside of the via.

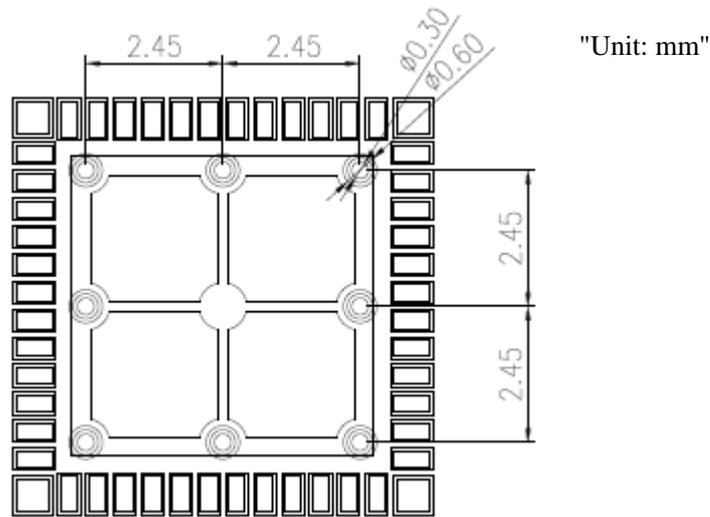


Figure 3.6 Recommended thermal via dimensions

3.3. Metal mask design

A metal mask is a lithograph for printing a solder paste on the land pattern of a printed wiring board. Recommended thickness of the metal mask is from 125 to 175 μm. However, the adjustment of the thickness may be also required due to the balance of peripheral parts size.

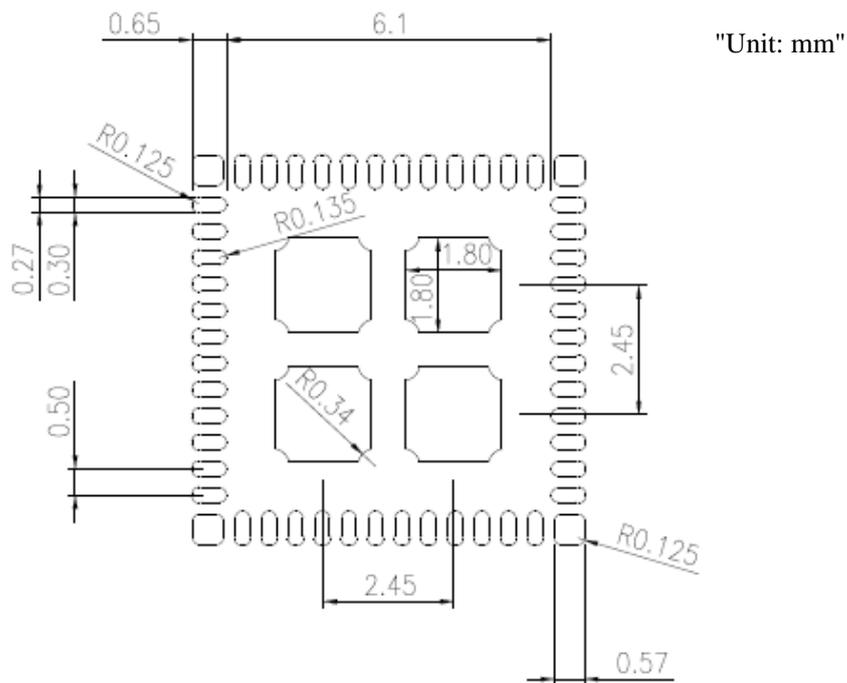


Figure 3.7 Recommended metal mask pattern

4. Mounting guide for printed wiring board

4.1. Mounting flow

The recommended soldering method for each package is reflow process. For the reflow process, refer to section 4.1.1 to 4.1.4.

4.1.1. Printing solder paste

A solder paste is a pasty composite material made by mixing solder, flux, and the like. The solder paste is printed through a metal mask to the land pattern of the printed wiring board.

4.1.2. Mounting package

A package is mounted to the position where the solder paste is printed. In addition, use of the package which absorbed moisture may generate a crack because of the heat generated by soldering. Please observe the precautions for unpacking conditions. For the package tends to absorb moisture, it is recommended to bake in advance.

4.1.3. Soldering (reflow soldering)

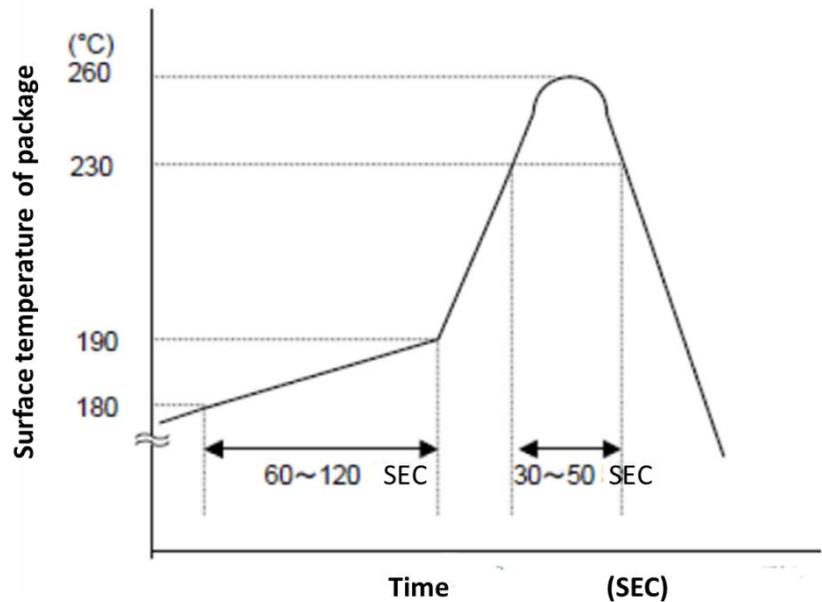
The printed wiring board mounting a package is soldered by the heating of a reflow oven. The package should be heated so that the temperature of the soldering may not exceed the maximum reflow temperature profile.

4.1.4. Visual inspection

In the visual inspection, a position gap, a solder bridge, and a poor-wetting soldering are confirmed.

4.2. Reflow thermal profile

Figure 4.1 shows an example of the reflow thermal profile. In this example, a surface temperature of the package is preheated for 60 to 120 seconds at about 180 to 190°C. After that, the temperature raises gradually, and the surface temperature of the package continues the state which is about 230 to 260°C (peak temperature) for 30 to 50 seconds. In addition, temperature profiles differ due to a package. Confirm the temperature profile of the package to be used.



- Temperature and time should be set less than the above profile.
- Optimum temperature should be set due to solder paste types.

Figure 4.1 Thermal profile example

5. Rework

Use a heater nozzle which heats the target package only to remove the package. The PCBA is preheated using a convection-type heater. Thermal profile at removal is the same as that of mounting, however, the peak time should be as short as possible. When the package with E-Pad is difficult to remove, heat the back of the PCBA with a heater. In the case of removal, please take care so that the land on the board does not exfoliate.

In addition, Toshiba warrants neither for reusing of the removal package nor the soldering reliability of removal part.

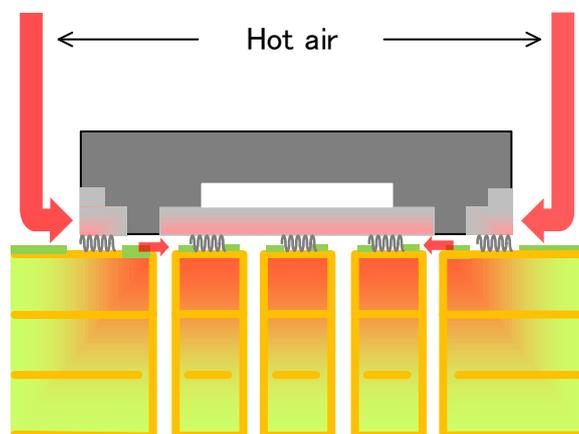


Figure 5.1 Rework overview

7. Revision History

Table 7.1 Revision History

Revision	Date	Description
1.0	2016-03-17	Newly released

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