TB6605FTG

Usage considerations

Summary

The TB6605FTG is a three-phase sine-wave PWM controller for DC brushless motors for home appliance, fan, and office equipment. High-efficiency drive and noise reduction are realized by sine-wave PWM drive with 2-phase modulation system.

This is a reference. Please do not determine the final equipment design by this material.

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1. Power supply voltage

1.1. Power supply voltage usage range

The TB6605FTG has a single power supply. Use the IC within below range.

Table 1.1 Power supply voltage usage range

Characteristic	Symbol	Voltage usage range	Unit
Power supply voltage	V_{CC}	9 to 28	V

(Note): Design the motor to correspond the voltage of OUT-A, OUT-B, and OUT-C terminals to the absolute maximum ratings (30V) or less.

2. Control input

2.1. Speed command PWM input

Table 2.1 Frequency range of PWM input

Characteristic	Symbol	Frequency range of PWM input	Unit
PWM-in frequency	fPWM-in	10 to 100	kHz

・PWM signal is inputted from outside to the terminal of PWM-in as a speed command signal.
The duty controls the sine-wave PWM modulation signal.
When ON duty of PWM-in increases, the duty of output PWM increases and the rotation speed becomes faster.
・Input is received by TTL. Pull-up resister of 5V is incorporated in the IC.
The operation is Low active. When the term of low level operation continues longer, ON term becomes longer.
・PWM control range of 0 to 100 % is recognized.
・Resolution: 20kHz 0.4%, 40kHz 0.8%
However, when PWM-in duty is recognized in 180°energization mode, the variation of this recognition (±0.4% (PWM-in=20 kHz)), which is generated from the non-synchronous with the internal clock, is ignored and cancelled.
・When PWM-in is 0 %, output is turned off and the lock protection is released.
・Output PWM frequency does not change depending on the PWM-in frequency. Output PWM is configured according to the internal reference clock frequency.

3. Detection circuit

This IC incorporates below functions. Note that this circuit does not necessarily provide the IC with a perfect protection from any kind of damages. Make sure to use the IC within the absolute maximum ratings. Otherwise, the IC may be destroyed by short-circuiting between outputs, air contamination faults, or faults due to improper grounding before operation.

3.1. Over current detection circuit

The resistor (R6) detects the over current. This circuit operates when the output voltage reaches the reference voltage of the current limiter circuit (Vdc = 0.25 V (typ.)).

The current value (IOUT), which is the threshold value of operating the over current detection, is calculated as follows; IOUT = Reference voltage of current limiter circuit (Vdc)/Detection resistor (R6). As for the resistor of R5 and the capacitor of C6, please adjust the filter to reduce the PWM switching noise and to avoid the malfunction of the over current detection.

Ex.)When the resistor (R6) is set 0.1 Ω, IOUT (typ.) = 0.25 V (typ.)/0.1 Ω = 2.5 A

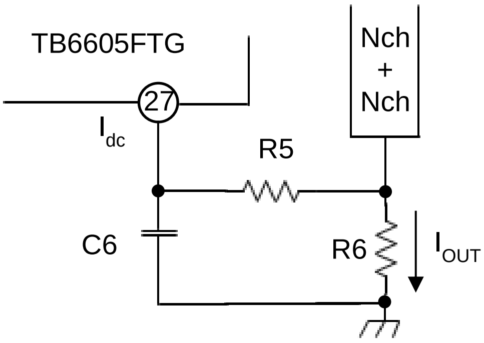


Figure 3.1 Adjustment of the filter value

3.2. Lock protection

Lock protection turns off the output power FET when the motor is locked.

<Setting method>

Below 6 modes are set by the voltage of CLd terminal.

<Operation description>

In case that the edge of the hall pulse signal (HP) does not generate within the lock protection time, upper and lower of all output power FET are turned off.

<Releasing method of turning off the outputs>

Latch mode is released at the timing of PWM frequency by setting the stop state, the brake state, or PWM-in=0 % (High) once.

In auto recovery, the operation recovers for 3 times of the lock protection time.

Please set the below time or more as a recognition time for release signal.

Stop recognition time: 6/frequency of internal reference clock ⇒ 1.2 μs @ fx = 5 MHz

Brake recognition time: 1/ (frequency of internal reference clock/128) ⇒ 99.2 μs @ fx = 5 MHz

PWM-in = 0 % recognition time: 1/ (frequency of internal reference clock/512) ⇒ 410 μs @ fx = 5 MHz

Table 3.1 Mode and lock protection time for voltage of CLd terminal

Voltage of CLd terminal			Mode
min(V)	typ.(V)	max(V)	
0	0	0.4	Without lock protection
0.65	0.71	0.77	Auto recovery mode, Lock protection time 10 s
1.05	1.13	1.22	Auto recovery mode, Lock protection time 5 s
1.53	1.63	1.75	Auto recovery mode, Lock protection time 1 s
1.99	2.12	2.24	Latch mode, Lock protection time 10 s
2.47	2.60	2.72	Latch mode, Lock protection time 5 s
2.95	V_{ref}	V_{ref}	Latch mode, Lock protection time 1 s

Setting voltage of the lock protection is converted by the internal A/D converter.
The A/D converter uses Vreg as a power supply. It determines the reference voltage with the dividing resistor voltage in the IC.
The voltage of the lock protection is configured by adopting the external resistor whose error is ±5 % by applying Vreg as a power supply.
Recommended external resistor and the setting voltage variation considering the variation of resistance are shown below.
CLd terminal should not be open. Configure its voltage as below table.
Capacitor should be connected to CLd terminal to reduce the noise.

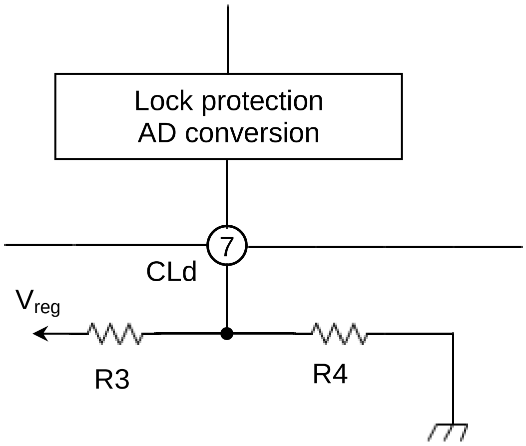


Figure 3.2　Adjustment by dividing resistor voltage

Mode	Ratings			External resistance (k Ω)		Variation of external R±5 % (calculated value)		
	min(V)	typ.(V)	max(V)	R3	R4	min	typ.	max
Without lock protection	0.00	0.00	0.40	100	0	0.00	0.00	0.00
Auto recovery mode, Lock protection time 10 s	0.65	0.71	0.77	91	15	0.65	0.71	0.77
Auto recovery mode, Lock protection time 5 s	1.05	1.13	1.22	82	24	1.05	1.13	1.22
Auto recovery mode, Lock protection time 1 s	1.53	1.63	1.75	68	33	1.53	1.63	1.75
Latch mode, Lock protection time 10 s	1.99	2.12	2.24	30	22	1.99	2.12	2.24
Latch mode, Lock protection time 5 s	2.47	2.60	2.72	36	39	2.47	2.60	2.72
Latch mode, Lock protection time 1 s	2.95	Vref	Vref	0	100	5.00	5.00	5.00

Table 3.2　Recommended values of external resistor

3.3. Boost avoiding function

When the motor rotation speed is decreased suddenly by PWM-in duty in the 180°energization mode (sine-wave drive), the voltage of the power supply rises because the current flows reversely from the motor to the power supply. This function is incorporated to suppress the boost of the power supply.

When the voltage of Vcc rises, the operation switches from 180°energization (synchronous rectification) to 120°energization (Upper PWM).

When the voltage of Vcc falls, the operation recovers to 180°energization (synchronous rectification) mode.

<Note>

This function switches the output drive mode by the voltage of the power supply. It cannot suppress the voltage boost which is generated by the power supply regeneration in the output off mode where the operation is switched from high speed rotation mode to PWM-in=0% or STOP mode, and other external reasons.

Usage conditions: 12V spec. and 24V spec. are switched by OVP terminal.

●12V spec. (OVP terminal = Low level)

(1) Switching voltage: When Vcc > 15.5V (typ.): Synchronous rectification (180°energization) ⇒ Upper PWM (120°energization)

Variation of judging voltage: 14.5V (min) 15.5V (typ.) 16.5V (max)

(2) Recovery voltage: When Vcc < 14.5V (typ.): Upper PWM (120°energization) ⇒ Synchronous rectification (180°energization)

Variation of judging voltage: 13.5V (min) 14.5V (typ.) 15.5V (max)

●24V spec. (OVP terminal = High level)

(1) Switching voltage: When Vcc > 28.5V (typ.): Synchronous rectification (180°energization) ⇒ Upper PWM (120°energization)

Variation of judging voltage: 27.5V (min), 28.5V (typ.), 29.5V (max)

(2) Recovery voltage: When Vcc < 14.5V (typ.): Upper PWM (120°energization) ⇒ Synchronous rectification (180°energization)

Variation of judging voltage: 26.5V (min), 27.5V (typ.), 28.5V (max)

3.4. Supply voltage supervisory function

Supply voltage supervisory function is incorporated for Vcc and Vreg voltage.

Vcc supply voltage (24 V, ext-applied)
・Vcc(H) ≤ 8.2 V(typ.) Vcc(L) ≤ 7.5 V(typ.)
(Power ON)
When Vcc supply voltage is 8.2 V (typ.) or less at the rising edge, external FET (Upper and Lower) is turned off and the internal logic is reset.
(Power OFF)
When Vcc supply voltage is 7.5 V (typ.) or less at the falling edge, external FET (Upper and Lower) is turned off and the internal logic is reset.

Vreg voltage (5 V, internal reference voltage)
・Vreg(H) ≤ 4.1 V(typ.) Vreg(L) ≤ 3.8 V(typ.)
(Power ON)
Vreg rises when Vcc rises.
When Vreg voltage is 4.1 V or less, external FET is turned off and the internal logic is reset.
(Power OFF)
Vreg falls when Vcc falls.
When Vreg voltage is 3.8 V or less, external FET is turned off and the internal logic is reset.

Upper Nch gate voltage
The gate voltage of the upper FET is monitored.
Output ON: The voltage between Vcc and Cp3 is 6.5V or more.
Output OFF: Above voltage falls to 6V.

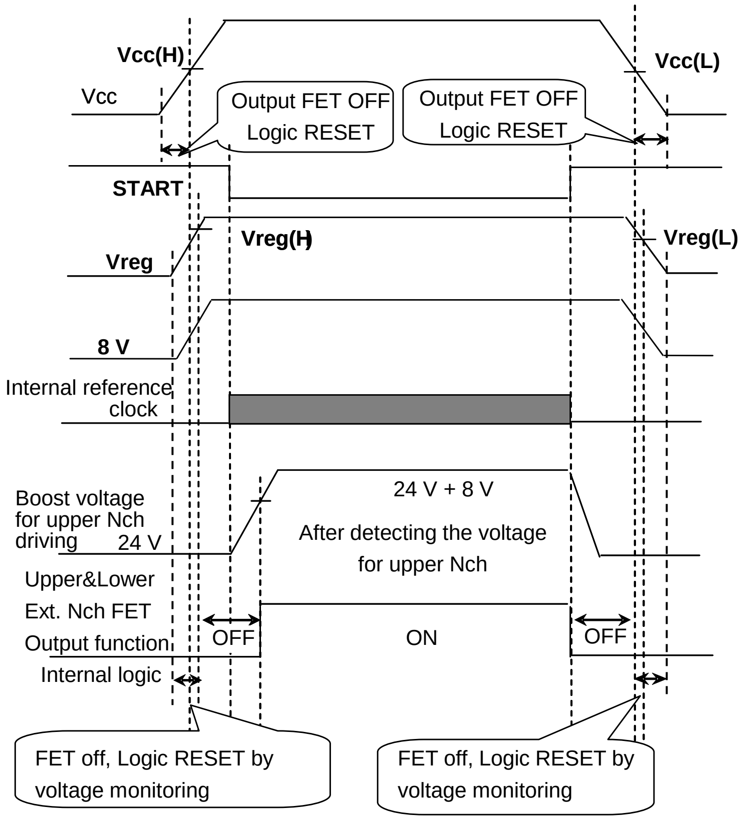


Figure 3.3 Supply voltage sequence

4. Application circuit example

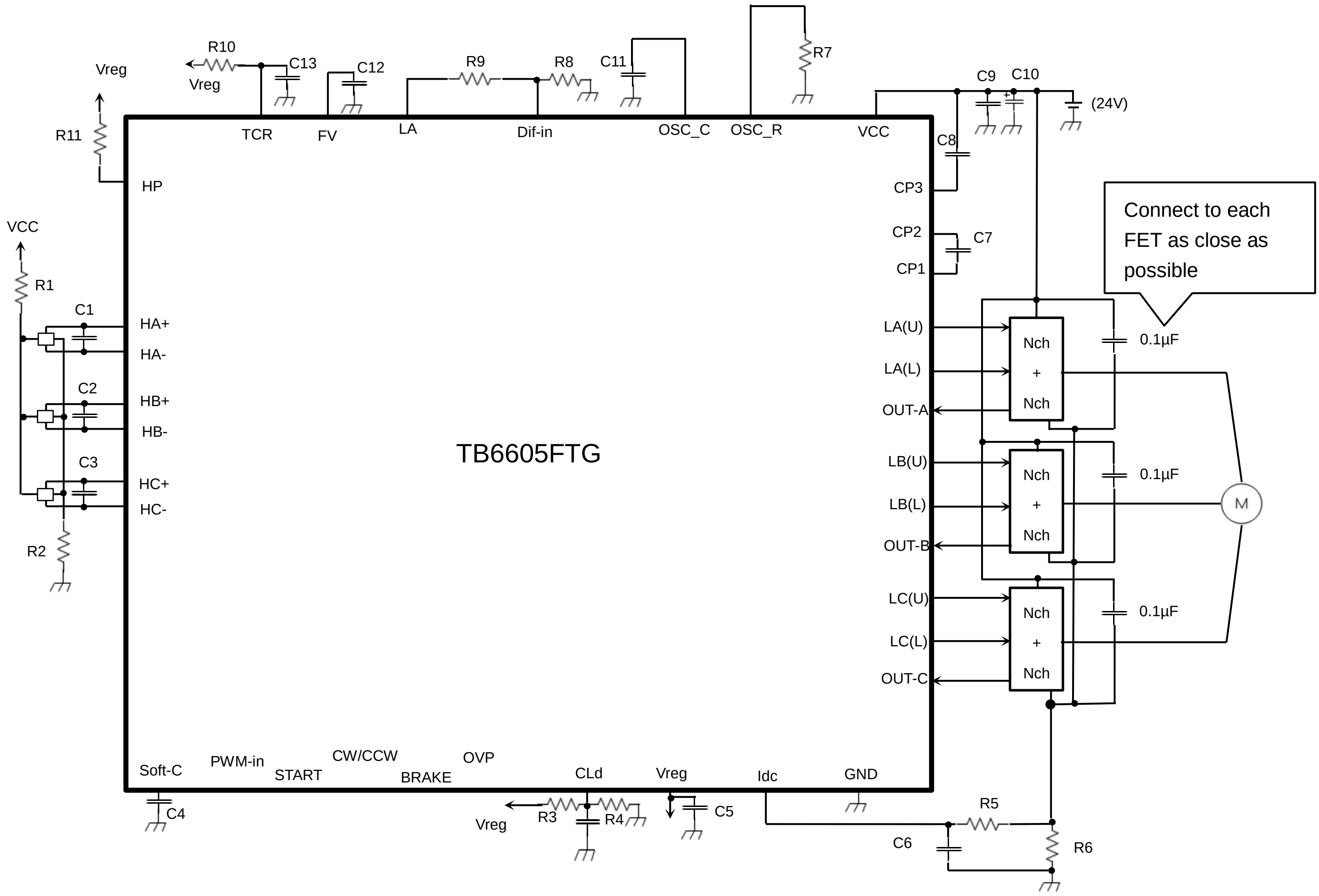


Figure 4.1 Application circuit example

(1) Internal reference clock frequency

IC generates reference clock internally with the external C and R.
Approximation of the external CR and the internal reference clock frequency (fx) is as follows;

$$fx = \frac{6.1}{1.85 \times C_{[pF]} \times 10^{-12} \times R_{[\Omega]} + 350 \times 10^{-9}} [Hz]$$

Following parameters are configured by this reference clock.

(a)PWM frequency
(b)Dead time
(c)Lock protection time, Recovery time
(d)Charge pump operating frequency
(e)Switching frequency from 120°to 180°energization

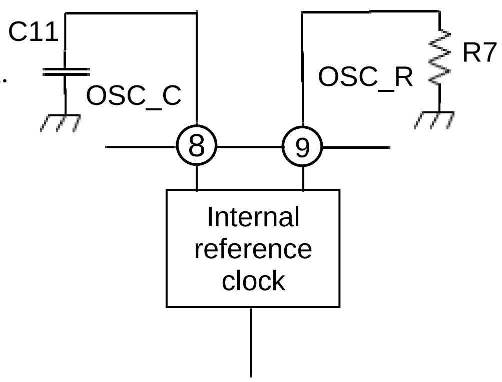


Figure 4.2 Adjustment of internal reference clock frequency

Each formula is as follows;

- ・PWM frequency fpwm = fx/248
- ・Dead time td = (1/fx)×6
- ・Charge pump (Voltage boost circuit) operating frequency: fx/16
- ・Lock protection time (tlock) and the recovery time (trev) are as follows;

  tlock = tsel/(fx/248/10001), trev = 3×tlock

  (1 s setting: tsel = 2, 5 s setting: tsel = 10, and 10 s setting: tsel = 20)
- ・Switching frequency from 120°to 180°energization: fH = fx ÷ (2^{10} × 64 × 6)

The internal reference clock should be configured in the range of 2MHz (min) to 8MHz (max) including the variation.

(*)When C=47pF and R=10kΩ, fx is 5 MHz (typ.). The variation is ±10 % when the frequency is 5MHz.

Table 4.1 Frequency and time determined by internal reference clock frequency

Setting range of internal reference clock frequency	2.3 MHz(min)	5 MHz(typ.)	7.2 MHz(max)
Setting range of PWM frequency	9.2 kHz	20.1 kHz	29.0 kHz
Setting range of dead time	2.6 µs	1.2 µs	0.8 µs
Setting range (5 s setting*) of lock protection time	10.78 s	4.96 s	3.44 s
Operation frequency of charge pump	143.75 kHz	312.5 kHz	450 kHz

(*) It can be set to 1/5 and x2 by CLd set.

⑵ Soft start

Soft start function starts the IC operation slowly in motor startup.
It starts the operation by limiting the speed command voltage which is inputted by PWM.
Speed command (PWM signal) is switched with 32 steps.
The external capacitor of soft_c terminal is used as a clock of 32 steps.
16 cycles of the oscillation frequency of soft_c terminal is recognized as one step.

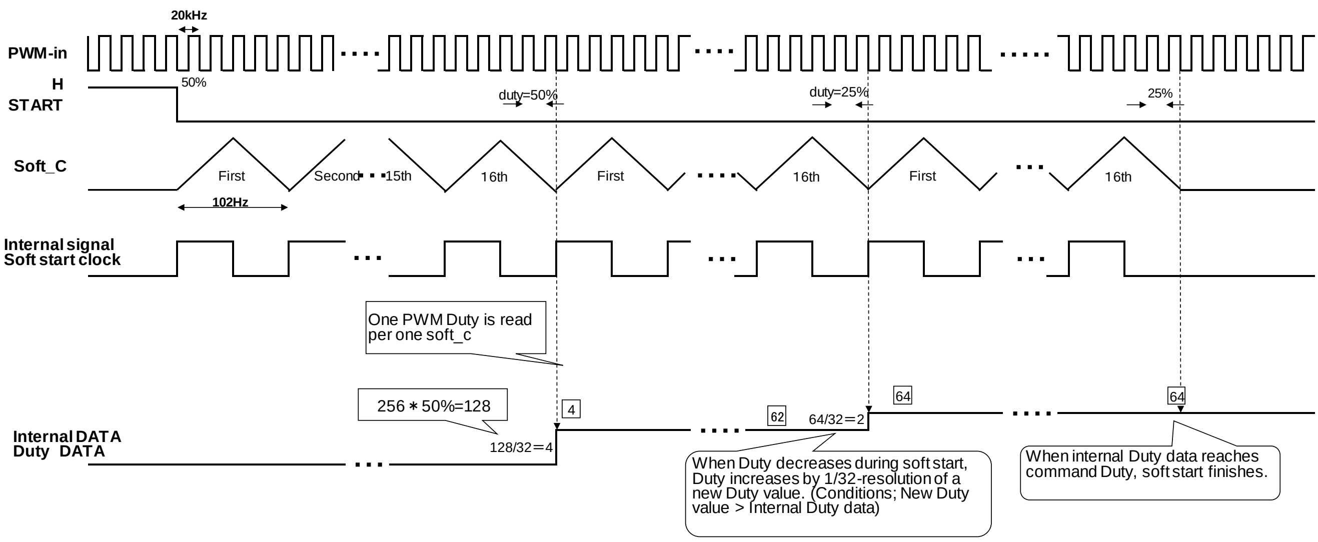


Figure 4.3 Sequence of soft start

External capacitor: 5 seconds in connecting the capacitor of 0. 016μF.
Maximum setting time: 5 s, Time variation: 5 s± (1 s)
Relation equation between the soft start time and the external capacitor is as follows;

$$Tsoft(s) = 16\times32/(0.0018\times10^{3}\times C^{-0.981})$$

C: Capacitance of external capacitor (μF)

*When the torque is very small, the error becomes larger because of the remainder of division.
In case of not using soft start function, short-circuit soft_c terminal to Vreg. Do not open soft_c terminal not to cause malfunction because of noise. In using soft start function, the capacitor of 1000pF or more should be connected.

(3) Auto lead angle

Lead angle converts the rotation number signal (HP frequency) to the voltage.
Conversion gain of the rotation number (HP frequency) and the lead angle is determined by the external constant number of TCR terminal.
Configure the gain (the external constant number of TCR terminal) according to the usage conditions and the characteristics of the motor.

The external constant number of TCR terminal can be configured by the following formula.
CR=0.6/ (8×f×ln (5/4))
Recommendation:
R=100kΩ, C < 0.1μF
C' should be configured according to LA of the latter step and the resolution of the A/D conversion of Dif-in.
LA: 156mV/step
Dif-in: 11mV/step

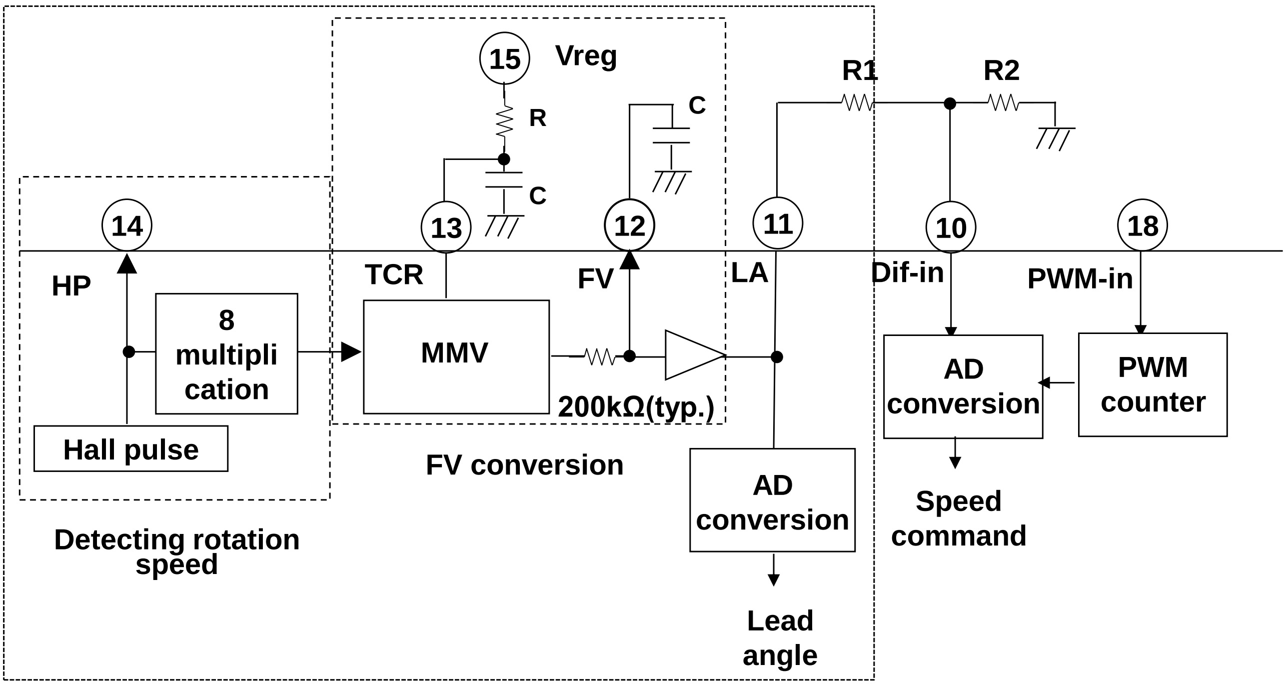


Figure 4.4　Adjustment of auto lead angle

・Speed feedback/Example of setting

As a function of improving the linearity of the rotation number for duty, speed feedback function is introduced.

The TB6605FTG improves the linearity of the rotation number by detecting the speed by the rotation number (HP frequency), converting frequency and voltage, and feed backing the voltage to the speed command (Duty).

Amount of feedback depends on the resistance ratio of R1 and R2 in the above figure. (G=R2/(R1+R2))

The speed feedback and the auto lead angle work at the same time.

5. Power dissipation

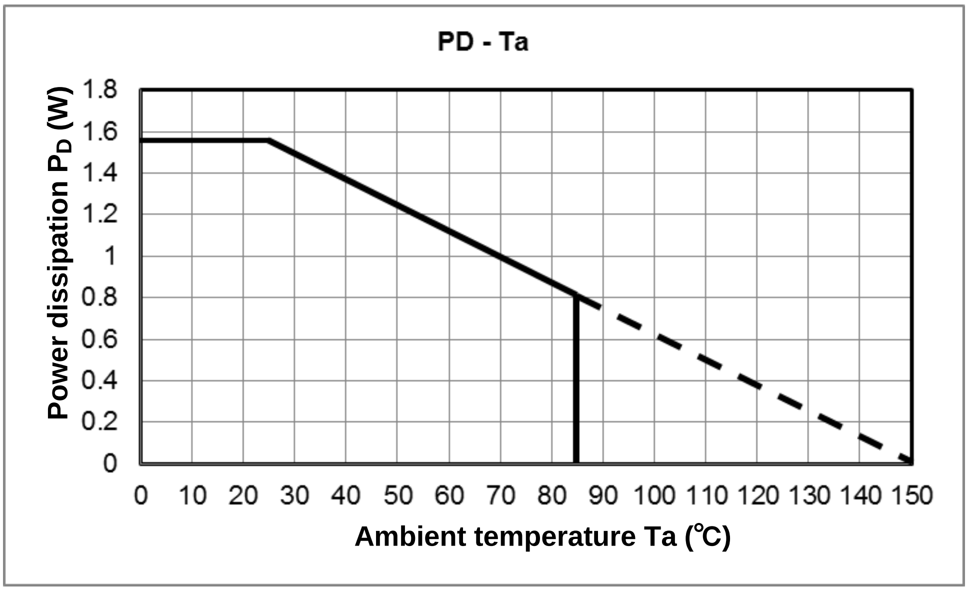


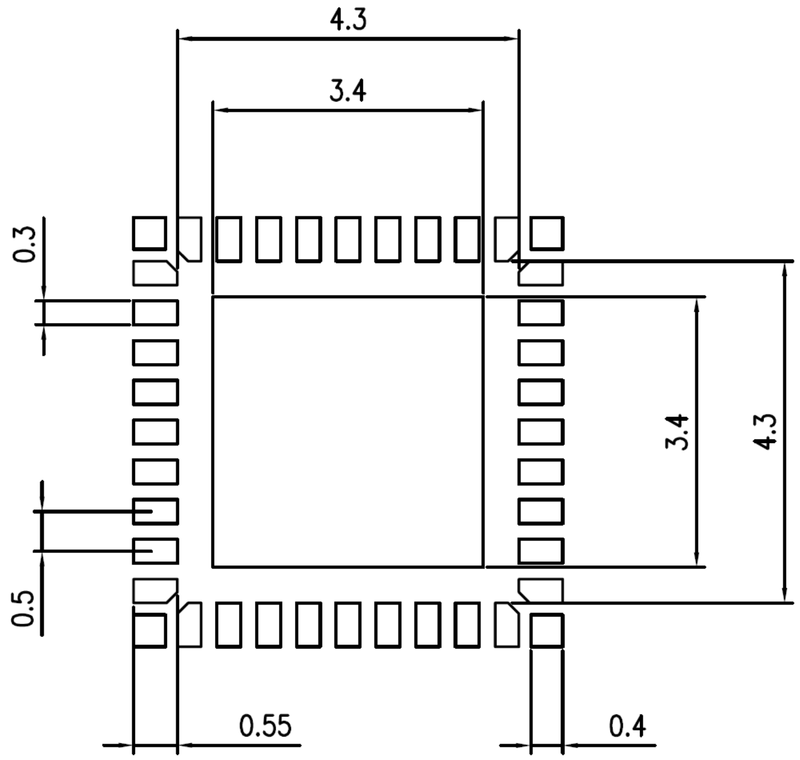
Figure 5.1 Power dissipation

In mounting on board (Single-layer glass-epoxy board: 76.2 mm×114.3 mm×1.6 mm, Cu: 60 %)

6. Notes in designing PCB layout

Please pay attention to the followings in designing layout.

・GND should be solid wired to reduce impedance.
・Output wiring of external FET, power supply line, and GND line, where large current flows, are made as wide as possible.
・The electrolytic capacitor connected to VM terminal should be assigned close to the input terminal as possible. Otherwise, switching noise may increase.
・The GND of the IC and that of the external FET should be connected to a common grounding point not to have common impedance.
・The dimensions of the land pattern for reference is as follows;



"Unit: mm"

Figure 6.1 Dimensions of the land pattern for reference

Notes
・All linear dimensions are given in millimeters unless otherwise specifies.
・This drawing is based on JEITA ET-7501 Level3 and should be treated as a reference only. TOSHIBA is not responsible for any incorrect or incomplete drawings and information.
・You are solely responsible for all aspects of your own land pattern, including but not limited to soldering processes.
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Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

IC Usage Considerations

Notes on handling of ICs

[1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

[2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

[3] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

[4] Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Points to remember on handling of ICs

(1) Over current Protection Circuit

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the over current protection circuits operate against the over current, clear the over current status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_j) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor’s power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device’s motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

(5) Others

Utmost care is necessary in the design of the output, VCC, VM, and GND lines since the IC may be destroyed by short-circuiting between outputs, air contamination faults, or faults due to improper grounding, or by short-circuiting between contiguous pins.

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