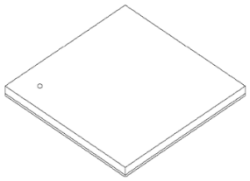
CMOS Digital Integrated Circuit Silicon Monolithic

TC358774XBG/TC358775XBG TC9592XBG/TC9593XBG

Mobile Peripheral Devices

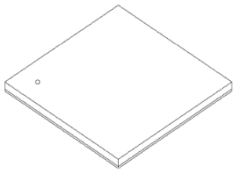
TC358774XBG/TC9592XBG



P-VFBGA49-0505-0.65-001

Weight: 39 mg (typ.)

TC358775XBG/TC9593XBG



P-VFBGA64-0606-0.65-001

Weight: 55 mg (typ.)

Overview

The TC358774XBG/TC358775XBG/TC9592XBG/TC9593XBG Functional Specification defines operation of MIPI® DSI® to LVDS low power chip. Exhibit LVDS Tx block operates at 1.8 V @135 MHz to reduce operation power.

1. Update 4-lane DSI Rx max bit rate @ 1 Gbps/lane to support 1920×1200×24 @60fps
2. Add STBY pin with to enable turning on VDDIO power first before other power supplies.

The primary function of this chip is DSI-to-LVDS Bridge, enabling video streaming output over DSI link to drive LVDS-compatible display panels. The chip supports up to 1600×1200 24-bits per pixel resolution for single-link LVDS and up to WUXGA (1920×1200 24-bits pixels)
resolution for dual-link LVDS. As a secondary function, the chip also supports an I^2C Controller which is controlled by the DSI link; this may be used as an interface to any other control functions through I^2C.

Features

● DSI Receiver

+ Configurable 1- up to 4-Data-Lane DSI Link with bi-directional support on Data Lane 0
+ Maximum bit rate of 1 Gbps/lane
+ Video input data formats:
  - RGB565 16-bits per pixel
  - RGB666 18-bits per pixel
  - RGB666 loosely packed 24-bits per pixel
  - RGB888 24-bits per pixel
+ Video frame size:
  - Up to 1600×1200 24-bits per pixel resolution to single-link LVDS display panel, limited by 135 MHz LVDS speed
  - Up to WUXGA resolutions (1920×1200 24-bits pixels) to dual-link LVDS display panel, limited by 4 Gbps DSI link speed
+ Supports Video Stream packets for video data transmission.
+ Supports generic long packets for accessing the chip's register set

● LVDS FPD Link Transmitter

+ Supports single-link or dual-link
+ Maximum pixel clock frequency of 135 MHz.
+ Maximum pixel clock speed of 135 MHz for single-link or 270 MHz for dual-link
+ Supports display up to 1600×1200 24-bits per pixel resolution for single-link, or up to 1920×1200 24-bits resolutions for dual-link
+ Supports the following pixel formats:
  - RGB666 18-bits per pixel
  - RGB888 24-bits per pixel
+ Features Toshiba Magic Square algorithm which enables a RGB666 display panel to produce a display quality almost equivalent to that of an RGB888 24-bits panel
+ Flexible mapping of parallel data input bit ordering
+ Supports programmable clock polarity
+ Supports two power saving states
  - Sleep state, when receiving DSI ULPS signaling
  - Standby state, entered by STBY pin assertion

● System Operation

+ Host configures the chip through DSI link
+ Through DSI link, Host accesses the chip register set using Generic Write and Read packets. One Generic Long Write packet can write to multiple contiguous register addresses
+ Power management features to save power
+ Configuration registers is also accessible through I^2C Target interface

- **Clock Source**
  - + LVDS pixel clock source is either from external clock EXTCLK or derived from DSICLK.
  - + A built-in PLL generates the high-speed LVDS serializing clock requiring no external components
- **Digital Input/Output Signals**
  - + All Digital Output signals can output ranging from 1.8 V or 3.3 V depending on IO supply voltage
- **Power supply**
  - + MIPI DSI D-PHY^{SM}: 1.2 V
  - + LVDS PHY: 1.8 V
  - + I/O: 1.8 V or 3.3 V (all IO supply pins must be same level)
  - + Digital Core: 1.2 V

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REFERENCE

1. MIPI D-PHY, “MIPI_D-PHY_specification_v01-00-00, May 14, 2009”
2. MIPI Alliance Specification for DSI version 1.01, Feb 2008

1. Introduction

The TC358774XBG/TC358775XBG/TC9592XBG/TC9593XBG Functional Specification defines operation of the DSI TO LVDS low power chip

1. Exhibit LVDS Tx block operates at 1.8 V @135 MHz to reduce operation power
2. Update 4-lane DSI Rx max bit rate @ 1 Gbps/lane to support 1920 × 1200 × 24 @60fps
3. Add STBY pin with to enable turning on VDDIO power first before other power supplies.

The primary function of this chip is DSI-to-LVDS Bridge, enabling video streaming output over DSI link to drive LVDS-compatible display panels. The chip supports up to 1600×1200 24-bits per pixel resolution for single-link LVDS and up to WUXGA (1920×1200 24-bits pixels) resolution for dual-link LVDS.

The chip can be configured through the DSI link by sending write register commands through DSI Generic Long Write-packets. It can also be configured through the I^2C Target interface. I^2C target address of TC358774XBG/TC358775XBG/TC9592XBG/TC9593XBG is 8'b0001_111X, where X = 0/1 for write/read.

This specification provides description of two product versions:

TC358774XBG/TC9592XBG:

In BGA49 package, it supports DSI-RX with up to 4 data lanes, and outputs to Single-Link LVDS.

TC358775XBG/TC9593XBG:

In BGA64 package, it supports DSI-RX with up to 4 data lanes, and outputs to Dual-Link LVDS.

1.1. Scope

This document details the operation of the chip, description of each major function that the chip supports, description of the configuration register set, and includes pinout, package, and electrical characteristics information.

2. Device Overview

The TC358774XBG/TC358775XBG/TC9592XBG/TC9593XBG chip functions primarily as a DSI-to-LVDS communication protocol bridge, enabling video streaming from a Host processor over DSI link to drive LVDS-compatible display panels. In other words, the chip receives video stream input through its DSI receiver (DSI-RX), buffers the received pixel data in a buffer, and then re-transmits the video stream out through the LVDS transmitter.

The chip is configured through the DSI link. Alternatively, it can optionally be configured through the I^2C Target interface.

The reference video pixel clock for the LVDS link is sourced either from an external clock via input pin EXTCLK or derived from DSICLK. The chip integrates a PLL which synthesizes the high-speed clock for use solely to serialize video data over the LVDS link.

The DSI-RX receiver supports from 1- to 4-Lane configurations at bit rate up to 1 Gbps per lane. Host can transmit video in video mode. In video mode, Host controls video timing by sending video frame and line sync events together with video pixel data; video data transmission can be burst or non-burst. Since the chip integrates only 1024-pixel of video buffer, Host still has to take care of transmitting pixel data at appropriate video line time in order to avoid buffer overflow (or underflow).

The LVDS transmitter supports a clock frequency of up to 135 MHz for either single- or dual-link.

The chip supports power management to conserve power when its functions are not in use. Host manages the chip's power consumption states by using ULPS signaling over DSI link and/or STBY pin.

3. Features

- **DSI Receiver**
  - + Configurable 1- up to 4-Data-Lane DSI Link with bi-directional support on Data Lane 0
  - + Maximum bit rate of 1 Gbps/lane
  - + Video input data formats:
    - RGB565 16-bits per pixel
    - RGB666 18-bits per pixel
    - RGB666 loosely packed 24-bits per pixel
    - RGB888 24-bits per pixel
  - + Video frame size:
    - Up to 1600×1200 24-bits per pixel resolution to single-link LVDS display panel, limited by 135 MHz LVDS speed
    - Up to WUXGA resolutions (1920×1200 24-bits pixels) to dual-link LVDS display panel, limited by 4 Gbps DSI link speed
  - + Supports Video Stream packets for video data transmission
  - + Supports generic long packets for accessing the chip's register set

- **LVDS FPD Link Transmitter**
  - + Supports single-link or dual-link
  - + Maximum pixel clock frequency of 135 MHz.
  - + Maximum pixel clock speed of 135 MHz for single-link or 270 MHz for dual-link
  - + Supports display up to 1600×1200 24-bits per pixel resolution for single-link, or up to 1920×1200 24-bits resolutions for dual-link
  - + Supports the following pixel formats:
    - RGB666 18-bits per pixel
    - RGB888 24-bits per pixel
  - + Features Toshiba Magic Square algorithm which enables a RGB666 display panel to produce a display quality almost equivalent to that of an RGB888 24-bits panel
  - + Flexible mapping of parallel data input bit ordering
  - + Supports programmable clock polarity
  - + Supports two power saving states
    - Sleep state, when receiving DSI ULPS signaling
    - Standby state, entered by STBY pin assertion

- **System Operation**
  - + Host configures the chip through DSI link.
  - + Through DSI link, Host accesses the chip register set using Generic Write and Read packets. One Generic Long Write packet can write to multiple contiguous register addresses.
  - + Power management features to save power
  - + Configuration registers is also accessible through I^2C Target interface.

- **Clock Source**
  - + LVDS pixel clock source is either from external clock EXTCLK or derived from DSICLK.
  - + A built-in PLL generates the high-speed LVDS serializing clock requiring no external components

- **Digital Input/Output Signals**
  - + All Digital Output signals can output ranging from 1.8 V or 3.3 V depending on IO supply voltage.

- **Power supply**
  - + MIPI DSI D-PHY: 1.2 V
  - + LVDS PHY: 1.8 V
  - + I/O: 1.8 V or 3.3 V (all IO supply pins must be same level)
  - + Digital Core: 1.2 V

- **Power Consumption**
  - + Power Down State is achieved by:
    1. Reset asserted
    2. EXTCLK not toggling
    3. STBY = 0
    4. DSI in ULPS Drive

Reduced Mode							
	VDDC	VDDS	DSI	LVDS		TOTAL Power	Unit
	VDDC	VDDIO	VDD1	LVDS1.2	LVDS1.8		
	1.2	1.8	1.2	1.2	1.8		V
720×480×18 @26 MHz	8.60	0.11	8.40	3.60	10.00		mA
	10.32	0.20	10.08	4.32	18.00	42.92	mW
1366×768×18 @85 MHz	17.20	0.13	14.60	8.30	11.10		mA
	20.64	0.23	17.52	9.96	19.98	68.33	mW
1920×1080×18 Dual Link @74 MHz	18.57	0.09	19.77	8.12	22.40		mA
	22.28	0.17	23.72	9.75	40.32	96.24	mW
Power Down	0.03	0.01	0.02	0.01	0.02		mA
	0.04	0.02	0.02	0.01	0.04	0.09	mW

4. Pin Layout

A1	A2	A3	A4	A5	A6	A7	A8
VSS_LVDS2_12	LVTX2AN	LVTX2BN	LVTX2CN	LVTX2DN	LVTX2EN	VSS_LVDS2_18	VSS_LVDS1_12
B1	**B2**	**B3**	**B4**	**B5**	**B6**	**B7**	**B8**
VDD_LVDS2_12	LVTX2AP	LVTX2BP	LVTX2CP	LVTX2DP	LVTX2EP	VDD_LVDS2_18	VDD_LVDS1_12
C1	**C2**	**C3**	**C4**	**C5**	**C6**	**C7**	**C8**
VSSIO	VDDIO	STBY	GPIO3	VDD_LVDS2_18	VSS_LVDS2_18	LVTX1AP	LVTX1AN
D1	**D2**	**D3**	**D4**	**D5**	**D6**	**D7**	**D8**
EXTCLK	GPIO2	GPIO1	RESX	TM	VDD_LVDS1_18	LVTX1BP	LVTX1BN
E1	**E2**	**E3**	**E4**	**E5**	**E6**	**E7**	**E8**
VSSC	VDDC	GPIO0	VDDC	VSSC	VSS_LVDS1_18	LVTX1CP	LVTX1CN
F1	**F2**	**F3**	**F4**	**F5**	**F6**	**F7**	**F8**
VSSIO	VDDIO	VDD_MIPI	VSS_MIPI	VSS_MIPI	VDD_MIPI	LVTX1DP	LVTX1DN
G1	**G2**	**G3**	**G4**	**G5**	**G6**	**G7**	**G8**
I2C_SCL	DSRXD0P	DSRXD1P	DSRXCP	DSRXD2P	DSRXD3P	LVTX1EP	LVTX1EN
H1	**H2**	**H3**	**H4**	**H5**	**H6**	**H7**	**H8**
I2C_SDA	DSRXD0M	DSRXD1M	DSRXCM	DSRXD2M	DSRXD3M	VDD_LVDS1_18	VSS_LVDS1_18

Figure 4.1 TC358775XBG/TC9593XBG Chip Pin Layout (BGA64 – Top View)

A1	A2	A3	A4	A5	A6	A7
VSSIO	VDDIO	RESX	GPIO0	VSSC	VDDC	VSSC
B1	**B2**	**B3**	**B4**	**B5**	**B6**	**B7**
EXTCLK	VDDC	VSSC	TM	VDD_LVDS1_12	LVTX1AP	LVTX1AN
C1	**C2**	**C3**	**C4**	**C5**	**C6**	**C7**
I2C_SDA	GPIO3	GPIO2	GPIO1	VSS_LVDS1_12	LVTX1BP	LVTX1BN
D1	**D2**	**D3**	**D4**	**D5**	**D6**	**D7**
I2C_SCL	STBY	VSS_MIPI	VDD_MIPI	VSS_LVDS1_18	LVTX1CP	LVTX1CN
E1	**E2**	**E3**	**E4**	**E5**	**E6**	**E7**
VDDIO	VSSIO	VSS_MIPI	VDD_MIPI	VDD_LVDS1_18	LVTX1DP	LVTX1DN
F1	**F2**	**F3**	**F4**	**F5**	**F6**	**F7**
DSRXD0P	DSRXD1P	DSRXCP	DSRXD2P	DSRXD3P	LVTX1EP	LVTX1EN
G1	**G2**	**G3**	**G4**	**G5**	**G6**	**G7**
DSRXD0M	DSRXD1M	DSRXCM	DSRXD2M	DSRXD3M	VDD_LVDS1_18	VSS_LVDS1_18

Figure 4.2 TC358774XBG/TC9592XBG Chip Pin Layout (BGA49 – Top View)

4.1. TC358775XBG/TC9593XBG BGA64 Pin-out Description

Group	Pin Name	IO Type	Pin Cnt.	Description	Power Supply Voltage
DSI-RX IF	DSRXCP	DSI-PHY	1	DSI clock signal - positive	1.2 V
	DSRXCM	DSI-PHY	1	DSI clock signal - negative	1.2 V
	DSRXD0P	DSI-PHY	1	DSI data lane 0 - positive	1.2 V
	DSRXD0M	DSI-PHY	1	DSI data lane 0 - negative	1.2 V
	DSRXD1P	DSI-PHY	1	DSI data lane 1 - positive	1.2 V
	DSRXD1M	DSI-PHY	1	DSI data lane 1 - negative	1.2 V
	DSRXD2P	DSI-PHY	1	DSI data lane 2 - positive	1.2 V
	DSRXD2M	DSI-PHY	1	DSI data lane 2 - negative	1.2 V
	DSRXD3P	DSI-PHY	1	DSI data lane 3 - positive	1.2 V
	DSRXD3M	DSI-PHY	1	DSI data lane 3 - negative	1.2 V
	VDD_MIPI	Power	2	MIPI Analog Power Supply	1.2 V
	VSS_MIPI	Ground	2	MIPI Analog Ground	GND
1st-Link LVDS-TX IF	LVTX1AP	LVDS-PHY	1	LVDS first-link data channel A - positive	1.8 V
	LVTX1AN	LVDS-PHY	1	LVDS first-link data channel A - negative	1.8 V
	LVTX1BP	LVDS-PHY	1	LVDS first-link data channel B - positive	1.8 V
	LVTX1BN	LVDS-PHY	1	LVDS first-link data channel B - negative	1.8 V
	LVTX1CP	LVDS-PHY	1	LVDS first-link data channel C - positive	1.8 V
	LVTX1CN	LVDS-PHY	1	LVDS first-link data channel C - negative	1.8 V
	LVTX1DP	LVDS-PHY	1	LVDS first-link data channel D (Clock) - positive	1.8 V
	LVTX1DN	LVDS-PHY	1	LVDS first-link data channel D (Clock) - negative	1.8 V
	LVTX1EP	LVDS-PHY	1	LVDS first-link data channel E - positive	1.8 V
	LVTX1EN	LVDS-PHY	1	LVDS first-link data channel E - negative	1.8 V
	VDD_LVDS1_18	Power	2	First-link LVDS 1.8 V Power Supply	1.8 V
	VSS_LVDS1_18	Ground	2	First-link LVDS 1.8 V Ground	GND
	VDD_LVDS1_12	Power	1	First-link LVDS 1.2 V Power Supply	1.2 V
	VSS_LVDS1_12	Ground	1	First-link LVDS 1.2 V Ground	GND
2nd-Link LVDS-TX IF	LVTX2AP	LVDS-PHY	1	LVDS second-link data channel A - positive	1.8 V
	LVTX2AN	LVDS-PHY	1	LVDS second-link data channel A - negative	1.8 V
	LVTX2BP	LVDS-PHY	1	LVDS second-link data channel B - positive	1.8 V
	LVTX2BN	LVDS-PHY	1	LVDS second-link data channel B - negative	1.8 V
	LVTX2CP	LVDS-PHY	1	LVDS second-link data channel C - positive	1.8 V
	LVTX2CN	LVDS-PHY	1	LVDS second-link data channel C - negative	1.8 V
	LVTX2DP	LVDS-PHY	1	LVDS second-link data channel D (Clock) - positive	1.8 V
	LVTX2DN	LVDS-PHY	1	LVDS second-link data channel D (Clock) -negative	1.8 V
	LVTX2EP	LVDS-PHY	1	LVDS second-link data channel E - positive	1.8 V
	LVTX2EN	LVDS-PHY	1	LVDS second-link data channel E - negative	1.8 V
	VDD_LVDS2_18	Power	2	Second-link LVDS 1.8 V Power Supply	1.8 V
	VSS_LVDS2_18	Ground	2	Second-link LVDS 1.8 V Ground	GND
	VDD_LVDS2_12	Power	1	Second-link LVDS 1.2 V Power Supply	1.2 V
	VSS_LVDS2_12	Ground	1	Second-link LVDS 1.2 V Ground	GND
I2C IF	I2C_SCL	S-OD	1	I2C Target interface clock signal	1.8 V or 3.3 V
	I2C_SDA	S-OD	1	I2C Target interface data signal	1.8 V or 3.3 V
GPIO	GPIO[3:0]	N-PD	4	GPIO bits 3-0	1.8 V or 3.3 V
SYSTEM	RESX	N-PD	1	Hardware reset, low active	1.8 V or 3.3 V
	EXTCLK	N-PD	1	External pixel clock source	1.8 V or 3.3 V
	STBY	N	1	Standby pin, low active	1.8 V or 3.3 V
	TM	N-PD	1	Test mode select	1.8 V or 3.3 V
	VDDIO	Power	2	IO Power Supply	1.8 V or 3.3 V
	VSSIO	Ground	2	IO Ground	GND
	VDDC	Power	2	Digital Core Power Supply	1.2 V
	VSSC	Ground	2	Digital Core Ground	GND

Buffer Type Abbreviation:

N: Normal IO
N-PD : Normal IO with Pull Down
S-OD: Pseudo open-drain output, schmitt input
DSI-PHY: front-end analog IO for DSI
LVDS-PHY: front-end analog IO for LVDS

4.2. TC358775XBG/TC9593XBG BGA64 Pin Count Summary

Table 4-1 TC358775XBG/TC9593XBG BGA64 Pin Count Summary

Group Name	Pin Count	Note
DSI-RX IF	14	Include DSI Power & Ground
1st-Link/2nd-Link LVDS-TX IF	32	Include LVDS Power & Ground
I2C IF	2	-
GPIO	4	-
SYSTEM	12	-
Total Pin Count	64	-

4.3. TC358774XBG/TC9592XBG BGA49 Pin-out Description

Group	Pin Name	IO Type	Pin Cnt.	Description	Power Supply Voltage
DSI-RX IF	DSRXCP	DSI-PHY	1	DSI clock signal - positive	1.2 V
	DSRXCM	DSI-PHY	1	DSI clock signal - negative	1.2 V
	DSRXD0P	DSI-PHY	1	DSI data lane 0 - positive	1.2 V
	DSRXD0M	DSI-PHY	1	DSI data lane 0 - negative	1.2 V
	DSRXD1P	DSI-PHY	1	DSI data lane 1 - positive	1.2 V
	DSRXD1M	DSI-PHY	1	DSI data lane 1 - negative	1.2 V
	DSRXD2P	DSI-PHY	1	DSI data lane 2 - positive	1.2 V
	DSRXD2M	DSI-PHY	1	DSI data lane 2 - negative	1.2 V
	DSRXD3P	DSI-PHY	1	DSI data lane 3 - positive	1.2 V
	DSRXD3M	DSI-PHY	1	DSI data lane 3 - negative	1.2 V
	VDD_MIPI	Power	2	MIPI Analog Power Supply	1.2 V
	VSS_MIPI	Ground	2	MIPI Analog Ground	GND
LVDS-TX IF	LVTX1AP	LVDS-PHY	1	LVDS first-link data channel A - positive	1.8 V
	LVTX1AN	LVDS-PHY	1	LVDS first-link data channel A - negative	1.8 V
	LVTX1BP	LVDS-PHY	1	LVDS first-link data channel B - positive	1.8 V
	LVTX1BN	LVDS-PHY	1	LVDS first-link data channel B - negative	1.8 V
	LVTX1CP	LVDS-PHY	1	LVDS first-link data channel C - positive	1.8 V
	LVTX1CN	LVDS-PHY	1	LVDS first-link data channel C - negative	1.8 V
	LVTX1DP	LVDS-PHY	1	LVDS first-link data channel D (Clock) - positive	1.8 V
	LVTX1DN	LVDS-PHY	1	LVDS first-link data channel D (Clock) - negative	1.8 V
	LVTX1EP	LVDS-PHY	1	LVDS first-link data channel E - positive	1.8 V
	LVTX1EN	LVDS-PHY	1	LVDS first-link data channel E - negative	1.8 V
	VDD_LVDS1_18	Power	2	First-link LVDS 1.8 V Power Supply	1.8 V
	VSS_LVDS1_18	Ground	2	First-link LVDS 1.8 V Ground	GND
	VDD_LVDS1_12	Power	1	First-link LVDS 1.2 V Power Supply	1.2 V
	VSS_LVDS1_12	Ground	1	First-link LVDS 1.2 V Ground	GND
I^2C IF	I2C_SCL	S-OD	1	I^2C Target interface clock signal	1.8 V or 3.3 V
	I2C_SDA	S-OD	1	I^2C Target interface data signal	1.8 V or 3.3 V
GPIO	GPIO[3:0]	N-PD	4	GPIO bits 3-0	1.8 V or 3.3 V
SYSTEM	RESX	N-PD	1	Hardware reset, low active	1.8 V or 3.3 V
	EXTCLK	N-PD	1	External pixel clock source	1.8 V or 3.3 V
	STBY	N	1	Standby pin, low active	1.8 V or 3.3 V
	TM	N-PD	1	Test mode select	1.8 V or 3.3 V
	VDDIO	Power	2	IO Power Supply	1.8 V or 3.3 V
	VSSIO	Ground	2	IO Ground	GND
	VDDC	Power	2	Digital Core Power Supply	1.2 V
	VSSC	Ground	3	Digital Core Ground	GND

Buffer Type Abbreviation:

N: Normal IO
N-PD: Normal IO
S-OD: Pseudo open-drain output, schmitt input
DSI-PHY: front-end analog IO for DSI
LVDS-PHY: front-end analog IO for LVDS

4.4. TC358774XBG/TC9592XBG BGA49 Pin Count Summary

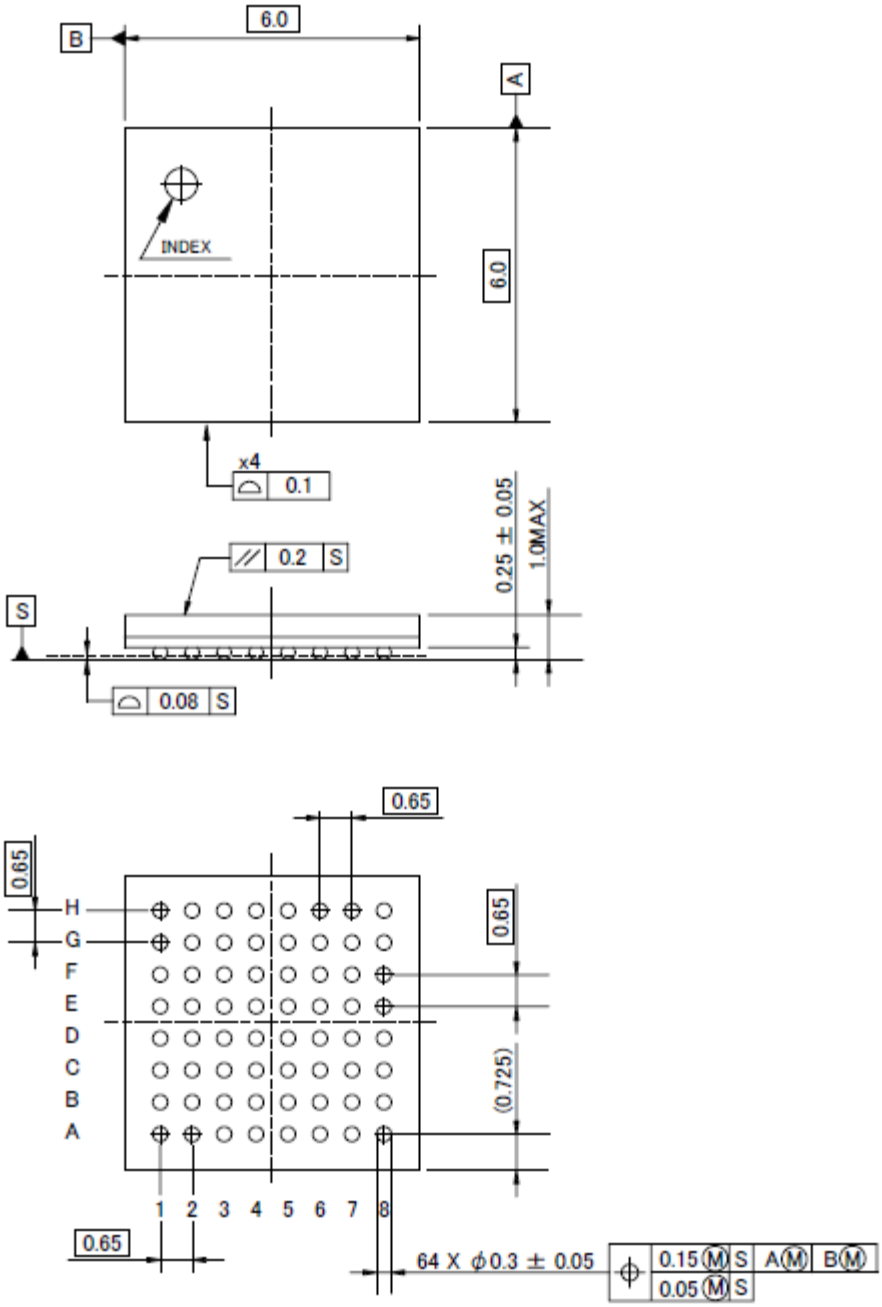
Table 4-2 BGA49 Pin Count Summary

Group Name	Pin Count	Note
DSI-RX IF	14	Include DSI Power & Ground
LVDS-TX IF	16	Include LVDS Power & Ground
I^2C IF	2	-
GPIO	4	-
SYSTEM	13	-
Total Pin Count	49	-

5. Package

P-VFBGA64-0606-0.65-001

(Unit: mm)

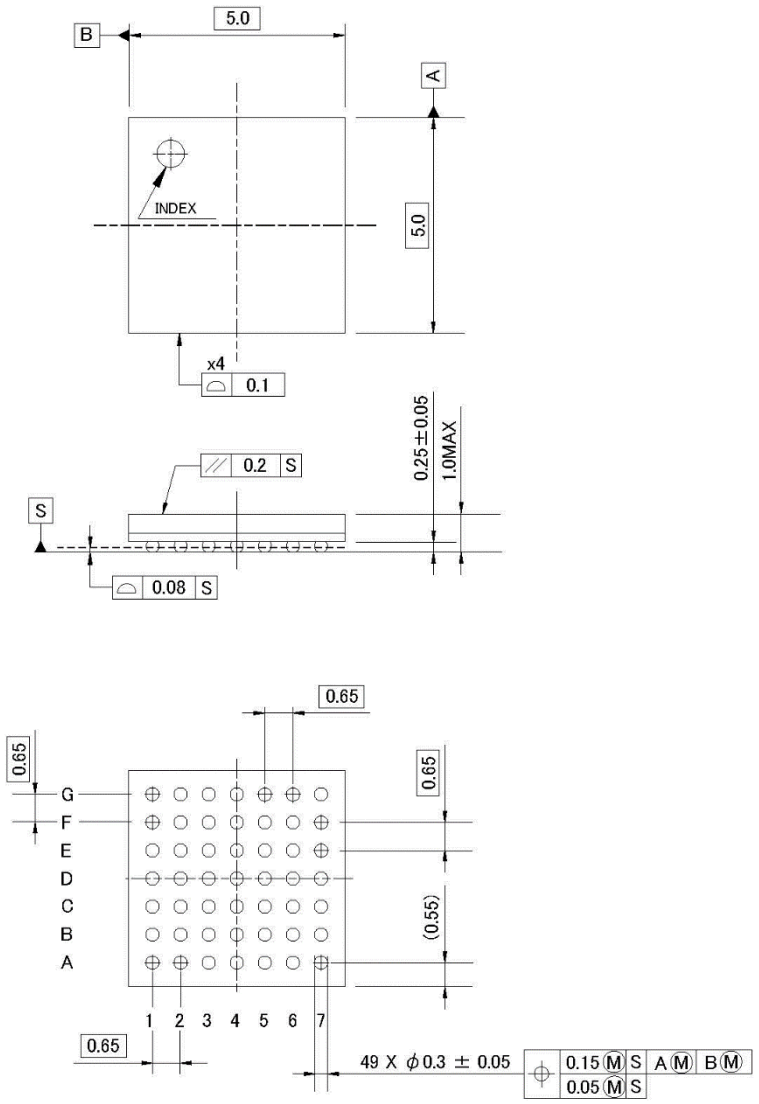


Weight: 55 mg (typ.)

Figure 5.1 TC358775XBG/TC9593XBG (P-VFBGA64-0606-0.65-001) Package Drawing

P-VFBGA49-0505-0.65-001

(Unit: mm)



Weight: 39 mg (typ.)

Figure 5.2 TC358774XBG/TC9592XBG (P-VFBGA49-0505-0.65-001) Package Drawing

Table 5-1 Information Summary

	TC358775XBG TC9593XBG Package	TC358774XBG TC9592XBG Package
Package Type	VFBGA	VFBGA
Ball Diameter	0.3 mm	0.3 mm
Ball Pitch (e)	0.65 mm	0.65 mm
Edge Ball center to center (E1 × D1)	4.55 mm × 4.55 mm	3.90 mm × 3.90 mm
Body Size (E × D)	6 mm × 6 mm	5 mm × 5 mm
Thickness (A)	1 mm	1 mm

6. Electrical characteristics

6.1. Absolute Maximum Ratings

Table 6-1 Absolute Maximum Ratings

VSSC = 0V

Parameter	Symbol	Rating	Unit
Supply voltage (1.8 V – Digital IO)	VDDIO	-0.3 to +3.9	V
Supply voltage (1.2 V – Digital Core)	VDDC	-0.3 to +1.8	V
Supply voltage (1.2 V – MIPI DSI PHY)	VDD_MIPI	-0.3 to +1.8	V
Supply voltage (1.8 V – LVDS PHY)	VDD_LVDS1_18, VDD_LVDS2_18	-0.3 to +3.9	V
Supply voltage (1.2 V – LVDS PHY)	VDD_LVDS1_12 VDD_LVDS2_12	-0.3 to +1.8	V
Input voltage (DSI I/O)	V_{IN_DSI}	-0.3 to VDD_MIPI +0.3	V
Output voltage (DSI I/O)	V_{OUT_DSI}	-0.3 to VDD_MIPI +0.3	V
Input voltage (Digital IO)	V_{IN_IO}	-0.3 to VDDIO +0.3	V
Output voltage (Digital IO)	V_{OUT_IO}	-0.3 to VDDIO +0.3	V
Output voltage (LVDS Driver)	V_{OUT_LVDS}	-0.3 to VDD_LVDS_18 +0.3	V
Input current	I_{in}	-10 to +10	mA
Storage temperature	T_{stg}	-40 to 125	°C

6.2. Operating Conditions

Table 6-2 Operating Conditions

VSSC = 0V

Parameter	Symbol	Min	Typ.	Max	Unit
Supply voltage (1.8 V – Digital IO)	VDDIO	1.7	1.8	1.9	V
Supply voltage (3.3 V – Digital IO)	VDDIO	3.0	3.3	3.6	V
Supply voltage (1.2 V – Digital Core)	VDDC	1.1	1.2	1.3	V
Supply voltage (1.2 V – LVDS PHY)	VDD_LVDS_12	1.1	1.2	1.3	V
Supply voltage (1.8 V – LVDS PHY)	VDD_LVDS_18	1.7	1.8	1.9	V
Supply voltage (1.2 V – MIPI-DSI PHY)	VDD_MIPI	1.1	1.2	1.3	V
Operating temperature (ambient temperature with voltage applied) for TC358774XBG/TC358775XBG	T_a	-30	+25	+85	°C
Operating temperature (ambient temperature with voltage applied) for TC9592XBG/TC9593XBG	T_a	-40	+25	+85	°C

6.3. DC Electrical Specification

All typical values are at normal operating conditions unless otherwise specified.

6.3.1. Normal CMOS I/Os DC Specifications

Table 6-3 Normal CMOS IOs DC Specifications

Parameter – CMOS I/Os	Symbol	Conditions	Min	Typ.	Max	Unit
Input voltage, High level Input (Note 1)	V_{IH}	-	0.7 VDDIO	-	VDDIO	V
Input voltage, Low level Input (Note 1)	V_{IL}	-	0	-	0.3 VDDIO	V
Input voltage High level CMOS Schmitt Trigger (Note 1)	V_{IHS}	-	0.7 VDDIO	-	VDDIO	V
Input voltage Low level CMOS Schmitt Trigger (Note 1)	V_{ILS}	-	0	-	0.3 VDDIO	V
Output voltage, Low level (Note 1), (Note 2)	V_{OL}	I_{OL} = 2 mA	0	-	0.2 VDDIO	V
Input leakage current, High level on Normal pin	I_{ILH1} (Note 3)	V_{IN} = +VDDIO, VDDIO = 3.6 V	-10	-	10	µA
Input leakage current, High level on Pull-down I/O pin	I_{ILH2} (Note 3)	V_{IN} = +VDDIO, VDDIO = 3.6 V	-	-	100	µA
Input leakage current, Low level On Normal pin or Pull-down I/O pin	I_{ILL1} (Note 4)	V_{IN} = 0 V, VDDIO = 3.6 V	-10	-	10	µA

Note 1: Each power source is operating within recommended operating condition.

Note 2: Current output value is specified to each IO buffer individually. Output voltage changes with output current value.

Note 3: Normal I/O pin applied VDDIO supply voltage to Vin (input voltage).

Note 4: Normal pin, or Pull-down I/O pin applied VSSIO (0 V) to Vin (input voltage).

6.3.2. DSI Differential I/Os DC Specifications

6.3.2.1 LP Transmitter

The low power transmitter is used for driving the lines in all low-power operating modes. The DC characteristics of the LP transmitter are given below.

Table 6-4 DSI LP Transmitter DC Specifications

Parameter	Symbol	Min	Typ.	Max	Unit
Thevenin output low level	V_{OL}	-50	-	50	mV
Output impedance of the LP transmitter	Z_{OLP}	110	-	-	Ω

6.3.2.2 HS Receiver

The high-speed receiver is a differential line receiver with a switch able parallel input termination. It is used to receive data during high speed transmission from the host. The DC characteristics of the HS receiver are given below.

Table 6-5 DSI HS Receiver DC Specifications

Parameter	Symbol	Min	Typ.	Max	Unit
Common-mode voltage HS receive mode	$V_{CMRX(DC)}$	70	-	330	mV
Differential input high threshold	V_{IDTH}	-	-	70	mV
Differential input low threshold	V_{IDTL}	-70	-	-	mV
Single-ended input high voltage	V_{IHHS}	-	-	460	mV
Single-ended input low voltage	V_{ILHS}	-40	-	-	mV
Single-ended threshold for HS termination enable	$V_{TERM-EN}$	-	-	450	mV
Differential input impedance	Z_{ID}	80	100	125	Ω

6.3.2.3 LP Receiver

The low-power receiver is used to detect the Low-Power state on each pin. It is used to receive data during low speed transmission from the host. The DC characteristics of the LP receiver are given below.

Table 6-6 DSI LP Receiver DC Specifications

Parameter	Symbol	Min	Typ.	Max	Unit
Logic 1 input voltage	V_{IH}	880	-	-	mV
Logic 0 input voltage	V_{IL}	-	-	550	mV

6.3.3. LVDS Transmitter DC Specifications

Table 6-7 LVDS Transmitter DC Specifications

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Output differential voltage Normal	$\|V_{OD}\|$	RLOAD = 100 Ω ± 1%	150	300	450	mV
Output differential voltage Reduced	$\|V_{OD}\|$	RLOAD = 100 Ω ± 1%	115	180	300	mV
Change in $\|V_{OD}\|$ between “0”and “1”	ΔV_{OD}	RLOAD = 100 Ω ± 1%	-	-	30	mV
Output offset voltage	V_{OS}	RLOAD = 100 Ω ± 1%	800	900	1000	mV
Change in V_{OS} between “0”and “1”	ΔV_{OS}	RLOAD = 100 Ω ± 1%	-	-	25	mV
Output current	I_{sab}	Driver shorted together	-	-	12	mA
Output current	I_{sab}, I_{sb}	Driver shorted to ground	-	-	30	mA

7. Revision History

Table 7-1 Revision History

Revision	Date	Description
1.5	2014-04-10	Newly released
1.5.1	2016-02-18	Package name and its drawing is modified. • TC358774XBG → P-VFBGA49-0505-0.65-001 • TC358775XBG → P-VFBGA64-0606-0.65-001
1.7b	2017-07-01	Added Table number as Table 6.7. Changed header, footer and the last page. Changed corporate name.
1.9	2026-04-14	Modified descriptions of services mark and trademark. Added service marks. Corrected typos. Modified Note numbers in Tabel 6.3. Corrected weights of TC358774XBG and TC358775XBG. Revised the last page “RESTRICTIONS ON PRODUCT USE” and added URL.
1.9.1	2020-01-15	IO type Correction in Section 4.1 and 4.3. IILL2 spec. to be deleted from Table 6.3.
1.9.2	2020-12-16	Corrected typo in Table 6.1
2.00	2026-04-14	Marged with TC9592XBG and TC9593XBG Updated the terms "Master/Slave" to "Controller/Target" Corrected typos Removed 1.2 Purpose Removed I2C Controller function Removed Precautions and Usage Considerations Revised the last page “RESTRICTIONS ON PRODUCT USE”

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