32-bit RISC Microcontroller

TMPM4K Group(1)

Reference manual

Memory Map

(MMAP-M4K(1))

Revision 2.0

2018-05

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

Contents

List of Figures

List of Tables

Preface

Related document

Document name
Arm documentation set for the Arm Cortex-M4(with FPU)

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C …
  Example: ***[ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]***
  In case of channel, "x" means 0, 1, and 2…
  Example: ***[T32A0RUNA], [T32A1RUNA], [T32A2RUNA] → [T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-ENC	Advanced Encoder input Circuit
AO	Constant energization region(8bit Bus)
APB	Advanced Peripheral Bus
A-PMD	Advanced Programmable Motor Control Circuit
A-VE+	Advanced Vector Engine Plus
CG	Clock control and Operation mode
CRC	Cyclic Redundancy Check
DMAC	Direct Memory Access Controller
DNF	Digital Noise Filter
I^2C	Inter-Integrated Circuit
IA(INT-I/F)	Interrupt control register A
IB(INT-I/F)	Interrupt control register B
IO	IO Bus(32bit Peripheral Bus)
IMN	Interrupt Monitor
LVD	Voltage Detection Circuit
NBDIF	Non Break Debug Interface
OFD	Oscillation Frequency Detector
OPAMP	Operational Amplifier
POR	Power On Reset Circuit
RAMP	RAM Parity
RLM	Low speed oscillation / power supply control / reset
SIWDT	Clock Selective Watchdog timer
TRGSEL	Trigger Selection circuit
TRM	Trimming circuit
TSPI	Toshiba Serial Peripheral Interface
T32A	32-bit Timer Event counter
UART	Universal Asynchronous Receiver Transmitter

1. Memory Map

The memory maps for TMPM4K Group(1) are based on the Arm® Cortex®-M4(with FPU) processor core memory map.

The internal ROM, internal RAM and special function registers (SFR) of TMPM4K Group(1) are mapped to the Code, SRAM and peripheral regions of the Cortex-M4(with FPU) respectively. The special function register (SFR) means the control registers of all input/output ports and peripheral functions.

The CPU register area is the processor core's internal register region.

For more information on each region, see the "Arm documentation set for the Arm Cortex-M4".

Note that access to regions indicated as "Fault" causes a memory fault if memory faults are enabled, or causes a hard fault if memory faults are disabled. Also, do not access the vendor-specific region.

1.1. TMPM4KxFYA

- Code Flash : 256KB
- RAM : 18KB
- Product : TMPM4K4FYAUG, TMP4K4FYAFG, TMPM4K2FYADUG, TMPM4K1FYAUG

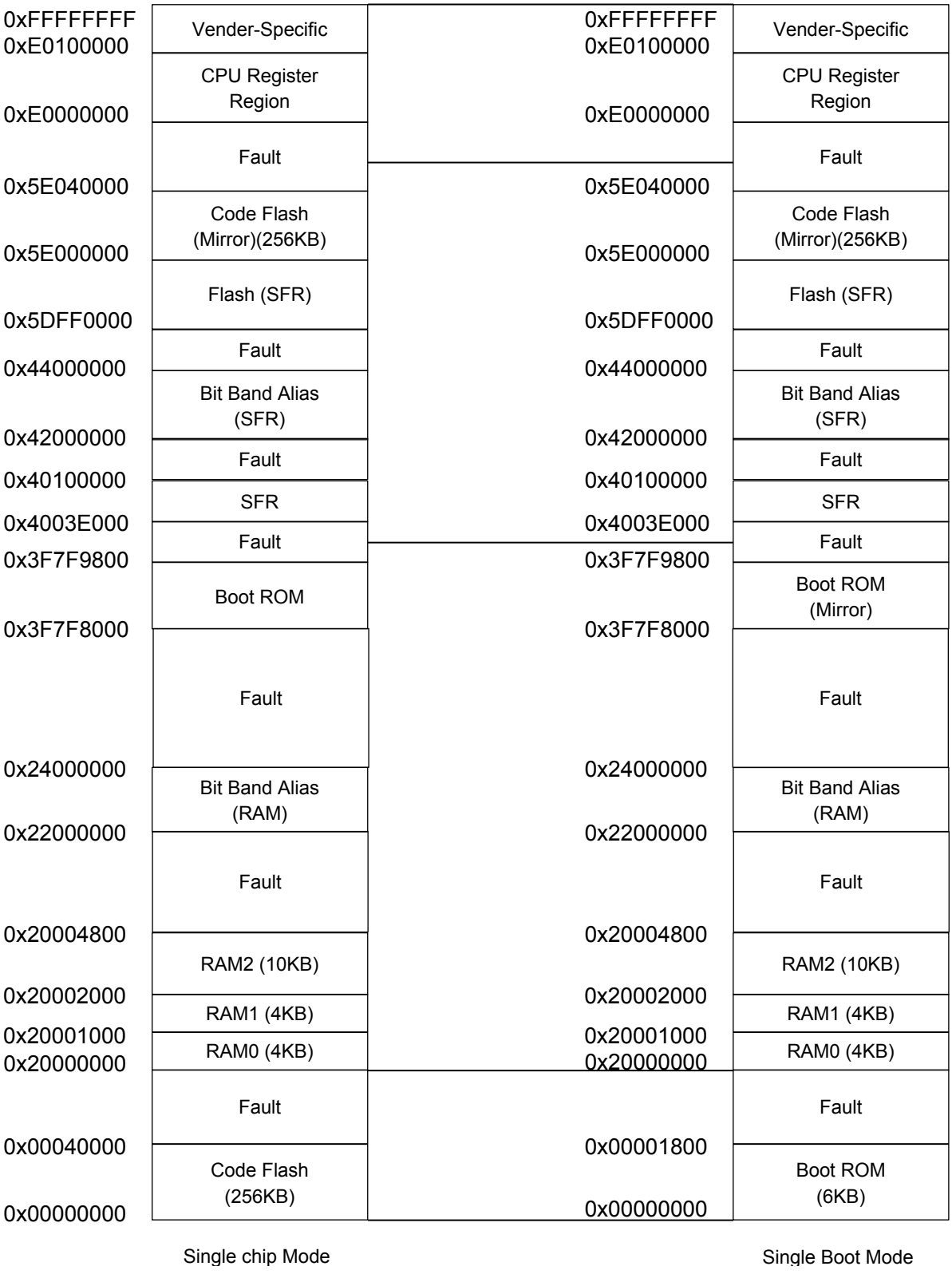

Figure 1.1 TMPM4KxFYA

1.2. TMPM4KxFWA

- Code Flash : 128KB
- RAM : 18KB
- Products : TMPM4K4FWAUG, TMP4K4FWAFG, TMPM4K2FWADUG, TMPM4K1FWAUG

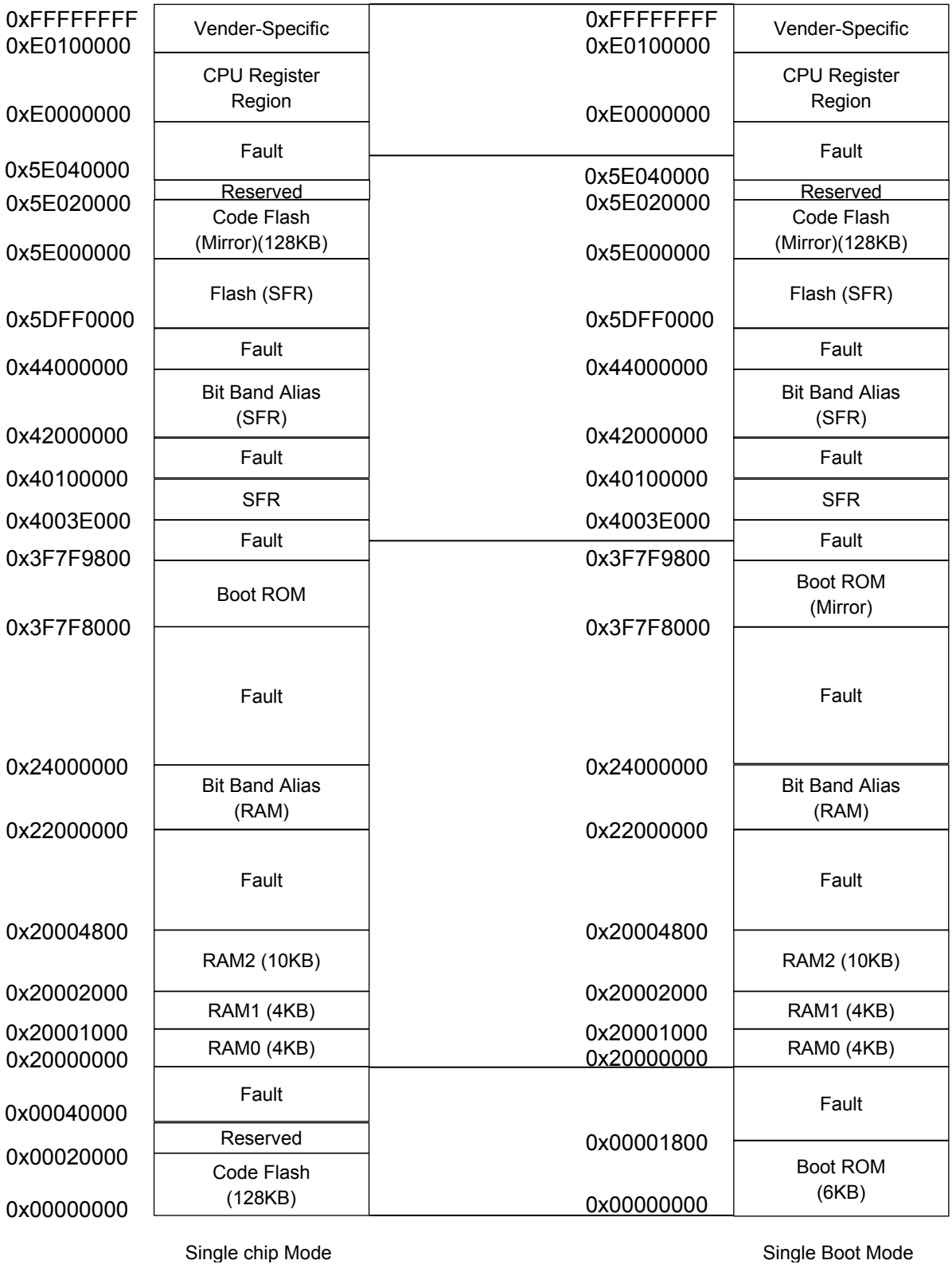

Figure 1.2 TMPM4KxFWA

1.3. TMPM4KxFUA

- Code Flash : 96KB
- RAM : 18KB
- Products : TMPM4K4FUAUG, TMP4K4FUAFG, TMPM4K2FUADUG, TMPM4K1FUAUG

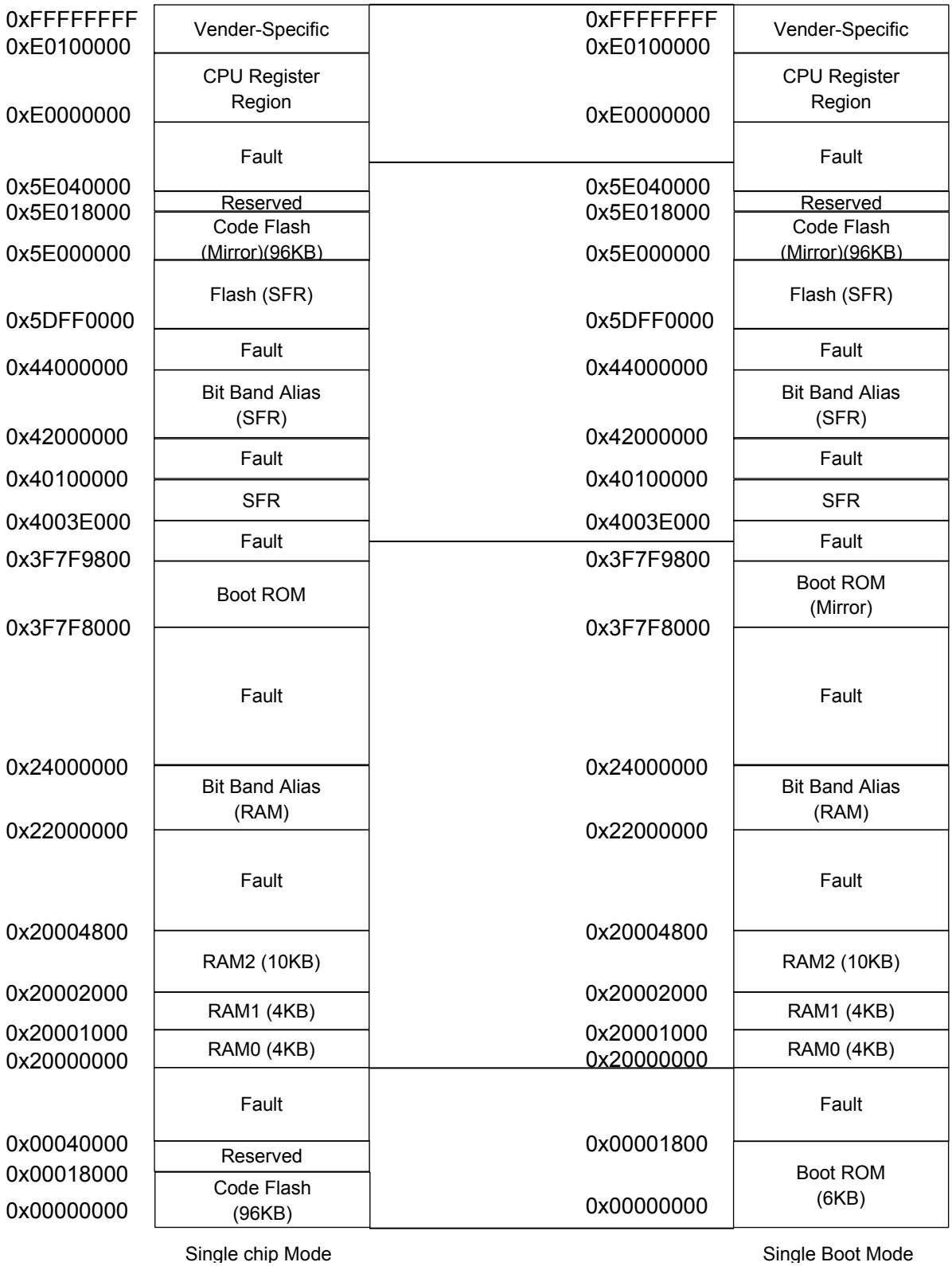

Figure 1.3 TMPM4KxFUA

1.4. TMPM4KxFSA

- Code Flash : 64KB
- RAM : 18KB
- Products : TMPM4K4FSAUG, TMPM4K4FSAFG, TMPM4K2FSADUG, TMPM4K1FSAUG, TMP4K0FSADUG

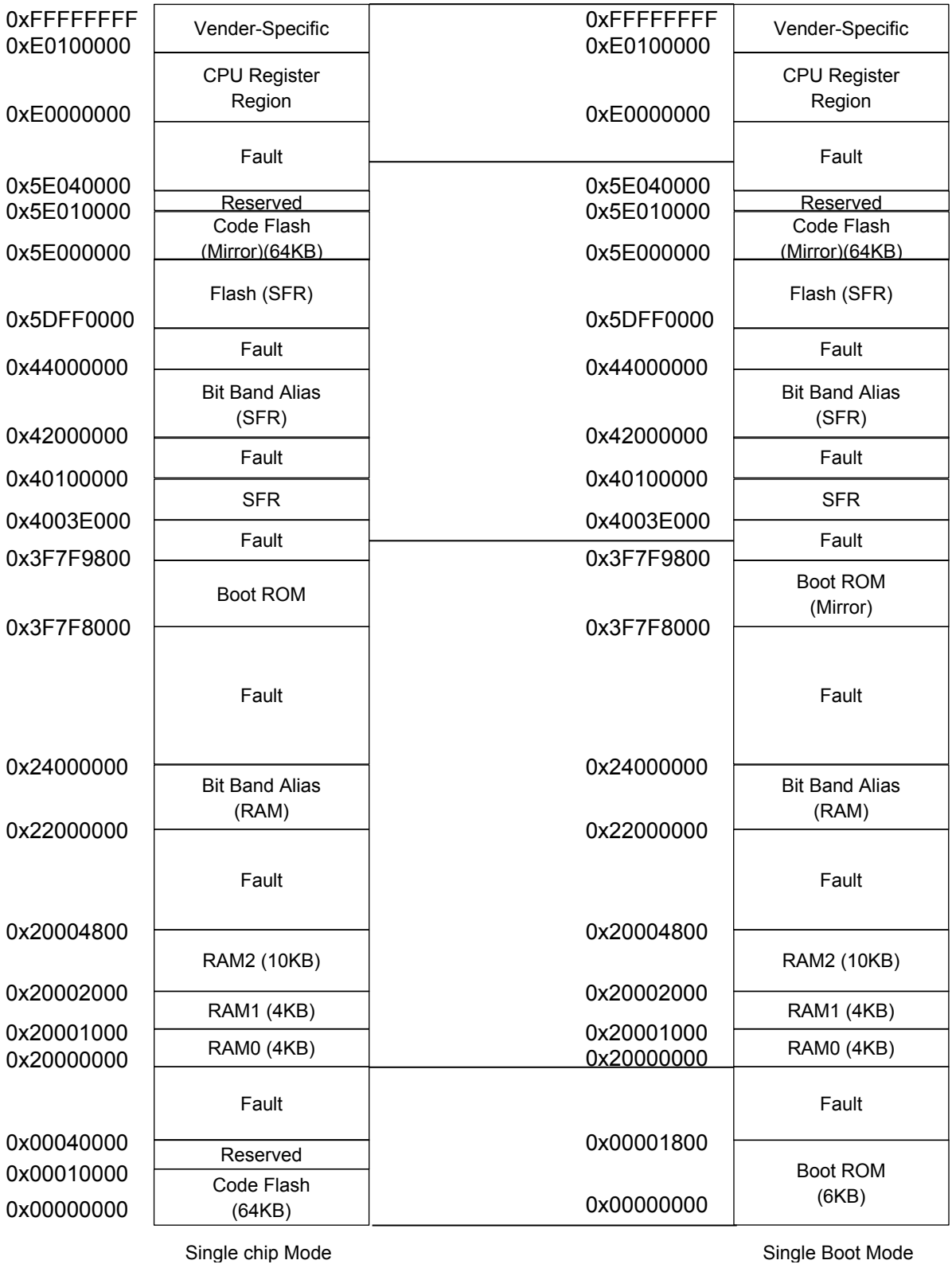

Figure 1.4 TMPM4KxFSA

2. Bus Matrix

TMPM4K Group(1) contains three bus masters such as a CPU core, DMA controller and NBDIF.

Bus masters connect to slave ports (S0 to S4) of Bus Matrix. In the bus matrix, master ports (M0 to M12) connect to peripheral functions via connections described as (○) or (●) in the following figure. (●) shows a connection to a mirror area.

While multiple slaves are connected to the same bus master line in the Bus Matrix, if multiple slave accesses are generated at the same time, a priority is given to access from a master with the smallest slave number.

2.1. Structure

2.1.1. Single chip mode

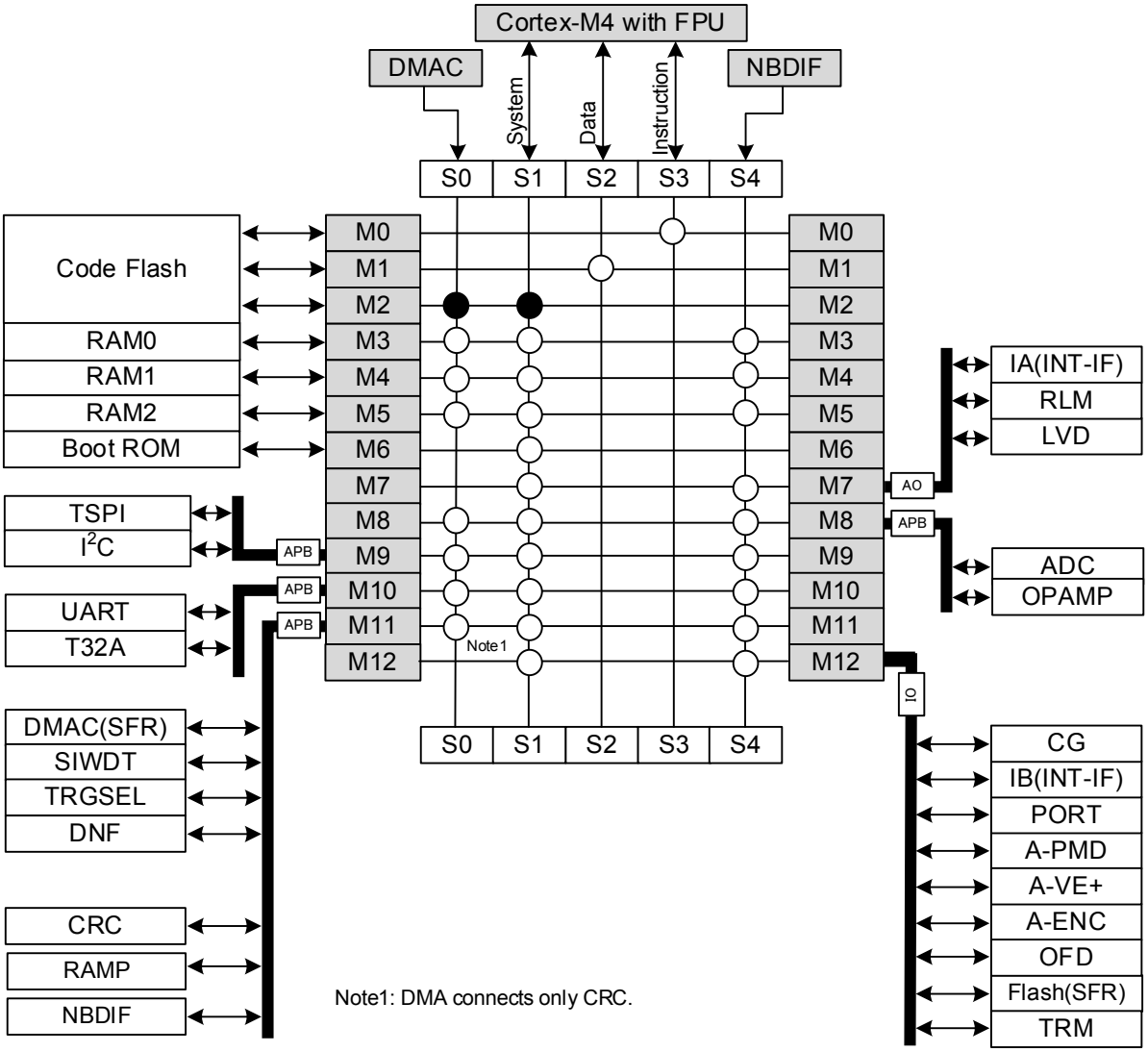

Figure 2.1 Single chip mode

2.1.2. Single boot mode

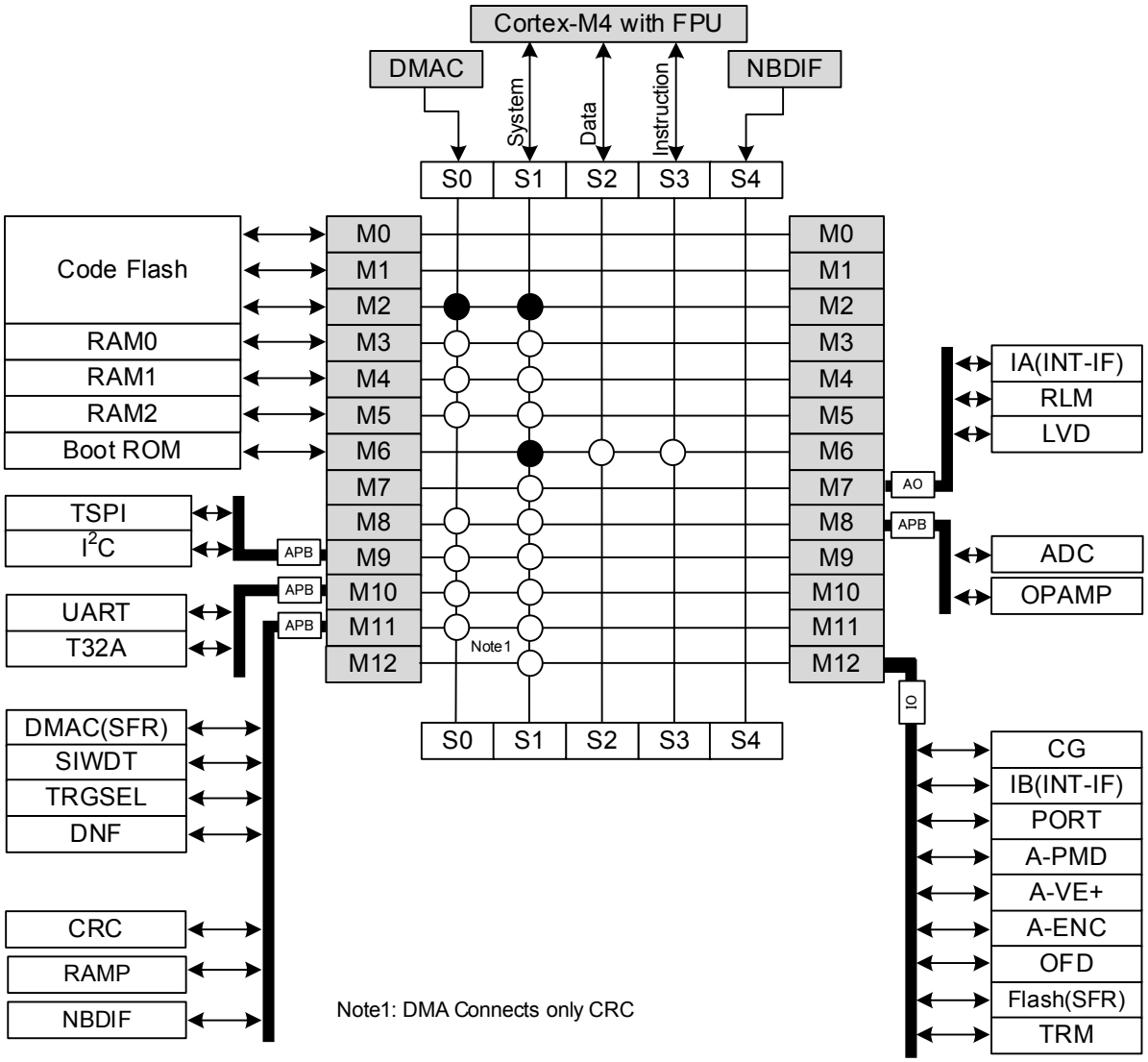

Figure 2.2 Single boot mode

2.2. Connection table

2.2.1. Code area / SRAM area

(1) Single chip mode

Table 2.1 Single chip mode

Start Address	Slave		Master				
			DMAC	Core S-Bus	Core D-Bus	Core I-Bus	NBDIF
			S0	S1	S2	S3	S4
0x00000000	Code Flash	M0	Fault	-	Fault	✓	Fault
		M1	Fault	-	✓	Fault	Fault
0x00040000	Fault	-	Fault	-	Fault	Fault	Fault
0x20000000	RAM0	M3	✓	✓	-	-	✓
0x20001000	RAM1	M4	✓	✓	-	-	✓
0x20002000	RAM2	M5	✓	✓	-	-	✓
0x20004800	Fault	-	Fault	Fault	-	-	Fault
0x22000000	Bit band alias	-	Fault	✓	-	-	Fault
0x24000000	Fault	-	Fault	Fault	-	-	Fault
0x3F7F8000	Boot ROM(Mirror)	M6	Fault	✓	-	-	Fault
0x5E000000	Code Flash (Mirror)	M2	✓	✓	-	-	Fault

✓: Accessible ,-: Not accessible, Fault: Bus error

(2) Single boot mode

Table 2.2 Single boot mode

Start Address	Slave		Master				
			DMAC	Core S-Bus	Core D-Bus	Core I-Bus	NBDIF
			S0	S1	S2	S3	S4
0x00000000	Boot ROM	M6	Fault	-	✓	✓	Fault
0x00001800	Fault	-	Fault	-	Fault	Fault	Fault
0x20000000	RAM0	M3	✓	✓	-	-	✓
0x20001000	RAM1	M4	✓	✓	-	-	✓
0x20002000	RAM2	M5	✓	✓	-	-	✓
0x20004800	Fault	-	Fault	Fault	-	-	Fault
0x22000000	Bit band alias	-	Fault	✓	-	-	Fault
0x24000000	Fault	-	Fault	Fault	-	-	Fault
0x3F7F8000	Boot ROM(Mirror)	M6	Fault	✓	-	-	Fault
0x5E000000	Code Flash (Mirror)	M2	✓	✓	-	-	Fault

✓: Accessible ,-: Not accessible, Fault: Bus error

2.2.2. Peripheral area / External bus area

Table 2.3 Peripheral area / External bus area

Start Address	Slave		Master				
			DMAC	Core S-Bus	Core D-Bus	Core I-Bus	NBDIF
			S0	S1	S2	S3	S4
0x40000000	Fault	-	Fault	Fault	-	-	Fault
0x4003E000	IA(INTIF)	M7	Fault	✓	-	-	✓
0x4003E400	RLM		Fault	✓	-	-	✓
0x4003EC00	LVD		Fault	✓	-	-	✓
0x4004C000	DMAC(SFR)	M11	Fault	✓	-	-	✓
0x40054000	Fault	-	Fault	Fault	-	-	Fault
0x40098000	TSPI (ch0 to 3)	M9	✓	✓	-	-	✓
0x400A0000	I^2C (ch0)	M9	✓	✓	-	-	✓
0x400B8700	ADC	M8	✓	✓	-	-	✓
0x400BA000	T32A (ch0 to 5)	M10	✓	✓	-	-	✓
0x400BB000	UART (ch0 to 3)	M10	✓	✓	-	-	✓
0x400BB400	SIWDT	M11	Fault	✓	-	-	✓
0x400BB600	DNF		Fault	✓	-	-	✓
0x400BB800	TRGSEL	M11	Fault	✓	-	-	✓
0x400BBA00	NBDIF		Fault	✓	-	-	✓
0x400BBB00	RAMP		Fault	✓	-	-	✓
0x400BBC00	CRC		✓	✓	-	-	✓
0x400BC000	OPAMP	M8	✓	✓	-	-	✓
0x400BC100	Fault	-	Fault	Fault	-	-	Fault
0x400C0000	PORT	M12	Fault	✓	-	-	✓
0x400CC000	Fault	-	Fault	Fault	-	-	Fault
0x400F1000	OFD	M12	Fault	✓	-	-	✓
0x400F3000	CG		Fault	✓	-	-	✓
0x400F3200	TRM		Fault	✓	-	-	✓
0x400F4E00	IB(INTIF)		Fault	✓	-	-	✓
0x400F4F00	IMN		Fault	✓	-	-	✓
0x400F6000	A-PMD(ch0 to 1)		Fault	✓	-	-	✓
0x400F7000	A-ENC		Fault	✓	-	-	✓
0x400F8000	A-VE+		Fault	✓	-	-	✓
0x40100000	Fault	-	Fault	Fault	-	-	Fault
0x42000000	Bit Band Alias	-	Fault	✓	-	-	Fault
0x44000000	Fault	-	Fault	Fault	-	-	Fault
0x5DFF0000	Flash(SFR)	M12	Fault	✓	-	-	✓
0x5E040000	Fault	-	Fault	Fault	-	-	Fault

✓: Accessible ,-: Not accessible, Fault: Bus error

3. Revision History

Table 3.1 Revision History

Revision	Date	Description
1.0	2017-11-01	First release
2.0	2018-05-08	Terms and Abbreviations Modified CG description, Deleted DAC, Modified NBD to NBDIF RAM Parity to RAMP, Added RAMP,OPAMP 2.1.1 Single chip mode Figure2.1 Modified NBD to NBDIF,AMP to OPAMP RAM Parity RAMP 2.1.2 Single boot mode Figure2.2 Modified NBD to NBDIF,AMP to OPAMP RAM Parity to RAMP 2.2.1 Code area / SRAM area Modified NBD to NBDIF Table 2.1 (added Code-Flash(M2) row, correction of Fault status to "-" in some S/D/I-Bus) Table2.2 (added Code-Flash(M2) row, correction of Fault status to "-" in some S/D/I-Bus) 2.2.2 Peripheral area / External bus area Table2.3 (deleted Code-Flash(M2) row, correction of Fault status to "-" in D/I-Bus), Modified NBD to NBDIF, AMP to OPAMP, RAM Parity to RAMP

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