32-bit RISC Microcontroller

TMPM4K Group(1)

Reference Manual
Input/Output Ports
(PORT-M4K(1))

Revision 2.1

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TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0] → [ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA] → [T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> =0x01 (hexadecimal), ***[XYZn]***<VW> =1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value.
  In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviations

Some of abbreviations used in this document are as follows:

JTAG	Joint Test Action Group
NBDIF	Non Break Debug Interface
SW	Serial Wire

1. Outlines

It is described about the register and setting of port. A list of the functions is indicated below.

Function Classification	Function	Description
Port	-	Programmable pull-up/Programmable pull-down/Open-drain output are possible.
Peripheral Function pins	Clock Output	System clock output is possible.
	External Interrupt	Interrupt pin has a noise filter(Filter width 30ns Typ.).
	32-bit Timer Event Counter	Input capture input pin. Timer output pin.
	Serial Peripheral Interface	Data input pin, Data output pin, Clock input/output pin
	Asynchronous Serial Communication Circuit	Data input pin, Data output pin, Handshake function pins.
	I^2C Interface	Data input/output pin, Clock input/output pin
	Analog Digital Convertor	Analog input pin
	Advanced Programmable Motor Control Circuit	X/Y/Z phase output pins, U/V/W phase output pins, EMG detection input pin, Overvoltage detection input pin.
	Advanced Encoder Input Circuit	Encoder input pin
	Trigger Input	External trigger input pin
Debug pin	JTAG	Test select input pin, Serial clock input pin, Serial data output pin, Serial data input pin, Test reset pin
	SW	Serial wire data input/output pin, Serial wire clock input pin, Serial wire viewer output pin
	Trace	Trace clock output pin, Trace data output 4pins.
	NBDIF	NBD synchronous input pin, NBD clock input pin, NBD data Input/output 4pins.
Control pin	High speed clock	High speed resonator connection pin / External Clock signal input pin
	BOOT mode control	BOOT mode control pin

2. Function

2.1. Clock supply

When you use Port, please set an applicable clock enable bit to 1 (clock supply) in fsys supply stop registers A or B (***[CGFSYSENA]***, ***[CGFSYSENB]***), fc supply stop register (***[CGFCEN]***). The corresponding registers and the bit locations depend on a product. Some products do not have all registers. For the details, refer to “Clock Control and Operation Mode” in Reference manual.

3. Signal connection list

This table is sorted the function pins by the signal name of the block diagram which is described each reference manual. Register setting of the peripherals function is being explained in the port order, so please use for a reverse lookup of port name.

The numerical value shows the pin number.

Table 3.1 Signal connection list (1/5)

Related Reference Manual	Function pin name	Port name	M4K4 (LQFP64)	M4K2 (LQFP48)	M4K1 (LQFP44)	M4K0 (LQFP32)
Asynchronous Serial Communication Circuit	UT0RXD	PK0	63	48	43	31
		PK1	64	1	44	32
		PK2	1	2	1	1
		PK3	2	3	2	2
	UT0TXDA	PK1	64	1	44	32
		PK0	63	48	43	31
		PK3	2	3	2	2
		PK2	1	2	1	1
	UT1RXD	PA1	18	13	-	-
		PA0	19	14		
	UT1TXDA	PA0	19	14		
		PA1	18	13		
	UT2RXD	PG1	57	42	40	28
	UT2TXDA	PG0	56	41	39	27
	UT3RXD	PC1	34	-	-	-
		PC0	35			
	UT3TXDA	PC0	35			
		PC1	34			
I^2C Interface	I2C0SDA	PB0	31	23	22	-
	I2C0SCL	PB1	32	24	23	
Serial Peripheral Interface	TSPI0RXD	PK2	1	2	1	-
	TSPI0TXD	PK3	2	3	2	
	TSPI0SCK	PK4	3	4	3	
	TSPI1RXD	PA1	18	-	-	-
	TSPI1TXD	PA0	19			
	TSPI1SCK	PA2	20			
	TSPI2RXD	PG1	57	42	40	28
	TSPI2TXD	PG0	56	41	39	27
	TSPI2SCK	PG2	58	43	41	29
	TSPI3RXD	PC1	34	-	-	-
	TSPI3TXD	PC0	35			
	TSPI3SCK	PC2	33			

Table 3.2 Signal connection list (2/5)

Related Reference Manual	Function pin name	Port name	M4K4 (LQFP64)	M4K2 (LQFP48)	M4K1 (LQFP44)	M4K0 (LQFP32)
32-bit Timer Event Counter	T32A00INA0	PK1	64	1	44	32
	T32A00OUTA	PK0	63	48	43	31
	T32A00INC0	PK1	64	1	44	32
	T32A00OUTC	PK0	63	48	43	31
	T32A01INA0	PA1	18	13	-	-
	T32A01INA1	PA2	20	-	-	-
	T32A01OUTA	PA2	20	-	-	-
	T32A01INB0	PA0	19	14	13	-
	T32A01OUTB	PA0	19	14	13	-
	T32A01INC0	PA1	18	13	-	-
	T32A01INC1	PA2	20	-	-	-
	T32A01OUTC	PA2	20	-	-	-
	T32A02INA0	PG1	57	42	40	28
	T32A02INA1	PG2	58	43	41	29
	T32A02OUTA	PG0	56	41	39	27
	T32A02INC0	PG1	57	42	40	28
	T32A02INC1	PG2	58	43	41	29
	T32A02OUTC	PG0	56	41	39	27
	T32A03INA0	PC1	34	-	-	-
	T32A03INA1	PC2	33	-	-	-
	T32A03OUTA	PC0	35	25	24	-
	T32A03INC0	PC1	34	-	-	-
	T32A03INC1	PC2	33	-	-	-
	T32A03OUTC	PC0	35	25	24	-
	T32A04INA0	PF1	52	-	-	-
	T32A04INA1	PF2	51	-	-	-
	T32A04OUTA	PF0	55	40	38	-
	T32A04INC0	PF1	52	-	-	-
	T32A04INC1	PF2	51	-	-	-
	T32A04OUTC	PF0	55	40	38	-
	T32A05INA0	PB1	32	24	23	-
	T32A05OUTA	PB0	31	23	22	-
	T32A05OUTB	PB1	32	24	23	-
	T32A05INC0	PB1	32	24	23	-
	T32A05OUTC	PB0	31	23	22	-

Table 3.3 Signal connection list (3/5)

Related Reference Manual	Function pin name	Port name	M4K4 (LQFP64)	M4K2 (LQFP48)	M4K1 (LQFP44)	M4K0 (LQFP32)
12-bit Analog to Digital Convertor	AINA00	PD0	37	27	26	19
	AINA01	PD1	38	28	27	20
	AINA03	PD2	39	29	28	21
	AINA04	PD3	40	30	29	-
	AINA06	PD4	41	31	30	22
	AINA07	PD5	42	32	31	-
	AINA09	PD6	43	33	32	23
	AINA10	PE0	44	34	33	-
	AINA11	PE1	45	35	34	-
	AINA12	PE2	46	36	-	-
	AINA13	PE3	47	-	-	-
	AINA14	PE4	48	-	-	-
	AINA15	PE5	49	37	35	24
Exception	INT00a	PK0	63	48	43	31
	INT00b	PF1	52	-	-	-
	INT01a	PK1	64	1	44	32
	INT01b	PF2	51	-	-	-
	INT02a	PK2	1	2	1	1
	INT02b	PB0	31	23	22	-
	INT03a	PK3	2	3	2	2
	INT03b	PB1	32	24	23	-
	INT04	PG0	56	41	39	27
	INT05	PG1	57	42	40	28
	INT06	PK4	3	4	3	-
	INT07a	PA0	19	14	13	-
	INT07b	PC2	33	-	-	-
	INT08	PC0	35	25	24	-
	INT09	PA1	18	13	-	-
	INT10	PC1	34	-	-	-

Table 3.4 Signal connection list (4/5)

Related Reference Manual	Function pin name	Port name	M4K4 (LQFP64)	M4K2 (LQFP48)	M4K1 (LQFP44)	M4K0 (LQFP32)
Advanced Programmable Motor Control Circuit	EMG0	PJ6	22	15	14	10
		PD6	43	33	32	23
		PH2	13	8	8	-
	OVV0	PJ7	21	-	-	-
	UO0	PJ0	28	21	20	16
	VO0	PJ2	26	19	18	14
	WO0	PJ4	24	17	16	12
	XO0	PJ1	27	20	19	15
	YO0	PJ3	25	18	17	13
	ZO0	PJ5	23	16	15	11
	PMD0DBG	PB0	31	23	22	-
		PG0	56	41	39	27
		PJ0	28	21	20	16
	EMG1	PF0	55	40	38	-
	UO1	PG0	56	41	39	27
	VO1	PG1	57	42	40	28
	WO1	PG2	58	43	41	29
	XO1	PG3	59	44	-	-
	YO1	PG4	60	45	-	-
	ZO1	PG5	61	46	-	-
	PMD1DBG	PB1	32	24	23	-
		PJ1	27	20	19	15
		PG1	57	42	40	28
Advanced Encoder Input Circuit	ENC0A	PG0	56	41	39	27
	ENC0B	PG1	57	42	40	28
	ENC0Z	PG2	58	43	41	29

Table 3.5 Signal connection list (5/5)

Related Reference Manual	Function pin name	Port name	M4K4 (LQFP64)	M4K2 (LQFP48)	M4K1 (LQFP44)	M4K0 (LQFP32)
Product Information (Trigger Selector)	TRGIN0	PF0	55	40	38	-
	TRGIN1	PB1	32	24	23	-
	TRGIN2	PF2	51	-	-	-
Debug Interface (JTAG/SW)	TMS	PK2	1	2	1	1
	TCK	PK3	2	3	2	2
	TDO	PK1	64	1	44	32
	TDI	PK0	63	48	43	31
	TRST_N	PK4	3	4	3	-
	SWDIO	PK2	1	2	1	1
	SWCLK	PK3	2	3	2	2
	SWV	PK1	64	1	44	32
Debug Interface (Trace)	TRACECLK	PL4	8	-	-	-
	TRACEDATA0	PL0	7			
	TRACEDATA1	PL1	6			
	TRACEDATA2	PL2	5			
	TRACEDATA3	PL3	4			
Debug Interface (NBDIF)	NBDSYNC	PK4	3	-	-	-
	NBDCLK	PL4	8			
	NBDDATA0	PL0	7			
	NBDDATA1	PL1	6			
	NBDDATA2	PL2	5			
	NBDDATA3	PL3	4			
Clock Generator and Operation Mode	X1	PH0	15	10	10	7
	EHCLKIN	PH0	15	10	10	7
	X2	PH1	16	11	11	8
	SCOUT	PJ0	28	21	20	16
FLASH Memory	BOOT_N	PJ6	22	15	14	10

4. Registers

The following registers should be set appropriately to use the ports.

Each register is 32 bits. The configuration of the register depends on the port count and its function assignment.

"x" and "n" in the following table show a port name and a function number, respectively.

Register Name		Type	Setting Value	Description
[PxDATA]	Data Register	R/W	0 or 1	Read from and write to a port.
[PxCR]	Output Control Register	R/W	0: Output disabled 1: Output enabled	Output control.
[PxFRn]	Function register n	R/W	0: PORT 1: Function	Function setting. When 1 is set, the assigned function becomes available. Each function assigned to a port has its own function register. If multiple functions are assigned to one port, only one function should be enabled.
[PxOD]	Open-drain Control Register	R/W	0: CMOS 1: Open-drain	Programmable open-drain control. The programmable open-drain is a pseudo open-drain. An output buffer is disabled when the output data is 1, which is set by ***[PxOD]*** = 1.
[PxPUP]	Pull-up Control Register	R/W	0: Pull-up disabled 1: Pull-up enabled	Programmable pull-up control.
[PxPDN]	Pull-down Control Register	R/W	0: Pull-down disabled 1: Pull-down enabled	Programmable pull-down control.
[PxIE]	Input Control Register	R/W	0: Input disabled 1: Input enabled	Input control. It takes 100ns time(Max) that an external data is reflected on ***[PxDATA]*** after the ***[PxIE]*** is enabled.

4.1. List of Register

When the bit which is assigned to no functions is read, "0" is returned. The write to the bit is ignored.

Table 4.1 Ports base address

Peripheral function		Channel/Unit	Base address
Input/output ports	PA	-	0x400C0000
	PB	-	0x400C0100
	PC	-	0x400C0200
	PD	-	0x400C0300
	PE	-	0x400C0400
	PF	-	0x400C0500
	PG	-	0x400C0600
	PH	-	0x400C0700
	PJ	-	0x400C0800
	PK	-	0x400C0900
	PL	-	0x400C0A00

Table 4.2 Register List

Register Name	Address (Base+)	Port A	Port B	Port C	Port D	Port E	Port F
Data Register	0x0000	*[PADATA]*	*[PBDATA]*	*[PCDATA]*	*[PDDATA]*	*[PEDATA]*	*[PFDATA]*
Output Control Register	0x0004	*[PACR]*	*[PBCR]*	*[PCCR]*	*[PDCR]*	*[PECR]*	*[PFCR]*
Function Register 1	0x0008	*[PAFR1]*	*[PBFR1]*	*[PCFR1]*	-	-	-
Function Register 2	0x000C	*[PAFR2]*	-	*[PCFR2]*	-	-	-
Function Register 3	0x0010	*[PAFR3]*	*[PBFR3]*	*[PCFR3]*	-	-	-
Function Register 4	0x0014	*[PAFR4]*	*[PBFR4]*	*[PCFR4]*	-	-	*[PFFR4]*
Function Register 5	0x0018	*[PAFR5]*	*[PBFR5]*	*[PCFR5]*	*[PDFR5]*	-	*[PFFR5]*
Function Register 6	0x001C	*[PAFR6]*	*[PBFR6]*	-	-	-	*[PFFR6]*
Function Register 7	0x0020	*[PAFR7]*	*[PBFR7]*	-	-	-	*[PFFR7]*
Open-Drain Control Register	0x0028	*[PAOD]*	*[PBOD]*	*[PCOD]*	*[PDOD]*	*[PEOD]*	*[PFOD]*
Pull-up Control Register	0x002C	*[PAPUP]*	*[PBPUP]*	*[PCPUP]*	*[PDPUP]*	*[PEPUP]*	*[PFPUP]*
Pull-down Control Register	0x0030	*[PAPDN]*	*[PBPDN]*	*[PCPDN]*	*[PDPDN]*	*[PEPDN]*	*[PFPDN]*
Input Control Register	0x0038	*[PAIE]*	*[PBIE]*	*[PCIE]*	*[PDIE]*	*[PEIE]*	*[PFIE]*

Register Name	Address (Base+)	Port G	Port H		Port J	Port K	Port L
			PH0/1	PH2/3			
Data Register	0x0000	*[PGDATA]*	*[PHDATA]*	*[PHDATA]*	*[PJDATA]*	*[PKDATA]*	*[PLDATA]*
Output Control Register	0x0004	*[PGCR]*	-	*[PHCR]*	*[PJCR]*	*[PKCR]*	*[PLCR]*
Function Register 1	0x0008	*[PGFR1]*	-	-	-	*[PKFR1]*	-
Function Register 2	0x000C	*[PGFR2]*	-	-	-	*[PKFR2]*	-
Function Register 3	0x0010	*[PGFR3]*	-	-	-	*[PKFR3]*	-
Function Register 4	0x0014	*[PGFR4]*	-	-	-	*[PKFR4]*	-
Function Register 5	0x0018	*[PGFR5]*	-	*[PHFR5]*	*[PJFR5]*	*[PKFR5]*	-
Function Register 6	0x001C	*[PGFR6]*	-	-	*[PJFR6]*	*[PKFR6]*	*[PLFR6]*
Function Register 7	0x0020	*[PGFR7]*	-	-	*[PJFR7]*	*[PKFR7]*	*[PLFR7]*
Open-Drain Control Register	0x0028	*[PGOD]*	-	*[PHOD]*	*[PJOD]*	*[PKOD]*	*[PLOD]*
Pull-up Control Register	0x002C	*[PGPUP]*	-	*[PHPUP]*	*[PJPUP]*	*[PKPUP]*	*[PLPUP]*
Pull-down Control Register	0x0030	*[PGPDN]*	*[PHPDN]*	*[PHPDN]*	*[PJPDN]*	*[PKPDN]*	*[PLPDN]*
Input Control Register	0x0038	*[PGIE]*	*[PHIE]*	*[PHIE]*	*[PJIE]*	*[PKIE]*	*[PLIE]*

Note: Do not access the addresses described as "-".

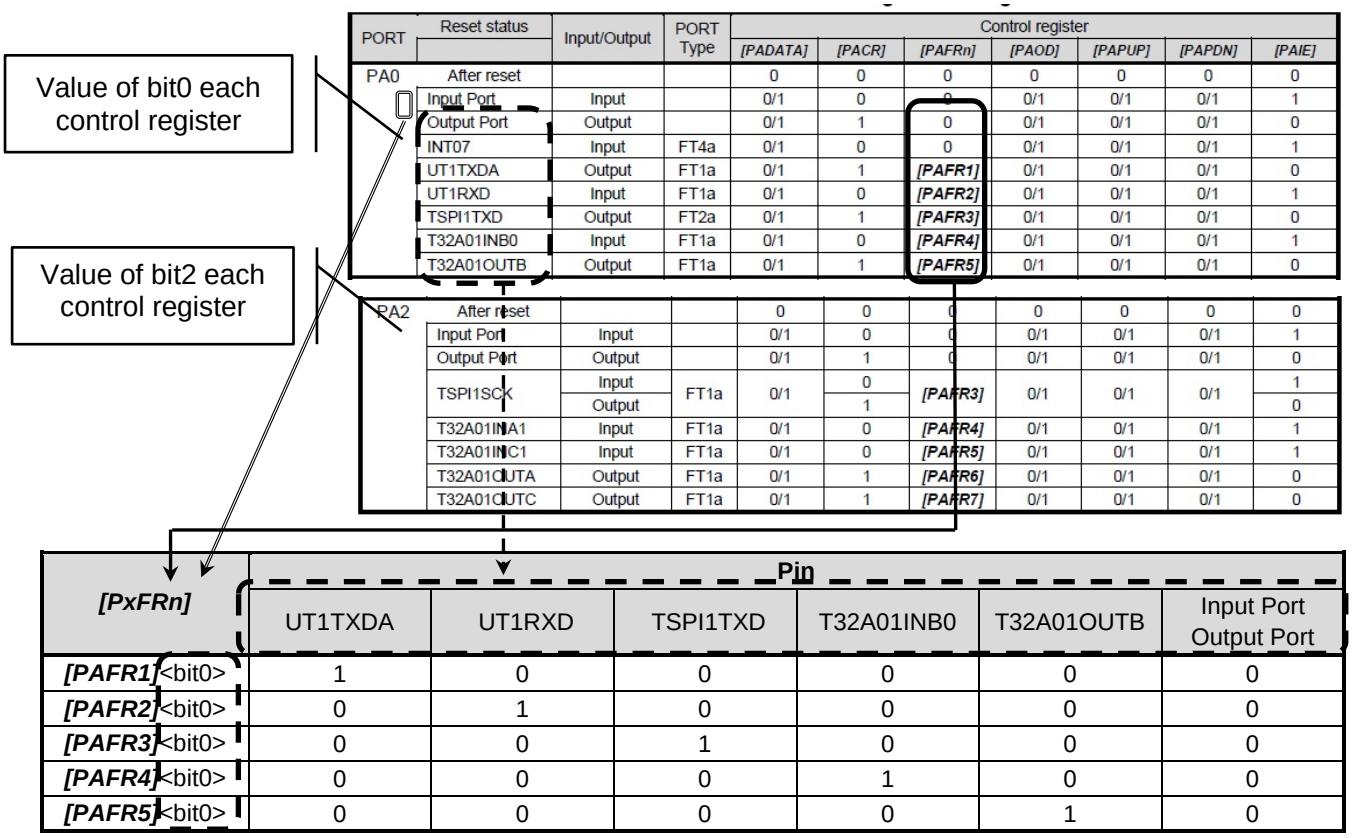
4.2. List of Port Functions and Settings

It is explained about viewpoint of a port register setting table.

The column of ***[PxFRn]*** shows the function register which should be set. When this register is set to "1", the corresponding function is enabled. (x is a port name and n is a function number.)

The bit in the "N/A" in the tables returns "0" when it is read. The write to the bit is ignored.

"0" or "1" in the tables shows the value which should be set. "0/1" means either value can be set.



PORT	Reset status	Input/Output	PORT Type	Control register						
				[PADATA]	[PACR]	[PAFRn]	[PAOD]	[PAPUP]	[PAPDN]	[PAIE]
PA0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT07	Input	FT4a	0/1	0	0	0/1	0/1	0/1	1
	UT1TXDA	Output	FT1a	0/1	1	[PAFR1]	0/1	0/1	0/1	0
	UT1RXD	Input	FT1a	0/1	0	[PAFR2]	0/1	0/1	0/1	1
	TSPI1TXD	Output	FT2a	0/1	1	[PAFR3]	0/1	0/1	0/1	0
	T32A01INB0	Input	FT1a	0/1	0	[PAFR4]	0/1	0/1	0/1	1
	T32A01OUTB	Output	FT1a	0/1	1	[PAFR5]	0/1	0/1	0/1	0
PA2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI1SCK	Input	FT1a	0/1	0	[PAFR3]	0/1	0/1	0/1	1
		Output			1					0
	T32A01INA1	Input	FT1a	0/1	0	[PAFR4]	0/1	0/1	0/1	1
	T32A01INC1	Input	FT1a	0/1	0	[PAFR5]	0/1	0/1	0/1	1
	T32A01OUTA	Output	FT1a	0/1	1	[PAFR6]	0/1	0/1	0/1	0
	T32A01OUTC	Output	FT1a	0/1	1	[PAFR7]	0/1	0/1	0/1	0

[PxFRn]	Pin					
	UT1TXDA	UT1RXD	TSPI1TXD	T32A01INB0	T32A01OUTB	Input Port Output Port
[PAFR1]<bit0>	1	0	0	0	0	0
[PAFR2]<bit0>	0	1	0	0	0	0
[PAFR3]<bit0>	0	0	1	0	0	0
[PAFR4]<bit0>	0	0	0	1	0	0
[PAFR5]<bit0>	0	0	0	0	1	0

4.2.1. Setting of using the function pin

To use the alternated pins as peripheral function output pins, set the peripheral function (***[PxFRn]***<bit m>=1) that uses the function register and then enable output control register (***[PxCR]***<bit m>=1). If output is enabled before setting the function register, the data register value of the port is output until the function register is set.

To use the alternated pins as input pins of the peripheral function, set the input control register of the port (***[PxIE]***<bit m>=1) and set the peripheral function that uses the function register (***[PxFRn]***<bit m>=1), then set the peripheral functions.

To use peripheral functions such as I^2C, set the input control register of the port (***[PxIE]***<bit m>=1), set the peripheral function (***[PxFRn]***<bit m>=1) and set the output control register to output enable (***[PxCR]***<bit m>=1), then set the peripheral function.

- When plural functions are assigned to the same pin, please use a function pin exclusively.
- When the same function is assigned to plural ports, please use a pin exclusively.

4.2.2. PORT A

Table 4.3 Port A register setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PADATA]	***[PACR]***	***[PAFRn]***	***[PAOD]***	***[PAPUP]***	***[PAPDN]***	***[PAIE]***
PA0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT07	Input	FT4a	0/1	0	0	0/1	0/1	0/1	1
	UT1TXDA	Output	FT1a	0/1	1	***[PAFR1]***	0/1	0/1	0/1	0
	UT1RXD	Input	FT1a	0/1	0	***[PAFR2]***	0/1	0/1	0/1	1
	TSPI1TXD	Output	FT2a	0/1	1	***[PAFR3]***	0/1	0/1	0/1	0
	T32A01INB0	Input	FT1a	0/1	0	***[PAFR4]***	0/1	0/1	0/1	1
	T32A01OUTB	Output	FT1a	0/1	1	***[PAFR5]***	0/1	0/1	0/1	0
PA1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT09	Input	FT4a	0/1	0	0	0/1	0/1	0/1	1
	UT1RXD	Input	FT1a	0/1	0	***[PAFR1]***	0/1	0/1	0/1	1
	UT1TXDA	Output	FT1a	0/1	1	***[PAFR2]***	0/1	0/1	0/1	0
	TSPI1RXD	Input	FT1a	0/1	0	***[PAFR3]***	0/1	0/1	0/1	1
	T32A01INA0	Input	FT1a	0/1	0	***[PAFR4]***	0/1	0/1	0/1	1
	T32A01INC0	Input	FT1a	0/1	0	***[PAFR5]***	0/1	0/1	0/1	1
PA2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI1SCK	Input	FT1a	0/1	0	***[PAFR3]***	0/1	0/1	0/1	1
		Output			1					0
	T32A01INA1	Input	FT1a	0/1	0	***[PAFR4]***	0/1	0/1	0/1	1
	T32A01INC1	Input	FT1a	0/1	0	***[PAFR5]***	0/1	0/1	0/1	1
	T32A01OUTA	Output	FT1a	0/1	1	***[PAFR6]***	0/1	0/1	0/1	0
	T32A01OUTC	Output	FT1a	0/1	1	***[PAFR7]***	0/1	0/1	0/1	0

4.2.3. PORT B

Table 4.4 Port B register setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PBDATA]	***[PBCR]***	***[PBFRn]***	***[PBOD]***	***[PBPUP]***	***[PBPDN]***	***[PBIE]***
PB0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT02	Input	FT4a	0/1	0	0	0/1	0/1	0/1	1
	I2C0SDA	I/O	FT1a	0/1	1	***[PBFR3]***	1	0/1	0	1
	T32A05OUTA	Output	FT1a	0/1	1	***[PBFR4]***	0/1	0/1	0/1	0
	T32A05OUTC	Output	FT1a	0/1	1	***[PBFR5]***	0/1	0/1	0/1	0
	PMD0DBG	Output	FT1a	0/1	1	***[PBFR7]***	0/1	0/1	0/1	0
PB1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT03	Input	FT4a	0/1	0	0	0/1	0/1	0/1	1
	T32A05OUTB	Output	FT1a	0/1	1	***[PBFR1]***	0/1	0/1	0/1	0
	I2C0SCL	I/O	FT1a	0/1	1	***[PBFR3]***	1	0/1	0	1
	T32A05INA0	Input	FT1a	0/1	0	***[PBFR4]***	0/1	0/1	0/1	1
	T32A05INC0	Input	FT1a	0/1	0	***[PBFR5]***	0/1	0/1	0/1	1
	TRGIN1	Input	FT1a	0/1	0	***[PBFR6]***	0/1	0/1	0/1	1
	PMD1DBG	Output	FT1a	0/1	1	***[PBFR7]***	0/1	0/1	0/1	0

4.2.4. PORT C

Table 4.5 Port C register setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PCDATA]	*[PCCR]*	*[PCFRn]*	*[PCOD]*	*[PCPUP]*	*[PCPDN]*	*[PCIE]*
PC0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT08	Input	FT4a	0/1	0	0	0/1	0/1	0/1	1
	UT3TXDA	Output	FT1a	0/1	1	***[PCFR1]***	0/1	0/1	0/1	0
	UT3RXD	Input	FT1a	0/1	0	***[PCFR2]***	0/1	0/1	0/1	1
	TSPI3TXD	Output	FT2a	0/1	1	***[PCFR3]***	0/1	0/1	0/1	0
	T32A03OUTA	Output	FT1a	0/1	1	***[PCFR4]***	0/1	0/1	0/1	0
	T32A03OUTC	Output	FT1a	0/1	1	***[PCFR5]***	0/1	0/1	0/1	0
PC1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT10	Input	FT4a	0/1	0	0	0/1	0/1	0/1	1
	UT3RXD	Input	FT1a	0/1	0	***[PCFR1]***	0/1	0/1	0/1	1
	UT3TXDA	Output	FT1a	0/1	1	***[PCFR2]***	0/1	0/1	0/1	0
	TSPI3RXD	Input	FT1a	0/1	0	***[PCFR3]***	0/1	0/1	0/1	1
	T32A03INA0	Input	FT1a	0/1	0	***[PCFR4]***	0/1	0/1	0/1	1
	T32A03INC0	Input	FT1a	0/1	0	***[PCFR5]***	0/1	0/1	0/1	1
PC2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT07	Input	FT4a	0/1	0	0	0/1	0/1	0/1	1
	TSPI3SCK	Input	FT1a	0/1	0	***[PCFR3]***	0/1	0/1	0/1	1
		Output			1					0
	T32A03INA1	Input	FT1a	0/1	0	***[PCFR4]***	0/1	0/1	0/1	1
	T32A03INC1	Input	FT1a	0/1	0	***[PCFR5]***	0/1	0/1	0/1	1

4.2.5. PORT D

Table 4.6 Port D register setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PDDATA]	***[PDCR]***	***[PDFRn]***	***[PDOD]***	***[PDPUP]***	***[PDPDN]***	***[PDIE]***
PD0	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA00(Note)	Input	FT5a	0/1	0	N/A	0/1	0	0	0
PD1	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA01(Note)	Input	FT5a	0/1	0	N/A	0/1	0	0	0
PD2	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA03(Note)	Input	FT5a	0/1	0	N/A	0/1	0	0	0
PD3	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA04(Note)	Input	FT5a	0/1	0	N/A	0/1	0	0	0
PD4	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA06(Note)	Input	FT5a	0/1	0	N/A	0/1	0	0	0
PD5	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA07(Note)	Input	FT5a	0/1	0	N/A	0/1	0	0	0
PD6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	AINA09(Note)	Input	FT5a	0/1	0	0	0/1	0	0	0
	EMG0	Input	FT1a	0/1	0	***[PDFR5]***	0/1	0/1	0/1	1

Note: When using analog input(AINAx), ***[PDIE]*** should be input disable"0", ***[PDCR]*** should be input disable"0", ***[PDPUP]*** should be pull-up disable"0", and ***[PDPDN]*** should be pull-up disable"0".

4.2.6. PORT E

Table 4.7 Port E register setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PEDATA]	*[PECR]*	*[PEFRn]*	*[PEOD]*	*[PEPUP]*	*[PEPDN]*	*[PEIE]*
PE0	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA10(Note)	Input	FT5a	0/1	0	N/A	0/1	0	0	0
PE1	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA11(Note)	Input	FT5a	0/1	0	N/A	0/1	0	0	0
PE2	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA12(Note)	Input	FT5a	0/1	0	N/A	0/1	0	0	0
PE3	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA13(Note)	Input	FT5a	0/1	0	N/A	0/1	0	0	0
PE4	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA14(Note)	Input	FT5a	0/1	0	N/A	0/1	0	0	0
PE5	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA15(Note)	Input	FT5a	0/1	0	N/A	0/1	0	0	0
	VREFH(Note)	Input	FT5a	0/1	0	N/A	0/1	0	0	0

Note: When using analog input(AINAx) or the analog reference input(VREFH), ***[PEIE]*** should be input disable"0", ***[PECR]*** should be input disable"0", ***[PEPUP]*** should be pull-up disable"0", and ***[PEPDN]*** should be pull-up disable"0".

4.2.7. PORT F

Table 4.8 Port F register setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PFDATA]	***[PFCR]***	***[PFFRn]***	***[PFOD]***	***[PFPUP]***	***[PFPDN]***	***[PFIE]***
PF0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A04OUTA	Output	FT1a	0/1	1	***[PFFR4]***	0/1	0/1	0/1	0
	T32A04OUTC	Output	FT1a	0/1	1	***[PFFR5]***	0/1	0/1	0/1	0
	TRGIN0	Input	FT1a	0/1	0	***[PFFR6]***	0/1	0/1	0/1	1
	EMG1	Input	FT1a	0/1	0	***[PFFR7]***	0/1	0/1	0/1	1
PF1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT00	Input	FT4a	0/1	0	0	0/1	0/1	0/1	1
	T32A04INA0	Input	FT1a	0/1	0	***[PFFR4]***	0/1	0/1	0/1	1
	T32A04INC0	Input	FT1a	0/1	0	***[PFFR5]***	0/1	0/1	0/1	1
PF2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT01	Input	FT4a	0/1	0	0	0/1	0/1	0/1	1
	T32A04INA1	Input	FT1a	0/1	0	***[PFFR4]***	0/1	0/1	0/1	1
	T32A04INC1	Input	FT1a	0/1	0	***[PFFR5]***	0/1	0/1	0/1	1
	TRGIN2	Input	FT1a	0/1	0	***[PFFR6]***	0/1	0/1	0/1	1

4.2.8. PORT G

Table 4.9 Port G register setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PGDATA]	*[PGCR]*	*[PGFRn]*	*[PGOD]*	*[PGPUP]*	*[PGPDN]*	*[PGIE]*
PG0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT04	Input	FT4a	0/1	0	0	0/1	0/1	0/1	1
	UT2TXDA	Output	FT1a	0/1	1	***[PGFR1]***	0/1	0/1	0/1	0
	TSPI2TXD	Output	FT2a	0/1	1	***[PGFR2]***	0/1	0/1	0/1	0
	T32A02OUTA	Output	FT1a	0/1	1	***[PGFR3]***	0/1	0/1	0/1	0
	T32A02OUTC	Output	FT1a	0/1	1	***[PGFR4]***	0/1	0/1	0/1	0
	ENC0A	Input	FT1a	0/1	0	***[PGFR5]***	0/1	0/1	0/1	1
	UO1	Output	FT2a	0/1	1	***[PGFR6]***	0/1	0/1	0/1	0
	PMG0DBG	Output	FT1a	0/1	1	***[PGFR7]***	0/1	0/1	0/1	0
PG1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT05	Input	FT4a	0/1	0	0	0/1	0/1	0/1	1
	UT2RXD	Input	FT1a	0/1	0	***[PGFR1]***	0/1	0/1	0/1	1
	TSPI2RXD	Input	FT1a	0/1	0	***[PGFR2]***	0/1	0/1	0/1	1
	T32A02INA0	Input	FT1a	0/1	0	***[PGFR3]***	0/1	0/1	0/1	1
	T32A02INC0	Input	FT1a	0/1	0	***[PGFR4]***	0/1	0/1	0/1	1
	ENC0B	Input	FT1a	0/1	0	***[PGFR5]***	0/1	0/1	0/1	1
	VO1	Output	FT2a	0/1	1	***[PGFR6]***	0/1	0/1	0/1	0
	PMD1DBG	Output	FT1a	0/1	1	***[PGFR7]***	0/1	0/1	0/1	0
PG2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI2SCK	Input	FT1a	0/1	0	***[PGFR2]***	0/1	0/1	0/1	1
		Output			1					0
	T32A02INA1	Input	FT1a	0/1	0	***[PGFR3]***	0/1	0/1	0/1	1
	T32A02INC1	Input	FT1a	0/1	0	***[PGFR4]***	0/1	0/1	0/1	1
	ENC0Z	Input	FT1a	0/1	0	***[PGFR5]***	0/1	0/1	0/1	1
	WO1	Output	FT2a	0/1	1	***[PGFR6]***	0/1	0/1	0/1	0
PG3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	XO1	Output	FT2a	0/1	1	***[PGFR6]***	0/1	0/1	0/1	0
PG4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	YO1	Output	FT2a	0/1	1	***[PGFR6]***	0/1	0/1	0/1	0
PG5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	ZO1	Output	FT2a	0/1	1	***[PGFR6]***	0/1	0/1	0/1	0

4.2.9. PORT H

Table 4.10 Port H register setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PHDATA]	***[PHCR]***	***[PHFRn]***	***[PHOD]***	***[PHPUP]***	***[PHPDN]***	***[PHIE]***
PH0	After reset			0	N/A	N/A	N/A	N/A	0	0
	Input Port	Input		0/1	N/A	N/A	N/A	N/A	0/1	1
	X1	Input	FT11a	0/1	N/A	N/A	N/A	N/A	0	0
	EHCLKIN	Input	FT11a	0/1	N/A	N/A	N/A	N/A	0	1
PH1	After reset			0	N/A	N/A	N/A	N/A	0	0
	Input Port	Input		0/1	N/A	N/A	N/A	N/A	0/1	1
	X2	Output	FT11a	0/1	N/A	N/A	N/A	N/A	0	0
PH2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	EMG0	Input	FT1a	0/1	0	***[PHFR5]***	0/1	0/1	0/1	1
PH3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0

4.2.10. PORT J

Table 4.11 Port J register setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PJDATA]	***[PJCR]***	***[PJFRn]***	***[PJOD]***	***[PJPUP]***	***[PJPDN]***	***[PJIE]***
PJ0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UO0	Output	FT2a	0/1	1	***[PJFR5]***	0/1	0/1	0/1	0
	SCOUT	Output	FT1a	0/1	1	***[PJFR6]***	0/1	0/1	0/1	0
	PMD0DBG	Output	FT1a	0/1	1	***[PJFR7]***	0/1	0/1	0/1	0
PJ1	After reset			0	0	0	0	0		0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	XO0	Output	FT2a	0/1	1	***[PJFR5]***	0/1	0/1	0/1	0
	PMD1DBG	Output	FT1a	0/1	1	***[PJFR7]***	0/1	0/1	0/1	0
PJ2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	VO0	Output	FT2a	0/1	1	***[PJFR5]***	0/1	0/1	0/1	0
PJ3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	YO0	Output	FT2a	0/1	1	***[PJFR5]***	0/1	0/1	0/1	0
PJ4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	WO0	Output	FT2a	0/1	1	***[PJFR5]***	0/1	0/1	0/1	0
PJ5	After reset	Input		0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	ZO0	Output	FT2a	0/1	1	***[PJFR5]***	0/1	0/1	0/1	0
PJ6	During reset (BOOT_N)	Input	FT16a	0	0	0	0	0(Note)	0	0(Note)
	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	EMG0	Input	FT1a	0/1	0	***[PJFR5]***	0/1	0/1	0/1	1
PJ7	After reset	Input		0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	OVV0	Input	FT1a	0/1	0	***[PJFR5]***	0/1	0/1	0/1	1

Note: PJ6 can input the BOOT_N signal while ***[PJPUP]*** is enabled ("1") and ***[PJIE]*** is also enabled ("1") during the reset period by the reset pin (RESET_N).

4.2.11. PORT K

Table 4.12 Port K register setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PKDATA]	*[PKCR]*	*[PKFRn]*	*[PKOD]*	*[PKPUP]*	*[PKPDN]*	*[PKIE]*
PK0	After reset (TDI)	Input	FT2a	0	0	***[PKFR7]***	0	1	0	1
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT00	Input	FT4a	0/1	0	0	0/1	0/1	0/1	1
	UT0RXD	Input	FT1a	0/1	0	***[PKFR1]***	0/1	0/1	0/1	1
	UT0TXDA	Output	FT1a	0/1	1	***[PKFR2]***	0/1	0/1	0/1	0
	T32A00OUTA	Output	FT1a	0/1	1	***[PKFR4]***	0/1	0/1	0/1	0
	T32A00OUTC	Output	FT1a	0/1	1	***[PKFR5]***	0/1	0/1	0/1	0
PK1	After reset (TDO/SWV)	Output	FT2a	0	1(Note)	***[PKFR7]***	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT01	Input	FT4a	0/1	0	0	0/1	0/1	0/1	1
	UT0TXDA	Output	FT1a	0/1	1	***[PKFR1]***	0/1	0/1	0/1	0
	UT0RXD	Input	FT1a	0/1	0	***[PKFR2]***	0/1	0/1	0/1	1
	T32A00INA0	Input	FT1a	0/1	0	***[PKFR4]***	0/1	0/1	0/1	1
	T32A00INC0	Input	FT1a	0/1	0	***[PKFR5]***	0/1	0/1	0/1	1
PK2	After reset (TMS/SWDIO)	Input/Output	FT2a	0	1(Note)	***[PKFR7]***	0	1	0	1
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT02	Input	FT4a	0/1	0	0	0/1	0/1	0/1	1
	UT0RXD	Input	FT1a	0/1	0	***[PKFR1]***	0/1	0/1	0/1	1
	UT0TXDA	Output	FT1a	0/1	1	***[PKFR2]***	0/1	0/1	0/1	0
	TSPI0RXD	Input	FT1a	0/1	0	***[PKFR3]***	0/1	0/1	0/1	1
PK3	After reset (TCK/SWCLK)	Input	FT2a	0	0	***[PKFR7]***	0	0	1	1
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT03	Input	FT4a	0/1	0	0	0/1	0/1	0/1	1
	UT0TXDA	Output	FT1a	0/1	1	***[PKFR1]***	0/1	0/1	0/1	0
	UT0RXD	Input	FT1a	0/1	0	***[PKFR2]***	0/1	0/1	0/1	1
	TSPI0TXD	Output	FT2a	0/1	1	***[PKFR3]***	0/1	0/1	0/1	0
PK4	After reset (TRST_N)	Input	FT3a	0	0	***[PKFR7]***	0	1	0	1
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT06	Input	FT4a	0/1	0	0	0/1	0/1	0/1	1
	TSPI0SCK	Input	FT1a	0/1	0	***[PKFR3]***	0/1	0/1	0/1	1
		Output			1					0
	NBDSYNC	Input	FT3a	0/1	0	***[PKFR6]***	0/1	0/1	0/1	1

Note: When receive the command from TOOL, it becomes output.

4.2.12. PORT L

Table 4.13 Port L register setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PLDATA]	*[PLCR]*	*[PLFRn]*	*[PLOD]*	*[PLPUP]*	*[PLPDN]*	*[PLIE]*
PL0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	NBDDATA0	Input/Output	FT2c	0/1	1	***[PLFR6]***	0/1	0/1	0	1
	TRACEDATA0	Output	FT1a	0/1	1	***[PLFR7]***	0/1	0/1	0/1	0
PL1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	NBDDATA1	Input/Output	FT2c	0/1	1	***[PLFR6]***	0/1	0/1	0	1
	TRACEDATA1	Output	FT1a	0/1	1	***[PLFR7]***	0/1	0/1	0/1	0
PL2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	NBDDATA2	Input/Output	FT2c	0/1	1	***[PLFR6]***	0/1	0/1	0	1
	TRACEDATA2	Output	FT1a	0/1	1	***[PLFR7]***	0/1	0/1	0/1	0
PL3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	NBDDATA3	Input/Output	FT2c	0/1	1	***[PLFR6]***	0/1	0/1	0	1
	TRACEDATA3	Output	FT1a	0/1	1	***[PLFR7]***	0/1	0/1	0/1	0
PL4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	NBDCLK	Input	FT3a	0/1	0	***[PLFR6]***	0/1	0/1	0/1	1
	TRACECLK	Output	FT1a	0/1	1	***[PLFR7]***	0/1	0/1	0/1	0

5. Port Circuit Diagram

The port has 8 types of circuits, FT1a to FT5a, FT11a and FT16a. Each circuit diagram is shown in the following page and after. The dot line block shows "Equivalent Circuit" which is described in "Datasheet".

The "I/O Reset" shown in the circuit diagram is described the power on reset(POR) or the reset pin(RESET_N). Although, “I/O Reset” of debug pins(TMS/SWDIO.TDI,TDO/SWV,TCK/SWCLK,TRST_N) is the power on reset(POR) only.

5.1. Type FT1a

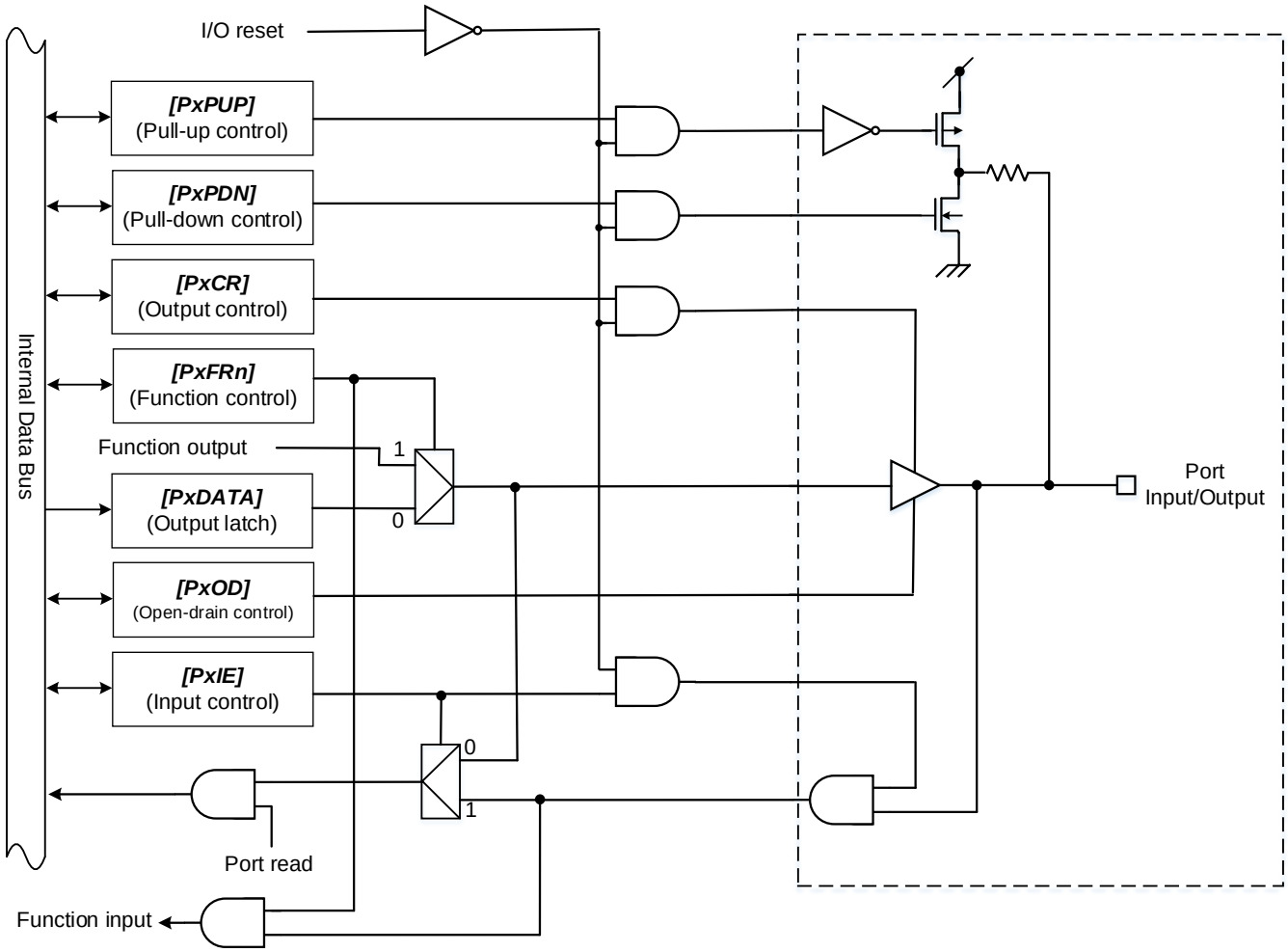


Figure 5.1 Port Type FT1a

5.2. Type FT2a

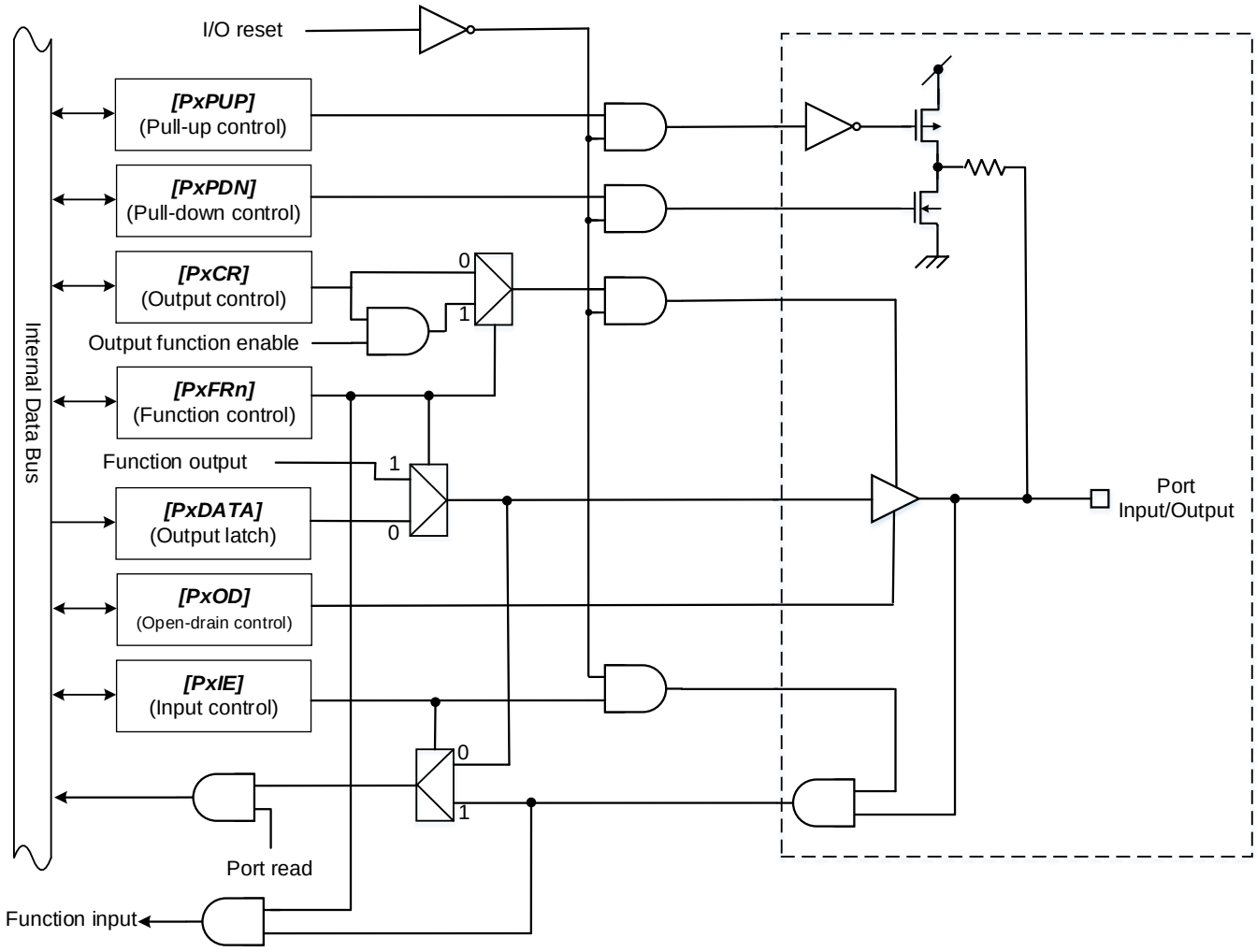


Figure 5.2 Port Type FT2a

5.3. Type FT2c

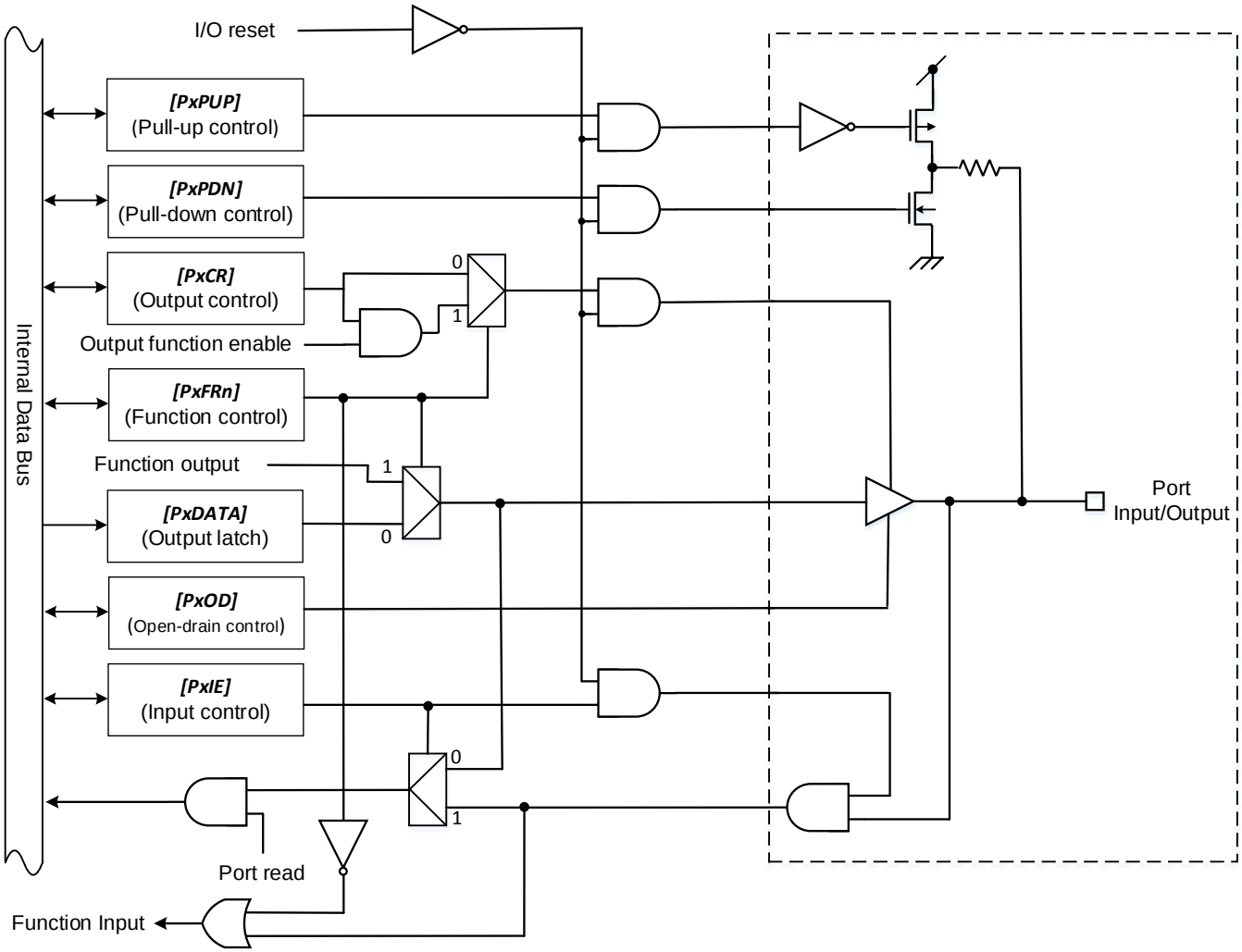


Figure 5.3 Port Type FT2c

5.4. Type FT3a

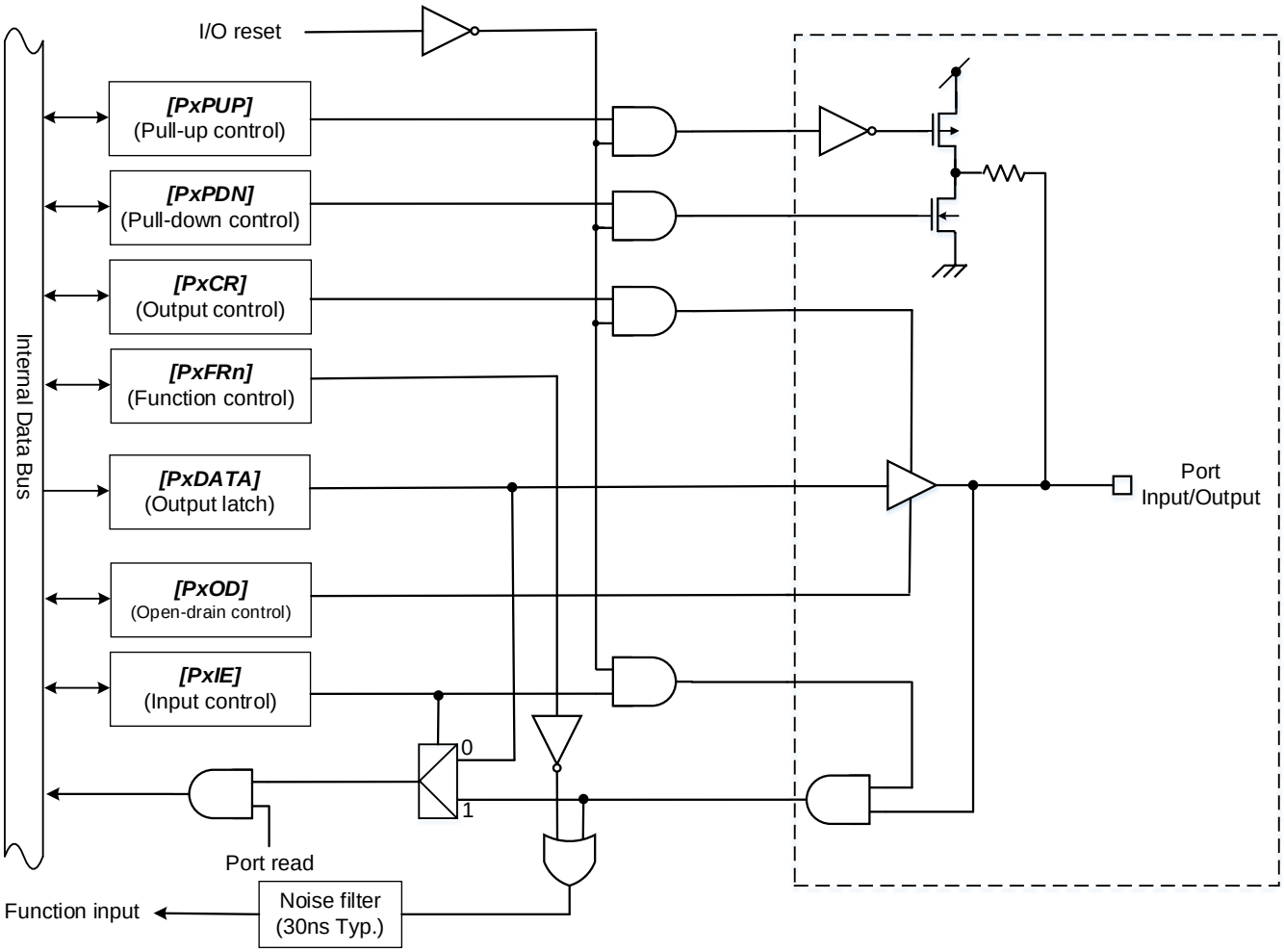


Figure 5.4 Port Type FT3a

5.5. Type FT4a

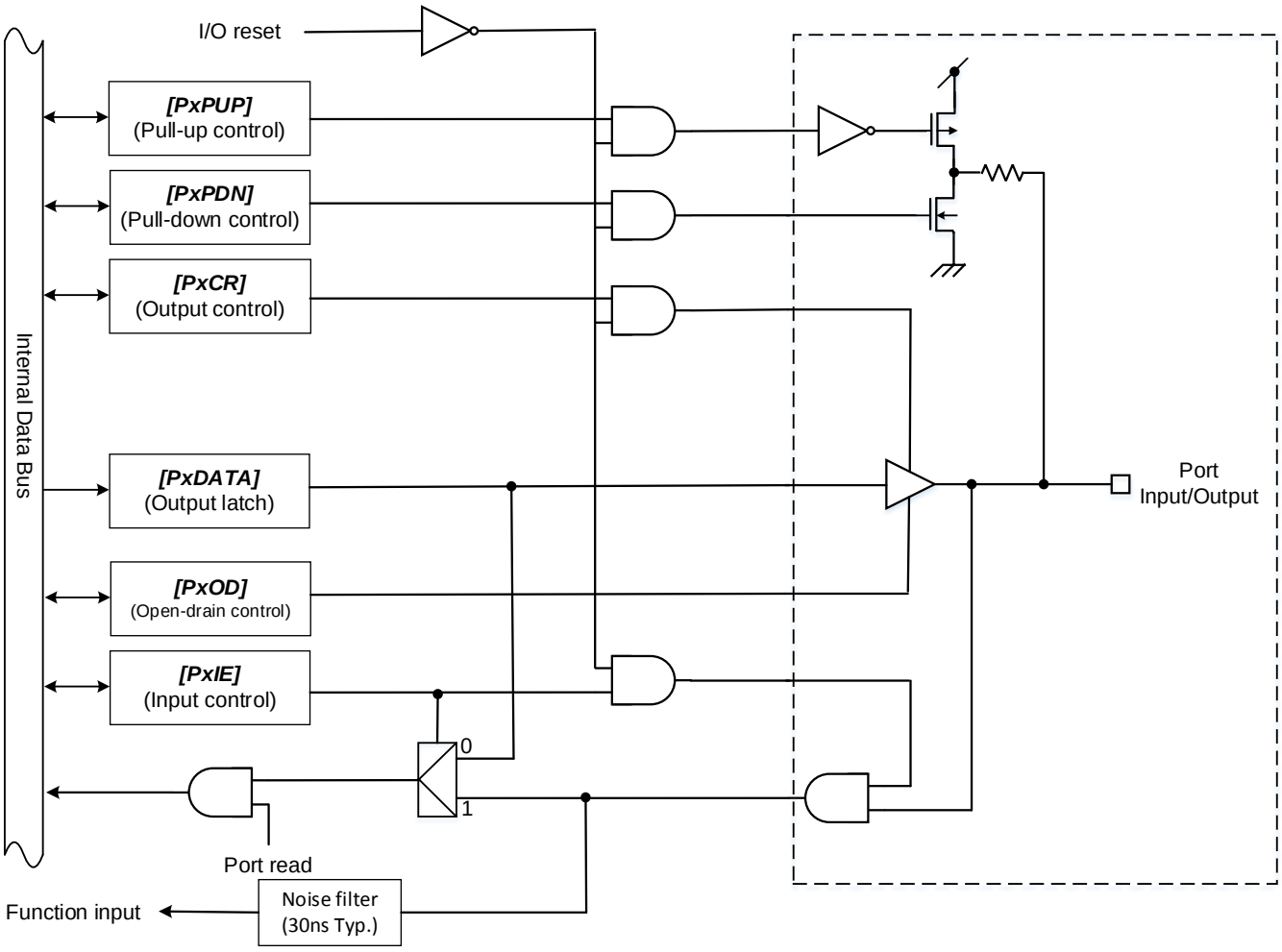


Figure 5.5 Port Type FT4a

5.6. Type FT5a

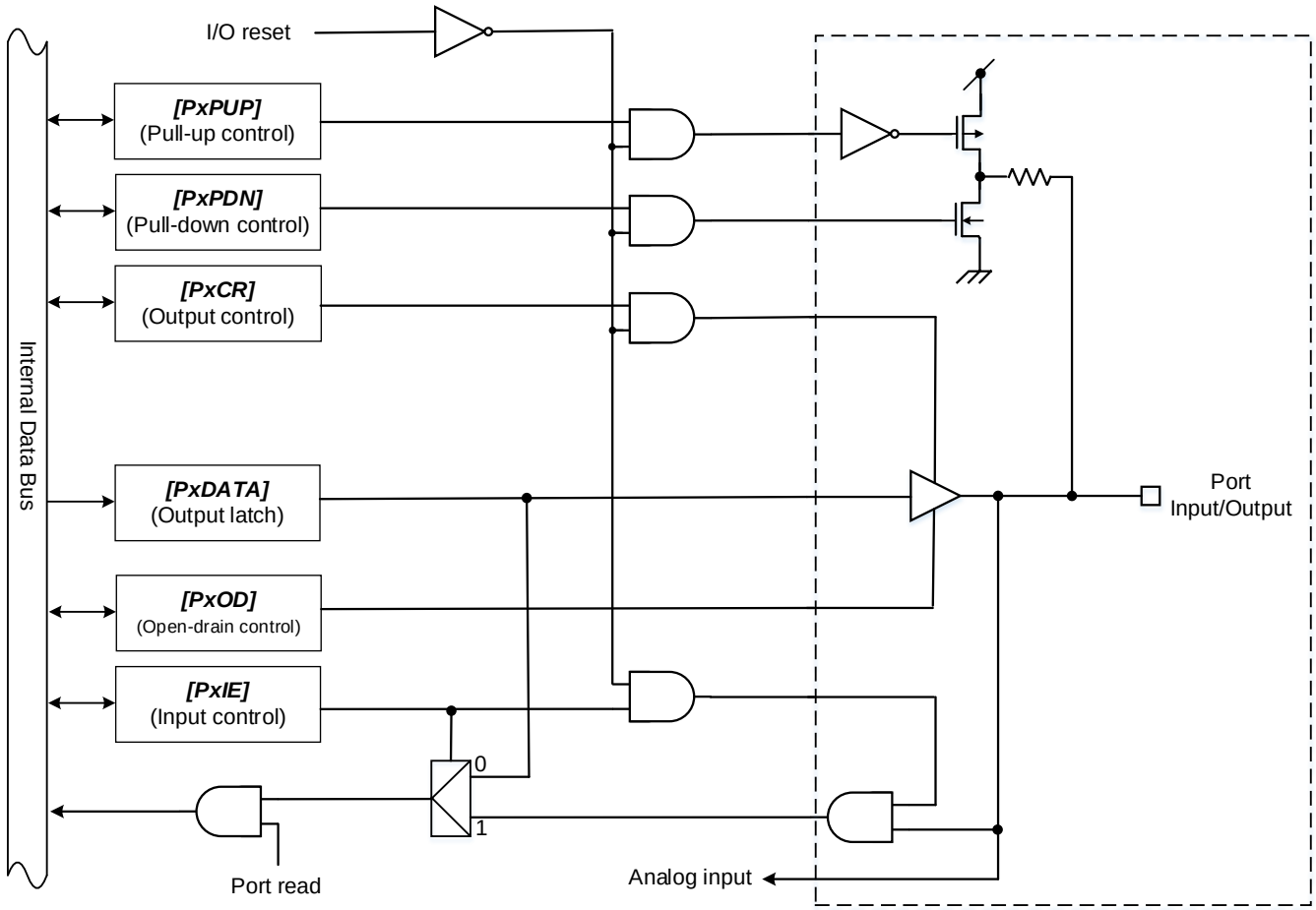


Figure 5.6 Port Type FT5a

5.7. Type FT11a

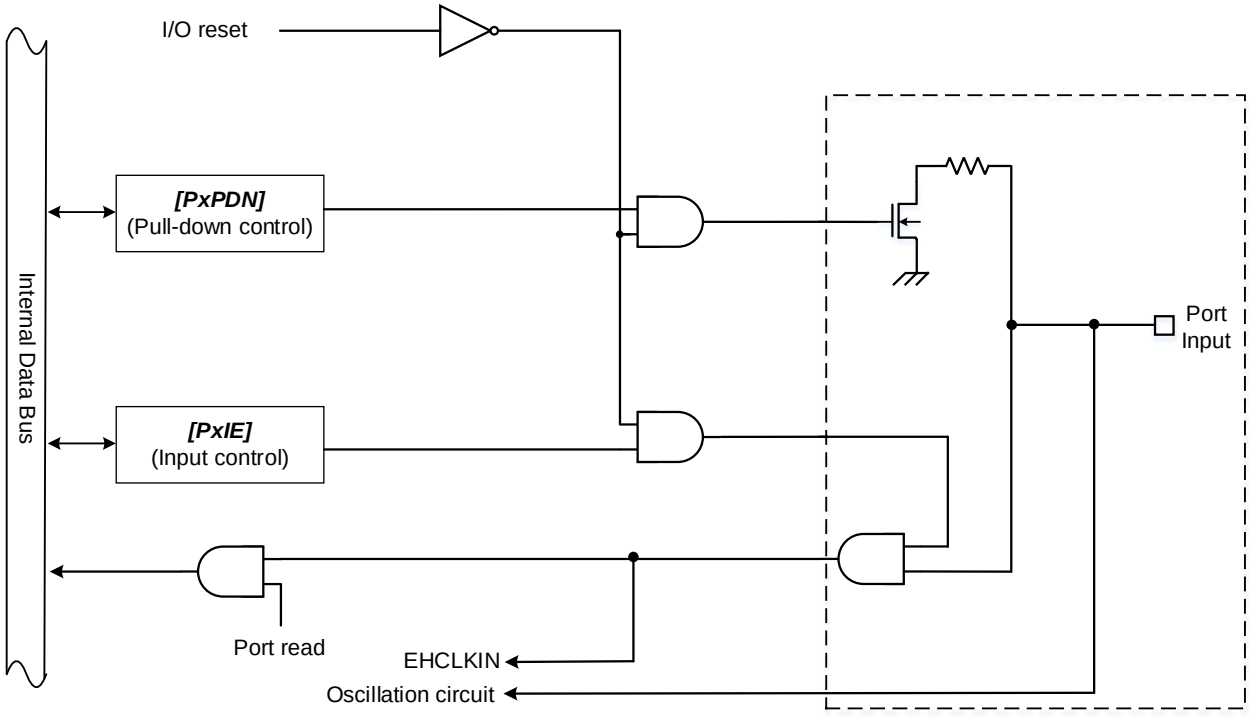


Figure 5.7 Port Type FT11a

5.8. Type FT16a

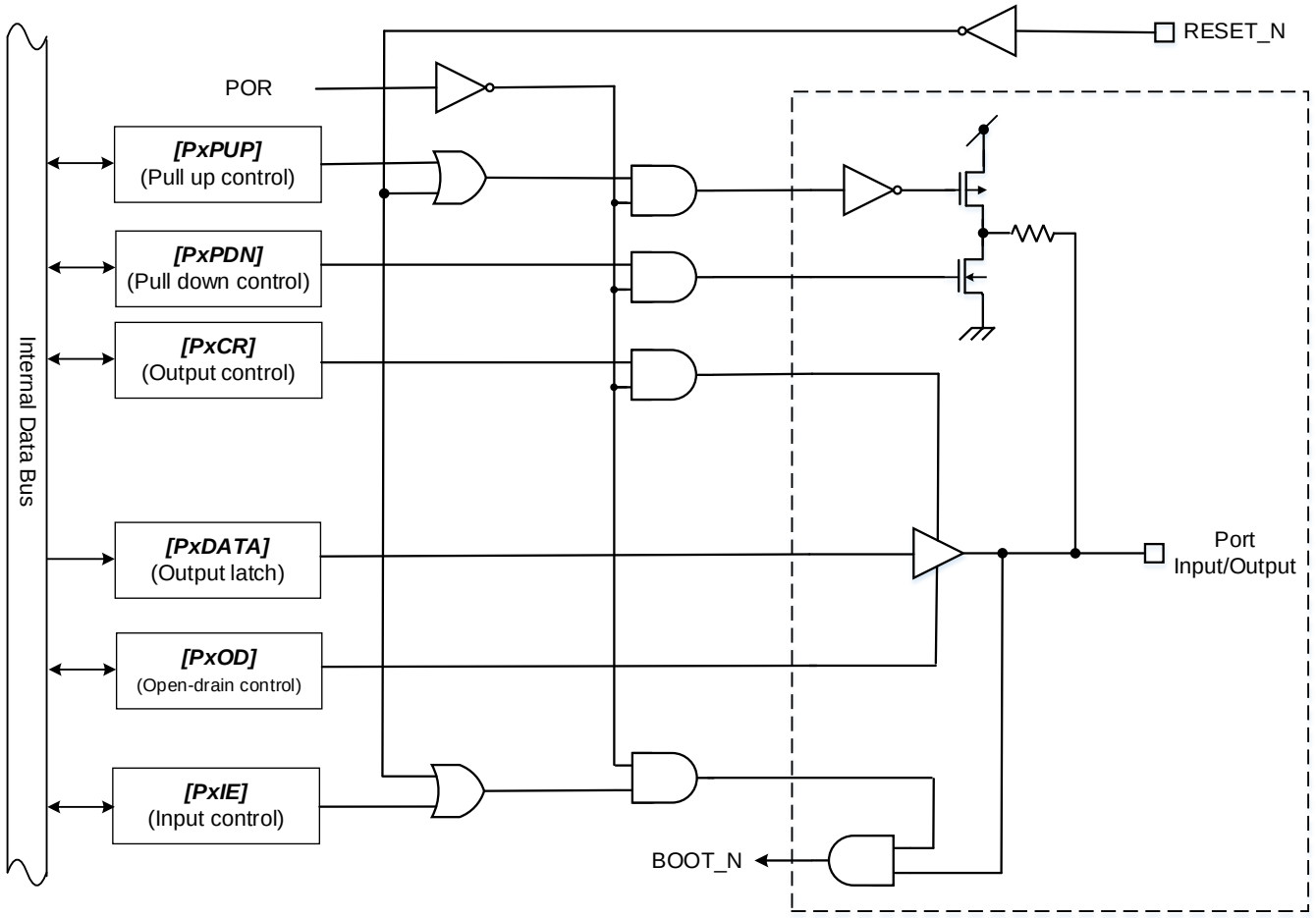


Figure 5.8 Port Type FT16a

6. Precaution

6.1. pin status during a reset period

During the reset period, the pin status is high impedance except for below pins. And, the pull-up/pull-down is invalid.

- The debug interface alternate pins(PK0 to PK4) are debug pin status.
- PJ6(BOOT_N) works as a BOOT function. It is enabled to be input and pulled-up during pin reset period. At the rising edge of the reset signal, if PJ6 is "High", the device enters single chip mode and boots from the on chip flash memory. If PJ6 is "Low", the device enters single BOOT mode and boots from the internal BOOT program.

6.2. Unused pins

We recommend that each unused pin should be connected to the power supply pins or GND pins via resistors.

Generally, if MCUs operate while the high-impedance pins left open, electrostatic damage or latch-up may occur in the internal LSI due to induced voltage influenced from external noise.

6.3. Important points of using debug interface pins used as general-purpose ports

After releasing reset, If the debug interface pins are used as the general I/O ports by the user program, the debug tool cannot be connected

If the debug tool cannot be connected, it can recover debug connection to erase the flash memory using UART connection set as single BOOT mode from external. For details, please refer "Flash memory" of reference manual.

7. Revision History

Table 7.1 Revision History

Revision	Date	Description
1.0	2017-11-14	First release
2.0	2018-04-26	Terms and Abbreviations changed NBD to NBDIF 2. revised Clock supply section 4.2.10 Port type of PJ6 revised Note revised 5. Port type FT6a deleted, Port type FT16a added. 5.3 Type 2c added 5.7 Type 12a revised 5.8 Type 16a added
2.1	2019-06-13	3. Single connection list Added EHCLKIN in Table3.5 4.2.1 Revised FxFR to FxFRn 4.2.3 PORT B Corrected I2SC0DA/I2C0SCL: FT12a to FT1a 4.2.5 PORD D Modified Note “When using analog input” to “When using analog input(AINAx)” 4.2.6 PORD E Modified Note “When using analog input” to “When using analog input(AINAx)” 4.2.11 PORT K Added initial PORT Corrected NBDSYNC: FT1a to FT2a 4.2.12 PORT L Corrected NBDDATAn: FT1a to FT2c Corrected NBDCLK: FT1a to FT3a 5. Port Circuit Diagram Added description 5.3 Type FT2c Added Figure 5.3 FT2c deleted Type FT12a 6.1 pin status during a reset period Corrected 2nd paragraph : “during reset period” to “during pin reset period”

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