32-bit RISC Microcontroller

TMPM4K Group(1)

Reference Manual

Product Information (PINFO-M4K(1))

Revision 2.1

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TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> =0x01 (hexadecimal), ***[XYZn]***<VW> =1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value.
  In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-ENC	Advanced Encoder input Circuit
A-PMD	Advanced Programmable Motor Control Circuit
A-VE+	Advanced Vector Engine plus
CRC	Cyclic Redundancy Check
DMAC	Direct Memory Access Controller
DNF	Digital Noise Filter
EHOSC	External High Speed Oscillator
IHOSC	Internal High Speed Oscillator
INT	Interrupt
I2C	Inter-Integrated Circuit
LVD	Voltage Detection Circuit
NBDIF	Non Break Debug Interface
OFD	Oscillation Frequency Detector
OPAMP	Operational Amplifier
RAMP	RAM parity
SIWDT	Clock Selective Watchdog Timer
TRGSEL	Trigger Selection circuit
TRM	Trimming circuit
TSPI	Toshiba Serial Peripheral Interface
T32A	32-bit Timer Event Counter
UART	Universal Asynchronous Receiver Transmitter

1. Overview

This chapter describes peripheral function-related channels or number of units, information of pins and product-specific function information. Use this chapter in conjunction with Reference Manual for Peripheral Function.

2. Information of Peripheral Function

2.1. Register Base address

The following table shows the type of base address of each peripheral.

Table 2.1 Type of Register base address

Product	Type of Base Address
TMPM4K Group(1)	TYPE1

To develop each peripheral function, please refer to the above type of base address.
In case of no information of Type1/2 of the base address in the Reference manual, it use as Type1.

2.2. Trigger Selector(TRGSEL)

The trigger selector is the circuit which chooses the one trigger and outputs the trigger signal to the peripheral function from two or more triggers inputted from the peripheral function, the port, etc.

The trigger chosen from eight triggers by ***[TSEL0CRn]***<INSELm> is outputted to the peripheral function of a connection destination.

"Figure 2.1 Example of Trigger Selector Connection" is an example of connection DMA transmission end interrupts to DMAC via trigger selector. The setup of input trigger selection, edge detection condition selection, trigger output selection, and trigger output control is performed by ***[TSEL0CR3]***.

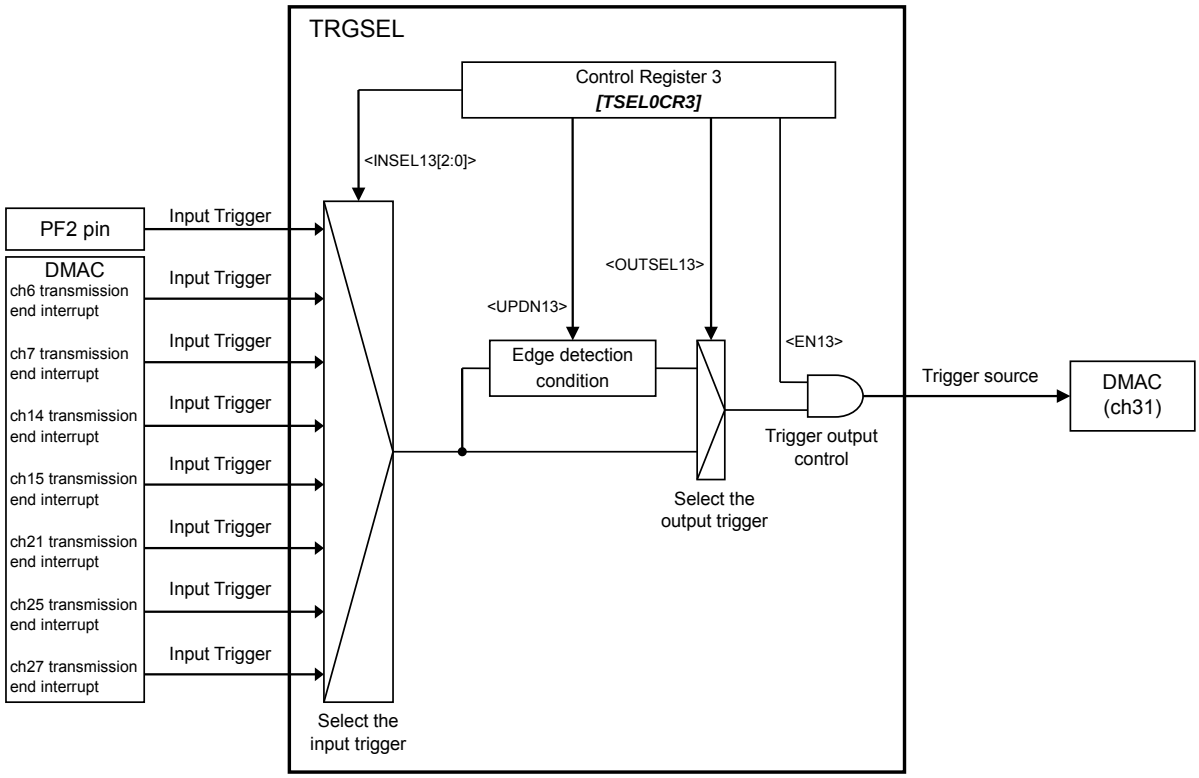

Figure 2.1 Example of Trigger Selector Connection

2.2.1. Trigger Selector List for the each Products

Trigger selector of TMPM4K Group(1) consist of 11 control registers(***[TSEL0CR0 to 10]***), and 41 triggers are controlled.

The following table shows "Trigger Selector List of each Product".

Table 2.2 Trigger Selector List for each Product (1/5)

Register	Bit Symbol	Trigger source	Trigger Source	Product (✓:Available, -:N/A)			
				M4K4	M4K2	M4K1	M4K0
[TSEL0CR0]	INSEL0	DMA ch18	ADC general purpose trigger DMA request ADC single conversion DMA request ADC continuous conversion DMA request	✓	✓	✓	✓
	INSEL1	DMA ch19	T32A ch0 DMA request at match A1 register T32A ch0 DMA request at match C1 register T32A ch1 DMA request at match A1 register T32A ch1 DMA request at match C1 register A-PMD ch0 PWM interrupt	✓	✓	✓	✓
	INSEL2	DMA ch20	T32A ch2 DMA request at match A1 register T32A ch2 DMA request at match C1 register T32A ch3 DMA request at match A1 register T32A ch3 DMA request at match C1 register A-PMD ch1 PWM interrupt	✓	✓	✓	✓
	INSEL3	DMA ch21	T32A ch4 DMA request at match A1 register T32A ch4 DMA request at match C1 register T32A ch5 DMA request at match A1 register T32A ch5 DMA request at match C1 register	✓	✓	✓	✓
[TSEL0CR1]	INSEL4	DMA ch22	T32A ch0 DMA request at match B1 register T32A ch1 DMA request at match B1 register T32A ch2 DMA request at match B1 register T32A ch3 DMA request at match B1 register T32A ch4 DMA request at match B1 register T32A ch5 DMA request at match B1 register	✓	✓	✓	✓
	INSEL5	DMA ch23	T32A ch0 DMA request at capture A0 register T32A ch0 DMA request at capture A1 register T32A ch1 DMA request at capture A0 register T32A ch1 DMA request at capture A1 register T32A ch0 DMA request at capture C0 register T32A ch0 DMA request at capture C1 register T32A ch1 DMA request at capture C0 register T32A ch1 DMA request at capture C1 register	✓	✓	✓	✓
	INSEL6	DMA ch24	T32A ch2 DMA request at capture A0 register T32A ch2 DMA request at capture A1 register T32A ch3 DMA request at capture A0 register T32A ch3 DMA request at capture A1 register T32A ch2 DMA request at capture C0 register T32A ch2 DMA request at capture C1 register T32A ch3 DMA request at capture C0 register T32A ch3 DMA request at capture C1 register	✓	✓	✓	✓
	INSEL7	DMA ch25	T32A ch4 DMA request at capture A0 register T32A ch4 DMA request at capture A1 register T32A ch5 DMA request at capture A0 register T32A ch5 DMA request at capture A1 register T32A ch4 DMA request at capture C0 register T32A ch4 DMA request at capture C1 register T32A ch5 DMA request at capture C0 register T32A ch5 DMA request at capture C1 register	✓	✓	✓	✓

Table 2.3 Trigger Selector List for each Product (2/5)

Register	Bit Symbol	Trigger source	Trigger Source	Product (✓:Available, -:N/A)			
				M4K4	M4K2	M4K1	M4K0
[TSEL0CR2]	INSEL8	DMA ch26	T32A ch0 DMA request at capture B0 register T32A ch0 DMA request at capture B1 register T32A ch1 DMA request at capture B0 register T32A ch1 DMA request at capture B1 register T32A ch2 DMA request at capture B0 register T32A ch2 DMA request at capture B1 register	✓	✓	✓	✓
	INSEL9	DMA ch27	T32A ch3 DMA request at capture B0 register T32A ch3 DMA request at capture B1 register T32A ch4 DMA request at capture B0 register T32A ch4 DMA request at capture B1 register T32A ch5 DMA request at capture B0 register T32A ch5 DMA request at capture B1 register	✓	✓	✓	✓
	INSEL10	DMA ch28	DMAC ch0 transfer completion DMAC ch1 transfer completion DMAC ch8 transfer completion DMAC ch9 transfer completion DMAC ch16 transfer completion DMAC ch17 transfer completion DMAC ch22 transfer completion	✓	✓	✓	✓
	INSEL11	DMA ch29	DMAC ch2 transfer completion DMAC ch3 transfer completion DMAC ch10 transfer completion DMAC ch11 transfer completion DMAC ch18 transfer completion DMAC ch19 transfer completion DMAC ch23 transfer completion	✓	✓	✓	✓
			PF0 (TRGIN0)	✓	✓	✓	-
[TSEL0CR3]	INSEL12	DMA ch30	DMAC ch4 transfer completion DMAC ch5 transfer completion DMAC ch12 transfer completion DMAC ch13 transfer completion DMAC ch20 transfer completion DMAC ch24 transfer completion DMAC ch26 transfer completion	✓	✓	✓	✓
			PB1 (TRGIN1)	✓	✓	✓	-
	INSEL13	DMA ch31	DMAC ch6 transfer completion DMAC ch7 transfer completion DMAC ch14 transfer completion DMAC ch15 transfer completion DMAC ch21 transfer completion DMAC ch25 transfer completion DMAC ch27 transfer completion	✓	✓	✓	✓
			PF2 (TRGIN2)	✓	-	-	-
	INSEL14	ADC	PF0 (TRGIN0)	✓	✓	✓	-
			PB1 (TRGIN1)	✓	✓	✓	-
			PF2 (TRGIN2)	✓	-	-	-
			T32A ch5 Timer register A1 match trigger T32A ch5 Timer register B1 match trigger T32A ch5 Timer register C1 match trigger	✓	✓	✓	✓
	INSEL15	TSPI ch0	PF0 (TRGIN0)	✓	✓	✓	-
			PB1 (TRGIN1)	✓	✓	✓	-
			PF2 (TRGIN2)	✓	-	-	-
			T32A ch5 Timer register A1 match trigger T32A ch5 Timer register B1 match trigger T32A ch5 Timer register C1 match trigger	✓	✓	✓	✓

Table 2.4 Trigger Selector List for each Product (3/5)

Register	Bit Symbol	Trigger source	Trigger Source	Product (✓:Available, -:N/A)			
				M4K4	M4K2	M4K1	M4K0
[TSEL0CR4]	INSEL16	TSPI ch1	PF0 (TRGIN0)	✓	-	-	-
			PB1 (TRGIN1)	✓	-	-	-
			PF2 (TRGIN2)	✓	-	-	-
			T32A ch5 Timer register A1 match trigger T32A ch5 Timer register B1 match trigger T32A ch5 Timer register C1 match trigger	✓	-	-	-
	INSEL17	TSPI ch2	PF0 (TRGIN0)	✓	✓	✓	-
			PB1 (TRGIN1)	✓	✓	✓	-
			PF2 (TRGIN2)	✓	-	-	-
			T32A ch5 Timer register A1 match trigger T32A ch5 Timer register B1 match trigger T32A ch5 Timer register C1 match trigger	✓	✓	✓	✓
	INSEL18	TSPI ch3	PF0 (TRGIN0)	✓	-	-	-
			PB1 (TRGIN1)	✓	-	-	-
			PF2 (TRGIN2)	✓	-	-	-
			T32A ch5 Timer register A1 match trigger T32A ch5 Timer register B1 match trigger T32A ch5 Timer register C1 match trigger	✓	-	-	-
	INSEL19	UART ch0	PF0 (TRGIN0)	✓	✓	✓	-
			PB1 (TRGIN1)	✓	✓	✓	-
			PF2 (TRGIN2)	✓	-	-	-
			T32A ch5 Timer register A1 match trigger T32A ch5 Timer register B1 match trigger T32A ch5 Timer register C1 match trigger	✓	✓	✓	✓
[TSEL0CR5]	INSEL20	UART ch1	PF0 (TRGIN0)	✓	✓	-	-
			PB1 (TRGIN1)	✓	✓	-	-
			PF2 (TRGIN2)	✓	-	-	-
			T32A ch5 Timer register A1 match trigger T32A ch5 Timer register B1 match trigger T32A ch5 Timer register C1 match trigger	✓	✓	-	-
	INSEL21	UART ch2	PF0 (TRGIN0)	✓	✓	✓	-
			PB1 (TRGIN1)	✓	✓	✓	-
			PF2 (TRGIN2)	✓	-	-	-
			T32A ch5 Timer register A1 match trigger T32A ch5 Timer register B1 match trigger T32A ch5 Timer register C1 match trigger	✓	✓	✓	✓
	INSEL22	UART ch3	PF0 (TRGIN0)	✓	-	-	-
			PB1 (TRGIN1)	✓	-	-	-
			PF2 (TRGIN2)	✓	-	-	-
			T32A ch5 Timer register A1 match trigger T32A ch5 Timer register B1 match trigger T32A ch5 Timer register C1 match trigger	✓	-	-	-
	INSEL23	T32A ch0 Timer A	PF0 (TRGIN0)	✓	✓	✓	-
			PB1 (TRGIN1)	✓	✓	✓	-
			PF2 (TRGIN2)	✓	-	-	-
			UART ch0 transmission completion trigger UART ch0 reception completion trigger TSPI ch0 transmit completion TSPI ch0 receive completion	✓	✓	✓	✓

Table 2.5 Trigger Selector List for each Product (4/5)

Register	Bit Symbol	Trigger source	Trigger Source	Product (✓:Available, -:N/A)			
				M4K4	M4K2	M4K1	M4K0
[TSEL0CR6]	INSEL24	T32A ch0 Timer B	T32A ch0 Timer register A0 match trigger T32A ch0 Timer register A1 match trigger T32A ch0 Timer A overflow trigger T32A ch0 Timer A underflow trigger	✓	✓	✓	✓
	INSEL25	T32A ch0 Timer C	T32A ch5 Timer register C0 match trigger T32A ch5 Timer register C1 match trigger T32A ch5 Timer C overflow trigger T32A ch5 Timer C underflow trigger	✓	✓	✓	✓
	INSEL26	T32A ch1 Timer A	PF0 (TRGIN0)	✓	✓	✓	-
			PB1 (TRGIN1)	✓	✓	✓	-
			PF2 (TRGIN2)	✓	-	-	-
			UART ch1 transmission completion trigger UART ch1 reception completion trigger TSPI ch1 transmit completion TSPI ch1 receive completion	✓	✓	-	-
	INSEL27	T32A ch1 Timer B	T32A ch1 Timer register A0 match trigger T32A ch1 Timer register A1 match trigger T32A ch1 Timer A overflow trigger T32A ch1 Timer A underflow trigger	✓	✓	✓	✓
[TSEL0CR7]	INSEL28	T32A ch1 Timer C	T32A ch0 Timer register C0 match trigger T32A ch0 Timer register C1 match trigger T32A ch0 Timer C overflow trigger T32A ch0 Timer C underflow trigger	✓	✓	✓	✓
	INSEL29	T32A ch2 Timer A	PF0 (TRGIN0)	✓	✓	✓	-
			PB1 (TRGIN1)	✓	✓	✓	-
			PF2 (TRGIN2)	✓	-	-	-
			UART ch2 transmission completion trigger UART ch2 reception completion trigger TSPI ch2 transmit completion TSPI ch2 receive completion	✓	✓	✓	✓
	INSEL30	T32A ch2 Timer B	T32A ch2 Timer register A0 match trigger T32A ch2 Timer register A1 match trigger T32A ch2 Timer A overflow trigger T32A ch2 Timer A underflow trigger	✓	✓	✓	✓
	INSEL31	T32A ch2 Timer C	T32A ch1 Timer register C0 match trigger T32A ch1 Timer register C1 match trigger T32A ch1 Timer C overflow trigger T32A ch1 Timer C underflow trigger	✓	✓	✓	✓

Table 2.6 Trigger Selector List for each Product (5/5)

Register	Bit Symbol	Trigger source	Trigger Source	Product (✓:Available, -:N/A)			
				M4K4	M4K2	M4K1	M4K0
[TSEL0CR8]	INSEL32	T32A ch3 Timer A	PF0 (TRGIN0)	✓	✓	✓	-
			PB1 (TRGIN1)	✓	✓	✓	-
			PF2 (TRGIN2)	✓	-	-	-
			UART ch3 transmission completion trigger UART ch3 reception completion trigger TSPI ch3 transmit completion TSPI ch3 receive completion	✓	-	-	-
			I^2C ch0 I^2C interrupt	✓	✓	✓	-
	INSEL33	T32A ch3 Timer B	T32A ch3 Timer register A0 match trigger T32A ch3 Timer register A1 match trigger T32A ch3 Timer A overflow trigger T32A ch3 Timer A underflow trigger	✓	✓	✓	✓
	INSEL34	T32A ch3 Timer C	T32A ch2 Timer register C0 match trigger T32A ch2 Timer register C1 match trigger T32A ch2 Timer C overflow trigger T32A ch2 Timer C underflow trigger	✓	✓	✓	✓
	INSEL35	T32A ch4 Timer A	PF0 (TRGIN0)	✓	✓	✓	-
			PB1 (TRGIN1)	✓	✓	✓	-
			PF2 (TRGIN2)	✓	-	-	-
			A-ENC ch0 divided pulse signal	✓	✓	✓	✓
[TSEL0CR9]	INSEL36	T32A ch4 Timer B	T32A ch4 Timer register A0 match trigger T32A ch4 Timer register A1 match trigger T32A ch4 Timer A overflow trigger T32A ch4 Timer A underflow trigger	✓	✓	✓	✓
	INSEL37	T32A ch4 Timer C	T32A ch3 Timer register C0 match trigger T32A ch3 Timer register C1 match trigger T32A ch3 Timer C overflow trigger T32A ch3 Timer C underflow trigger	✓	✓	✓	✓
	INSEL38	T32A ch5 Timer A	PF0 (TRGIN0)	✓	✓	✓	-
			PB1 (TRGIN1)	✓	✓	✓	-
			PF2 (TRGIN2)	✓	-	-	-
			ADC general purpose trigger interrupt ADC single conversion interrupt ADC continuous conversion interrupt ADC monitor function 0 Interrupt ADC monitor function 1 Interrupt	✓	✓	✓	✓
	INSEL39	T32A ch5 Timer B	T32A ch5 Timer register A0 match trigger T32A ch5 Timer register A1 match trigger T32A ch5 Timer A overflow trigger T32A ch5 Timer A underflow trigger	✓	✓	✓	✓
[TSEL0CR10]	INSEL40	T32A ch5 Timer C	T32A ch4 Timer register C0 match trigger T32A ch4 Timer register C1 match trigger T32A ch4 Timer C overflow trigger T32A ch4 Timer C underflow trigger	✓	✓	✓	✓

2.2.2. Operation and setting

When using TRGSEL, please set an applicable clock enable bit to "1" (clock supply) in fsys supply stop register A (***[CGFSYSENA]***, ***[CGFSYSMENA]***), fsys supply stop register B (***[CGFSYSENB]***, ***[CGFSYSMENB]***), and fc supply stop registers (***[CGFCEN]***).

An applicable register and the bit position vary according to a product. Therefore, the register may not exist with the product. Please refer to "Clock Control and Operation Mode" of the reference manual for the details.

Setting procedure of Trigger selector is as following.

(1) Selection of an input trigger (***[TSEL0CRn]*** <INSELm>)

Selection of the input trigger used for the trigger source is performed.

Please set up selection of the input trigger by the input trigger subdevice bit (***[TSEL0CRn]*** <INSELm>) of the control register. (n: register number, m: trigger number)

(2) Selection of edge detection conditions (***[TSEL0CRn]*** <UPDNm>)

For the input trigger signal which needs edge detection, selection of rising edge or falling edge detection is performed.

Please set up selection of edge detection conditions in the selection bit (***[TSEL0CRn]***<UPDNm>) of a control register.

The following shows the trigger signal which needs edge detection.

- External trigger input (TRGIN0, TRGIN1, and TRGIN2)

(3) Selection of a trigger output (***[TSEL0CRn]***<OUTSELm>)

Selection of an output without or with edge detection is performed.

Please set up selection of a trigger output in the selection bit (***[TSEL0CRn]***<OUTSELm>) of a control register.

(4) Output enable (***[TSEL0CRn]***<ENm>)

The output (enable/disable) of the selected trigger signal is chosen.

Please set up selection of output (enable/disable) in the setting bit (***[TSEL0CRn]***<ENm>) of a control register. A trigger output will be enabled if ***[TSEL0CRn]***<ENm> is set as "1".

2.2.3. List of Registers

The table below shows control registers and their addresses.

Peripheral function		Channel/Unit	Base address
Trigger selector	TRGSEL	ch0	0x400BB800

Register name		Address(Base+)
Control Register 0	***[TSELxCR0]***	0x0000
Control Register 1	***[TSELxCR1]***	0x0004
Control Register 2	***[TSELxCR2]***	0x0008
Control Register 3	***[TSELxCR3]***	0x000C
Control Register 4	***[TSELxCR4]***	0x0010
Control Register 5	***[TSELxCR5]***	0x0014
Control Register 6	***[TSELxCR6]***	0x0018
Control Register 7	***[TSELxCR7]***	0x001C
Control Register 8	***[TSELxCR8]***	0x0020
Control Register 9	***[TSELxCR9]***	0x0024
Control Register 10	***[TSELxCR10]***	0x0028

2.2.4. Details of Registers

The following chapters show the detail of registers. The sign in the functional column parenthesis of each table expresses each function signal name.

2.2.4.1. *[TSELxCR0]* (Control Register 0)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as 0
30:28	INSEL3[2:0]	000	R/W	Select the input trigger (DMA ch21) 000: T32A ch4 DMA request at match A1 register (T32A04DMAREQCMPA1) 001: T32A ch4 DMA request at match C1 register(T32A04DMAREQCMPC1) 010: T32A ch5 DMA request at match A1 register(T32A05DMAREQCMPA1) 011: T32A ch5 DMA request at match C1 register(T32A05DMAREQCMPC1) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as 0
26	UPDN3	0	R/W	Edge detection 0: Rising edge detection 1: falling edge detection
25	OUTSEL3	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN3	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as 0
22:20	INSEL2[2:0]	000	R/W	Select the input trigger (DMA ch20) 000: T32A ch2 DMA request at match A1 register(T32A02DMAREQCMPA1) 001: T32A ch2 DMA request at match C1 register(T32A02DMAREQCMPC1) 010: T32A ch3 DMA request at match A1 register(T32A03DMAREQCMPA1) 011: T32A ch3 DMA request at match C1 register(T32A03DMAREQCMPC1) 100: A-PMD ch1 PWM interrupt (INTPWM1) 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as 0
18	UPDN2	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL2	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN2	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as 0

Bit	Bit Symbol	After Reset	Type	Function
14:12	INSEL1[2:0]	000	R/W	Select the input trigger (DMA ch19) 000: T32A ch0 DMA request at match A1 register (T32A00DMAREQCMPA1) 001: T32A ch0 DMA request at match C1 register (T32A00DMAREQCMPC1) 010: T32A ch1 DMA request at match A1 register (T32A01DMAREQCMPA1) 011: T32A ch1 DMA request at match C1 register (T32A01DMAREQCMPC1) 100: A-PMD ch0 PWM interrupt (INTPWM0) 101: Reserved 110: Reserved 111: Reserved
11	-	0	R	Read as 0
10	UPDN1	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
9	OUTSEL1	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN1	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as 0
6:4	INSEL0[2:0]	000	R/W	Select the input trigger (DMA ch18) 000: ADC general purpose trigger DMA request (ADATRG_DMAREQ) 001: ADC single conversion DMA request (ADASGL_DMAREQ) 010: ADC continuous conversion DMA request (ADACNT_DMAREQ) 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as 0
2	UPDN0	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL0	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN0	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.4.2. *[TSELxCR1]* (Control Register1)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as 0
30:28	INSEL7[2:0]	000	R/W	Select the input trigger (DMA ch25) 000: T32A ch4 DMA request capture A0(T32A04DMAREQCAPA0) 001: T32A ch4 DMA request capture A1(T32A04DMAREQCAPA1) 010: T32A ch5 DMA request capture A0(T32A05DMAREQCAPA0) 011: T32A ch5 DMA request capture A1(T32A05DMAREQCAPA1) 100: T32A ch4 DMA request capture C0(T32A04DMAREQCAPC0) 101: T32A ch4 DMA request capture C1(T32A04DMAREQCAPC1) 110: T32A ch5 DMA request capture C0(T32A05DMAREQCAPC0) 111: T32A ch5 DMA request capture C1(T32A05DMAREQCAPC1)
27	-	0	R	Read as 0
26	UPDN7	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL7	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN7	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as 0
22:20	INSEL6[2:0]	000	R/W	Select the input trigger (DMA ch24) 000: T32A ch2 DMA request capture A0(T32A02DMAREQCAPA0) 001: T32A ch2 DMA request capture A1(T32A02DMAREQCAPA1) 010: T32A ch3 DMA request capture A0(T32A03DMAREQCAPA0) 011: T32A ch3 DMA request capture A1(T32A03DMAREQCAPA1) 100: T32A ch2 DMA request capture C0(T32A02DMAREQCAPC0) 101: T32A ch2 DMA request capture C1(T32A02DMAREQCAPC1) 110: T32A ch3 DMA request capture C0(T32A03DMAREQCAPC0) 111: T32A ch3 DMA request capture C1(T32A03DMAREQCAPC1)
19	-	0	R	Read as 0
18	UPDN6	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL6	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN6	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as 0
14:12	INSEL5[2:0]	000	R/W	Select the input trigger (DMA ch23) 000: T32A ch0 DMA request capture A0(T32A00DMAREQCAPA0) 001: T32A ch0 DMA request capture A1(T32A00DMAREQCAPA1) 010: T32A ch1 DMA request capture A0(T32A01DMAREQCAPA0) 011: T32A ch1 DMA request capture A1(T32A01DMAREQCAPA1) 100: T32A ch0 DMA request capture C0(T32A00DMAREQCAPC0) 101: T32A ch0 DMA request capture C1(T32A00DMAREQCAPC1) 110: T32A ch1 DMA request capture C0(T32A01DMAREQCAPC0) 111: T32A ch1 DMA request capture C1(T32A01DMAREQCAPC1)
11	-	0	R	Read as 0
10	UPDN5	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection

Bit	Bit Symbol	After Reset	Type	Function
9	OUTSEL5	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN5	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as 0
6:4	INSEL4[2:0]	000	R/W	Select the input trigger (DMA ch22) 000: T32A ch0 DMA request at match B1 register (T32A00DMAREQCMPB1) 001: T32A ch1 DMA request at match B1 register (T32A01DMAREQCMPB1) 010: T32A ch2 DMA request at match B1 register (T32A02DMAREQCMPB1) 011: T32A ch3 DMA request at match B1 register (T32A03DMAREQCMPB1) 100: T32A ch4 DMA request at match B1 register (T32A04DMAREQCMPB1) 101: T32A ch5 DMA request at match B1 register (T32A05DMAREQCMPB1) 110: Reserved 111: Reserved
3	-	0	R	Read as 0
2	UPDN4	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL4	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN4	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.4.3. *[TSELxCR2]* (Control Register 2)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as 0
30:28	INSEL11[2:0]	000	R/W	Select the input trigger (DMA ch29) 000: DMAC ch2 transfer completion(INTDMAATC2) 001: DMAC ch3 transfer completion(INTDMAATC3) 010: DMAC ch10 transfer completion(INTDMAATC10) 011: DMAC ch11 transfer completion(INTDMAATC11) 100: DMAC ch18 transfer completion(INTDMAATC18) 101: DMAC ch19 transfer completion(INTDMAATC19) 110: DMAC ch23 transfer completion(INTDMAATC23) 111: PF0 (TRGIN0)
27	-	0	R	Read as 0
26	UPDN11	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL11	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN11	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as 0
22:20	INSEL10[2:0]	000	R/W	Select the input trigger (DMA ch28) 000: DMAC ch0 transfer completion(INTDMAATC0) 001: DMAC ch1 transfer completion(INTDMAATC1) 010: DMAC ch8 transfer completion(INTDMAATC8) 011: DMAC ch9 transfer completion(INTDMAATC9) 100: DMAC ch16 transfer completion(INTDMAATC16) 101: DMAC ch17 transfer completion(INTDMAATC17) 110: DMAC ch22 transfer completion(INTDMAATC22) 111: Reserved
19	-	0	R	Read as 0
18	UPDN10	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL1	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN10	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as 0
14:12	INSEL9[2:0]	000	R/W	Select the input trigger (DMA ch27) 000: T32A ch3 DMA request capture B0(T32A03DMAREQCAPB0) 001: T32A ch3 DMA request capture B1(T32A03DMAREQCAPB1) 010: T32A ch4 DMA request capture B0(T32A04DMAREQCAPB0) 011: T32A ch4 DMA request capture B1(T32A04DMAREQCAPB1) 100: T32A ch5 DMA request capture B0(T32A05DMAREQCAPB0) 101: T32A ch5 DMA request capture B1(T32A05DMAREQCAPB1) 110: Reserved 111: Reserved
11	-	0	R	Read as 0
10	UPDN9	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection

Bit	Bit Symbol	After Reset	Type	Function
9	OUTSEL9	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN9	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as 0
6:4	INSEL8[2:0]	000	R/W	Select the input trigger (DMA ch26) 000: T32A ch0 DMA request capture B0(T32A00DMAREQCAPB0) 001: T32A ch0 DMA request capture B1(T32A00DMAREQCAPB1) 010: T32A ch1 DMA request capture B0(T32A01DMAREQCAPB0) 011: T32A ch1 DMA request capture B1(T32A01DMAREQCAPB1) 100: T32A ch2 DMA request capture B0(T32A00DMAREQCAPB0) 101: T32A ch2 DMA request capture B1(T32A01DMAREQCAPB1) 110: Reserved 111: Reserved
3	-	0	R	Read as 0
2	UPDN8	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL8	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN8	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.4.4. *[TSELxCR3]* (Control Register 3)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as 0
30:28	INSEL15[2:0]	000	R/W	Select the input trigger (TSPI ch0 trigger input) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: T32A ch5 Timer register A1 match trigger(T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved
27	-	0	R	Read as 0
26	UPDN15	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL15	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN15	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as 0
22:20	INSEL14[2:0]	000	R/W	Select the input trigger (ADC general purpose trigger) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved
19	-	0	R	Read as 0
18	UPDN14	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL14	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN14	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as 0
14:12	INSEL13[2:0]	000	R/W	Select the input trigger (DMA ch31) 000: DMAC ch6 transfer completion(INTDMAATC6) 001: DMAC ch7 transfer completion(INTDMAATC7) 010: DMAC ch14 transfer completion(INTDMAATC14) 011: DMAC ch15 transfer completion(INTDMAATC15) 100: DMAC ch21 transfer completion(INTDMAATC21) 101: DMAC ch25 transfer completion(INTDMAATC25) 110: DMAC ch27 transfer completion(INTDMAATC27) 111: PF2(TRGIN2)
11	-	0	R	Read as 0
10	UPDN13	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection

Bit	Bit Symbol	After Reset	Type	Function
9	OUTSEL13	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN13	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as 0
6:4	INSEL12[2:0]	000	R/W	Select the input trigger (DMA ch30) 000: DMAC ch4 transfer completion(INTDMAATC4) 001: DMAC ch5 transfer completion(INTDMAATC5) 010: DMAC ch12 transfer completion(INTDMAATC12) 011: DMAC ch13 transfer completion(INTDMAATC13) 100: DMAC ch20 transfer completion(INTDMAATC20) 101: DMAC ch24 transfer completion(INTDMAATC24) 110: DMAC ch26 transfer completion(INTDMAATC26) 111: PB1(TRGIN1)
3	-	0	R	Read as 0
2	UPDN12	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL12	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN12	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.4.5. *[TSELxCR4]* (Control Register 4)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as 0
30:28	INSEL19[2:0]	000	R/W	Select the input trigger (UART ch0 trigger input) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved
27	-	0	R	Read as 0
26	UPDN19	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL19	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN19	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as 0
22:20	INSEL18[2:0]	000	R/W	Select the input trigger (TSPI ch3 trigger input) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved
19	-	0	R	Read as 0
18	UPDN18	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL18	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN18	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as 0
14:12	INSEL17[2:0]	000	R/W	Select the input trigger (TSPI ch2 trigger input) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved
11	-	0	R	Read as 0
10	UPDN17	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection

Bit	Bit Symbol	After Reset	Type	Function
9	OUTSEL17	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN17	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as 0
6:4	INSEL16[2:0]	000	R/W	Select the input trigger (TSPI ch1 trigger input) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved
3	-	0	R	Read as 0
2	UPDN16	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL16	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN16	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.4.6. *[TSELxCR5]* (Control Register 5)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as 0
30:28	INSEL23[2:0]	000	R/W	Select the input trigger (T32A ch0 Timer A internal trigger input) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: UART ch0 transmission completion trigger (UART0TXTRG) 100: UART ch0 reception completion trigger (UART0RXTRG) 101: TSPI ch0 transmit completion (TSPI0TXEND) 110: TSPI ch0 receive completion (TSPI0RXEND) 111: Reserved
27	-	0	R	Read as 0
26	UPDN23	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL23	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN23	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as 0
22:20	INSEL22[2:0]	000	R/W	Select the input trigger (UART ch3 trigger input) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved
19	-	0	R	Read as 0
18	UPDN22	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL22	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN22	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as 0
14:12	INSEL21[2:0]	000	R/W	Select the input trigger (UART ch2 trigger input) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved
11	-	0	R	Read as 0
10	UPDN21	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection

Bit	Bit Symbol	After Reset	Type	Function
9	OUTSEL21	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN21	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as 0
6:4	INSEL20[2:0]	000	R/W	Select the input trigger (UART ch1 trigger input) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 100: T32A ch5 Timer register B1 match trigger (T32A05TRGOUTCMPB1) 101: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 110: Reserved 111: Reserved
3	-	0	R	Read as 0
2	UPDN20	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL20	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN20	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.4.7. *[TSELxCR6]* (Control Register 6)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as 0
30:28	INSEL27[2:0]	000	R/W	Select the input trigger (T32A ch1 Timer B internal trigger input) 000: T32A ch1 Timer register A0 match trigger(T32A01TRGOUTCMPA0) 001: T32A ch1 Timer register A1 match trigger(T32A01TRGOUTCMPA1) 010: T32A ch1 Timer A overflow trigger(T32A01TRGOUTOFA) 011: T32A ch1 Timer A underflow trigger(T32A01TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as 0
26	UPDN27	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL27	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN27	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as 0
22:20	INSEL26[2:0]	000	R/W	Select the input trigger (T32A ch1 Timer A internal trigger input) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: UART ch1 transmission completion trigger (UART1TXTRG) 100: UART ch1 reception completion trigger (UART1RXTRG) 101: TSPI ch1 transmit completion(TSPI1TXEND) 110: TSPI ch1 receive completion(TSPI1RXEND) 111: Reserved
19	-	0	R	Read as 0
18	UPDN26	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL26	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN26	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as 0
14:12	INSEL25[2:0]	000	R/W	Select the input trigger (T32A ch0 Timer C internal trigger input) 000: T32A ch5 Timer register C0 match trigger(T32A05TRGOUTCMPC0) 001: T32A ch5 Timer register C1 match trigger(T32A05TRGOUTCMPC1) 010: T32A ch5 Timer C overflow trigger(T32A05TRGOUTOFC) 011: T32A ch5 Timer C underflow trigger(T32A05TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	-	0	R	Read as 0
10	UPDN25	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection

Bit	Bit Symbol	After Reset	Type	Function
9	OUTSEL25	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN25	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as 0
6:4	INSEL24[2:0]	000	R/W	Select the input trigger (T32A ch0 Timer B internal trigger input) 000: T32A ch0 Timer register A0 match trigger(T32A00TRGOUTCMPA0) 001: T32A ch0 Timer register A1 match trigger(T32A00TRGOUTCMPA1) 010: T32A ch0 Timer A overflow trigger(T32A00TRGOUTOFA) 011: T32A ch0 Timer A underflow trigger(T32A00TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as 0
2	UPDN24	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL24	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN24	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.4.8. *[TSELxCR7]* (Control Register 7)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as 0
30:28	INSEL31[2:0]	000	R/W	Select the input trigger (T32A ch2 Timer C internal trigger input) 000: T32A ch1 Timer register C0 match trigger(T32A01TRGOUTCMPC0) 001: T32A ch1 Timer register C1 match trigger(T32A01TRGOUTCMPC1) 010: T32A ch1 Timer C overflow trigger(T32A01TRGOUTOFC) 011: T32A ch1 Timer C underflow trigger(T32A01TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as 0
26	UPDN31	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL31	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN31	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as 0
22:20	INSEL30[2:0]	000	R/W	Select the input trigger (T32A ch2 Timer B internal trigger input) 000: T32A ch2 Timer register A0 match trigger(T32A02TRGOUTCMPA0) 001: T32A ch2 Timer register A1 match trigger(T32A02TRGOUTCMPA1) 010: T32A ch2 Timer A overflow trigger(T32A02TRGOUTOFA) 011: T32A ch2 Timer A underflow trigger(T32A02TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as 0
18	UPDN30	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL30	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN30	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as 0
14:12	INSEL29[2:0]	000	R/W	Select the input trigger (T32A ch2 Timer A internal trigger input) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: UART ch2 transmission completion trigger (UART2TXTRG) 100: UART ch2 reception completion trigger (UART2RXTRG) 101: TSPI ch2 transmit completion(TSPI2TXEND) 110: TSPI ch2 receive completion(TSPI2RXEND) 111: Reserved
11	-	0	R	Read as 0
10	UPDN29	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection

Bit	Bit Symbol	After Reset	Type	Function
9	OUTSEL29	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN29	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as 0
6:4	INSEL28[2:0]	000	R/W	Select the input trigger (T32A ch1 Timer C internal trigger input) 000: T32A ch0 Timer register C0 match trigger (T32A00TRGOUTCMPC0) 001: T32A ch0 Timer register C1 match trigger (T32A00TRGOUTCMPC1) 010: T32A ch0 Timer C overflow trigger (T32A00TRGOUTOFC) 011: T32A ch0 Timer C underflow trigger (T32A00TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as 0
2	UPDN28	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL28	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN28	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.4.9. *[TSELxCR8]* (Control Register 8)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as 0
30:28	INSEL35[2:0]	000	R/W	Select the input trigger (T32A ch4 Timer A internal trigger input) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: A-ENC ch0 divided pulse signal (ENC0TIMPLS) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as 0
26	UPDN35	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL35	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN35	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as 0
22:20	INSEL34[2:0]	000	R/W	Select the input trigger (T32A ch3 Timer C internal trigger input) 000: T32A ch2 Timer register C0 match trigger(T32A02TRGOUTCMPC0) 001: T32A ch2 Timer register C1 match trigger(T32A02TRGOUTCMPC1) 010: T32A ch2 Timer C overflow trigger (T32A02TRGOUTOFC) 011: T32A ch2 Timer C underflow trigger (T32A02TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as 0
18	UPDN34	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL34	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN34	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as 0
14:12	INSEL33[2:0]	000	R/W	Select the input trigger (T32A ch3 Timer B internal trigger input) 000: T32A ch3 Timer register A0 match trigger (T32A03TRGOUTCMPA0) 001: T32A ch3 Timer register A1 match trigger (T32A03TRGOUTCMPA1) 010: T32A ch3 Timer A overflow trigger (T32A03TRGOUTOFA) 011: T32A ch3 Timer A underflow trigger (T32A03TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	-	0	R	Read as 0
10	UPDN33	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection

Bit	Bit Symbol	After Reset	Type	Function
9	OUTSEL33	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN33	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as 0
6:4	INSEL32[2:0]	000	R/W	Select the input trigger (T32A ch3 Timer A internal trigger input) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: UART ch3 transmission completion trigger (UART3TXTRG) 100: UART ch3 reception completion trigger (UART3RXTRG) 101: TSPI ch3 transmit completion (TSPI3TXEND) 110: TSPI ch3 receive completion (TSPI3RXEND) 111: I^2C ch0 I^2C interrupt (INTI2C0)
3	-	0	R	Read as 0
2	UPDN32	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL32	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN32	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.4.10. *[TSELxCR9]* (Control Register 9)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as 0
30:28	INSEL39[2:0]	000	R/W	Select the input trigger (T32A ch5 Timer B internal trigger input) 000: T32A ch5 Timer register A0 match trigger (T32A05TRGOUTCMPA0) 001: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 010: T32A ch5 Timer A overflow trigger (T32A05TRGOUTOFA) 011: T32A ch5 Timer A underflow trigger (T32A05TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as 0
26	UPDN39	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
25	OUTSEL39	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
24	EN39	0	R/W	Trigger output control 0: Disable 1: Enable
23	-	0	R	Read as 0
22:20	INSEL38[2:0]	000	R/W	Select the input trigger (T32A ch5 Timer A internal trigger input) 000: PF0 (TRGIN0) 001: PB1 (TRGIN1) 010: PF2 (TRGIN2) 011: ADC general purpose trigger interrupt (INTADATRG) 100: ADC single conversion interrupt (INTADASGL) 101: ADC continuous conversion interrupt (INTADACNT) 110: ADC monitor function 0 Interrupt (INTADACP0) 111: ADC monitor function 1 Interrupt (INTADACP1)
19	-	0	R	Read as 0
18	UPDN38	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
17	OUTSEL38	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
16	EN38	0	R/W	Trigger output control 0: Disable 1: Enable
15	-	0	R	Read as 0
14:12	INSEL37[2:0]	000	R/W	Select the input trigger (T32A ch4 Timer C internal trigger input) 000: T32A ch3 Timer register C0 match trigger (T32A03TRGOUTCMPC0) 001: T32A ch3 Timer register C1 match trigger (T32A03TRGOUTCMPC1) 010: T32A ch3 Timer C overflow trigger (T32A03TRGOUTOFC) 011: T32A ch3 Timer C underflow trigger (T32A03TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	-	0	R	Read as 0
10	UPDN37	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection

Bit	Bit Symbol	After Reset	Type	Function
9	OUTSEL37	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
8	EN37	0	R/W	Trigger output control 0: Disable 1: Enable
7	-	0	R	Read as 0
6:4	INSEL36[2:0]	000	R/W	Select the input trigger (T32A ch4 Timer B internal trigger input) 000: T32A ch4 Timer register A0 match trigger (T32A04TRGOUTCMPA0) 001: T32A ch4 Timer register A1 match trigger (T32A04TRGOUTCMPA1) 010: T32A ch4 Timer A overflow trigger (T32A04TRGOUTOFA) 011: T32A ch4 Timer A underflow trigger (T32A04TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as 0
2	UPDN36	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL36	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN36	0	R/W	Trigger output control 0: Disable 1: Enable

2.2.4.11. *[TSELxCR10]* (Control Register 10)

Bit	Bit Symbol	After Reset	Type	Function
31:7	-	0	R	Read as 0
6:4	INSEL40[2:0]	000	R/W	Select the input trigger (T32A ch5 Timer C internal trigger input) 000: T32A ch4 Timer register C0 match trigger (T32A04TRGOUTCMPC0) 001: T32A ch4 Timer register C1 match trigger (T32A04TRGOUTCMPC1) 010: T32A ch4 Timer C overflow trigger (T32A04TRGOUTOFC) 011: T32A ch4 Timer C underflow trigger (T32A04TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as 0
2	UPDN40	0	R/W	Edge detection 0: Rising edge detection 1: Falling edge detection
1	OUTSEL40	0	R/W	Select the output trigger 0: The edge detection is disable 1: The edge detection is enable
0	EN40	0	R/W	Trigger output control 0: Disable 1: Enable

2.3. Direct Memory Access Controller

2.3.1. Built-in unit

Following table shows the built-in unit of each product.

Table 2.7 DMAC built-in unit

Product Name	DMAC unit (✓: Available, - : N/A)
	Unit A
M4K4	✓
M4K2	✓
M4K1	✓
M4K0	✓

2.3.2. DMA Request Table

Following table shows the DMA request List.

The channel which has a register name in the trigger selector column of a table should choose the request used by a trigger selector.

"-" in the table does not have an applicable function.

Table 2.8 DMA Request Table (1/4)

ch No	Single transfer		Burst transfer		
		Signal name	Trigger selector		Signal name
0	TSPI ch0 reception	TSPI0RX_DMA	-	TSPI ch0 reception	TSPI0RX_DMA
1	TSPI ch0 transmission	TSPI0TX_DMA	-	TSPI ch0 transmission	TSPI0TX_DMA
2	TSPI ch1 reception	TSPI1RX_DMA	-	TSPI ch1 reception	TSPI1RX_DMA
3	TSPI ch1 transmission	TSPI1TX_DMA	-	TSPI ch1 transmission	TSPI1TX_DMA
4	TSPI ch2 reception	TSPI2RX_DMA	-	TSPI ch2 reception	TSPI2RX_DMA
5	TSPI ch2 transmission	TSPI2TX_DMA	-	TSPI ch2 transmission	TSPI2TX_DMA
6	TSPI ch3 reception	TSPI3RX_DMA	-	TSPI ch3 reception	TSPI3RX_DMA
7	TSPI ch3 transmission	TSPI3TX_DMA	-	TSPI ch3 transmission	TSPI3TX_DMA
8	UART ch0 reception	UART0RX_DMAREQ	-	UART ch0 reception	UART0RX_DMAREQ
9	UART ch0 transmission	UART0TX_DMAREQ	-	UART ch0 transmission	UART0TX_DMAREQ
10	UART ch1 reception	UART1RX_DMAREQ	-	UART ch1 reception	UART1RX_DMAREQ
11	UART ch1 transmission	UART1TX_DMAREQ	-	UART ch1 transmission	UART1TX_DMAREQ
12	UART ch2 reception	UART2RX_DMAREQ	-	UART ch2 reception	UART2RX_DMAREQ
13	UART ch2 transmission	UART2TX_DMAREQ	-	UART ch2 transmission	UART2TX_DMAREQ
14	UART ch3 reception	UART3RX_DMAREQ	-	UART ch3 reception	UART3RX_DMAREQ
15	UART ch3 transmission	UART3TX_DMAREQ	-	UART ch3 transmission	UART3TX_DMAREQ
16	-	-		I^2C ch0 reception	I2C0RXDMAREQ

Note: The ch18 to 31 is set by trigger source of DMA request. For the detail of connection, refer to the "2.2 Trigger Selector".

Table 2.9 DMA request table (2/4)

ch No	Single transfer		Burst transfer		
		Signal name	Trigger selector		Signal name
17	-	-		I^2C ch0 transmission	I2C0TXDMAREQ
18	-	-	***[TSEL0CR0]*** <INSEL0>	AD general purpose trigger	ADATRG_DMAREQ
				AD single conversion	ADASLG_DMAREQ
				AD continue conversion	ADACNT_DMAREQ
19	-	-	***[TSEL0CR0]*** <INSEL1>	T32A ch0 compare A1 matched	T32A00DMAREQCMPA1
				T32A ch0 compare C1 matched	T32A00DMAREQCMPC1
				T32A ch1 compare A1 matched	T32A01DMAREQCMPA1
				T32A ch1 compare C1 matched	T32A01DMAREQCMPC1
				A-PMD ch0 PWM interrupt	INTPWM0
20	-	-	***[TSEL0CR0]*** <INSEL2>	T32A ch2 compare A1 matched	T32A02DMAREQCMPA1
				T32A ch2 compare C1 matched	T32A02DMAREQCMPC1
				T32A ch3 compare A1 matched	T32A03DMAREQCMPA1
				T32A ch3 compare C1 matched	T32A03DMAREQCMPC1
				A-PMD ch1 PWM interrupt	INTPWM1
21	-	-	***[TSEL0CR0]*** <INSEL3>	T32A ch4 compare A1 matched	T32A04DMAREQCMPA1
				T32A ch4 compare C1 matched	T32A04DMAREQCMPC1
				T32A ch5 compare A1 matched	T32A05DMAREQCMPA1
				T32A ch5 compare C1 matched	T32A05DMAREQCMPC1
22	-	-	***[TSEL0CR1]*** <INSEL4>	T32A ch0 capture B1	T32A00DMAREQCAPB1
				T32A ch1 capture B1	T32A00DMAREQCAPB1
				T32A ch2 capture B1	T32A01DMAREQCAPB1
				T32A ch3 capture B1	T32A01DMAREQCAPB1
				T32A ch4 capture B1	T32A00DMAREQCAPB1
				T32A ch5 capture B1	T32A00DMAREQCAPB1
23	-	-	***[TSEL0CR1]*** <INSEL5>	T32A ch0 capture A0	T32A00DMAREQCAPA0
				T32A ch0 capture A1	T32A00DMAREQCAPA1
				T32A ch1 capture A0	T32A01DMAREQCAPA0
				T32A ch1 capture A1	T32A01DMAREQCAPA1
				T32A ch0 capture C0	T32A00DMAREQCAPC0
				T32A ch0 capture C1	T32A00DMAREQCAPC1
				T32A ch1 capture C0	T32A01DMAREQCAPC0
				T32A ch1 capture C1	T32A01DMAREQCAPC1
24	-	-	***[TSEL0CR1]*** <INSEL6>	T32A ch2 capture A0	T32A02DMAREQCAPA0
				T32A ch2 capture A1	T32A02DMAREQCAPA1
				T32A ch3 capture A0	T32A03DMAREQCAPA0
				T32A ch3 capture A1	T32A03DMAREQCAPA1
				T32A ch2 capture C0	T32A02DMAREQCAPC0
				T32A ch2 capture C1	T32A02DMAREQCAPC1
				T32A ch3 capture C0	T32A03DMAREQCAPC0
				T32A ch3 capture C1	T32A03DMAREQCAPC1

Note: The ch18 to 31 is set by trigger source of DMA request. For the detail of connection, refer to the "2.2 Trigger Selector"

Table 2.10 DMA request table (3/4)

ch No	Single transfer		Burst transfer		
		Signal name	Trigger selector		Signal name
25	-	-	***[TSEL0CR1]*** <INSEL7>	T32A ch4 capture A0	T32A04DMAREQCAPA0
				T32A ch4 capture A1	T32A04DMAREQCAPA1
				T32A ch5 capture A0	T32A05DMAREQCAPA0
				T32A ch5 capture A1	T32A05DMAREQCAPA1
				T32A ch4 capture C0	T32A04DMAREQCAPC0
				T32A ch4 capture C1	T32A04DMAREQCAPC1
				T32A ch5 capture C0	T32A05DMAREQCAPC0
				T32A ch5 capture C1	T32A05DMAREQCAPC1
26	-	-	***[TSEL0CR2]*** <INSEL8>	T32A ch0 capture B0	T32A00DMAREQCAPB0
				T32A ch0 capture B1	T32A00DMAREQCAPB1
				T32A ch1 capture B0	T32A01DMAREQCAPB0
				T32A ch1 capture B1	T32A01DMAREQCAPB1
				T32A ch2 capture B0	T32A02DMAREQCAPB0
				T32A ch2 capture B1	T32A02DMAREQCAPB1
27	-	-	***[TSEL0CR2]*** <INSEL9>	T32A ch3 capture B0	T32A03DMAREQCAPB0
				T32A ch3 capture B1	T32A03DMAREQCAPB1
				T32A ch4 capture B0	T32A04DMAREQCAPB0
				T32A ch4 capture B1	T32A04DMAREQCAPB1
				T32A ch5 capture B0	T32A05DMAREQCAPB0
				T32A ch5 capture B1	T32A05DMAREQCAPB1
28	-	-	***[TSEL0CR2]*** <INSEL10>	DMAC ch0 transfer completion	INTDMAATC0
				DMAC ch1 transfer completion	INTDMAATC1
				DMAC ch8 transfer completion	INTDMAATC8
				DMAC ch9 transfer completion	INTDMAATC9
				DMAC ch16 transfer completion	INTDMAATC16
				DMAC ch17 transfer completion	INTDMAATC17
				DMAC ch22 transfer completion	INTDMAATC22
29	-	-	***[TSEL0CR2]*** <INSEL11>	DMAC ch2 transfer completion	INTDMAATC2
				DMAC ch3 transfer completion	INTDMAATC3
				DMAC ch10 transfer completion	INTDMAATC10
				DMAC ch11 transfer completion	INTDMAATC11
				DMAC ch18 transfer completion	INTDMAATC18
				DMAC ch19 transfer completion	INTDMAATC19
				DMAC ch23 transfer completion	INTDMAATC23
				TRGIN0(PF0)	TRGIN0

Note: The ch18 to 31 is set by trigger source of DMA request. For the detail of connection, refer to the "2.2 Trigger Selector"

Table 2.11 DMA request list (4/4)

ch no.	Single transfer		Burst transfer		
		Signal name	TRG selector		Signal name
30	-	-	*[TSEL0CR3]* <INSEL12>	DMAC ch4 transfer completion	INTDMAATC4
				DMAC ch5 transfer completion	INTDMAATC5
				DMAC ch12 transfer completion	INTDMAATC12
				DMAC ch13 transfer completion	INTDMAATC13
				DMAC ch20 transfer completion	INTDMAATC20
				DMAC ch24 transfer completion	INTDMAATC24
				DMAC ch26 transfer completion	INTDMAATC26
				TRGIN1(PB1)	TRGIN1
31	-	-	*[TSEL0CR3]* <INSEL13>	DMAC ch6 transfer completion	INTDMAATC6
				DMAC ch7 transfer completion	INTDMAATC7
				DMAC ch14 transfer completion	INTDMAATC14
				DMAC ch15 transfer completion	INTDMAATC15
				DMAC ch21 transfer completion	INTDMAATC21
				DMAC ch25 transfer completion	INTDMAATC25
				DMAC ch27 transfer completion	INTDMAATC27
				TRGIN2(PF2)	TRGIN2

Note: The ch18 to 31 is set by trigger source of DMA request. For the detail of connection, refer to the "2.2 Trigger Selector"

2.4. 32-bit Timer Event Counter(T32A)

2.4.1. Built-in channel

Following table shows the T32A built-in channel of each product.

Table 2.12 T32A built-in channel

Product	T32A channel (✓: Available, - : N/A)					
	ch0	ch1	ch2	ch3	ch4	ch5
M4K4	✓	✓	✓	✓	✓	✓
M4K2	✓	✓	✓	✓	✓	✓
M4K1	✓	✓	✓	✓	✓	✓
M4K0	✓	✓	✓	✓	✓	✓

2.4.2. Functional pins

The functional pins are assigned to the port of the following tables.
Please do not use simultaneously the same function currently assigned to two or more pins.
There is also a channel which does not have functional pins depending on a product.

Table 2.13 T32A functional pin and port (1/2)

Channel	Functional pin (Signal name)		Port	Ports for products (✓: Available, - : N/A)			
				M4K4	M4K2	M4K1	M4K0
ch0	T32A00INA0	Input	PK1	✓	✓	✓	✓
	T32A00INA1	Input	-	-	-	-	-
	T32A00OUTA	Output	PK0	✓	✓	✓	✓
	T32A00INB0	Input	-	-	-	-	-
	T32A00INB1	Input	-	-	-	-	-
	T32A00OUTB	Output	-	-	-	-	-
	T32A00INC0	Input	PK1	✓	✓	✓	✓
	T32A00INC1	Input	-	-	-	-	-
	T32A00OUTC	Output	PK0	✓	✓	✓	✓
ch1	T32A01INA0	Input	PA1	✓	✓	-	-
	T32A01INA1	Input	PA2	✓	-	-	-
	T32A01OUTA	Output	PA2	✓	-	-	-
	T32A01INB0	Input	PA0	✓	✓	✓	-
	T32A01INB1	Input	-	-	-	-	-
	T32A01OUTB	Output	PA0	✓	✓	✓	-
	T32A01INC0	Input	PA1	✓	✓	-	-
	T32A01INC1	Input	PA2	✓	-	-	-
	T32A01OUTC	Output	PA2	✓	-	-	-
ch2	T32A02INA0	Input	PG1	✓	✓	✓	✓
	T32A02INA1	Input	PG2	✓	✓	✓	✓
	T32A02OUTA	Output	PG0	✓	✓	✓	✓
	T32A02INB0	Input	-	-	-	-	-
	T32A02INB1	Input	-	-	-	-	-
	T32A02OUTB	Output	-	-	-	-	-
	T32A02INC0	Input	PG1	✓	✓	✓	✓
	T32A02INC1	Input	PG2	✓	✓	✓	✓
	T32A02OUTC	Output	PG0	✓	✓	✓	✓

Table 2.14 T32A functional pins and port (2/2)

Channel	Functional pin (Signal name)		Port	Ports for products (✓: Available, - : N/A)			
				M4K4	M4K2	M4K1	M4K0
ch3	T32A03INA0	Input	PC1	✓	-	-	-
	T32A03INA1	Input	PC2	✓	-	-	-
	T32A03OUTA	Output	PC0	✓	✓	✓	-
	T32A03INB0	Input	-	-	-	-	-
	T32A03INB1	Input	-	-	-	-	-
	T32A03OUTB	Output	-	-	-	-	-
	T32A03INC0	Input	PC1	✓	-	-	-
	T32A03INC1	Input	PC2	✓	-	-	-
	T32A03OUTC	Output	PC0	✓	✓	✓	-
ch4	T32A04INA0	Input	PF1	✓	-	-	-
	T32A04INA1	Input	PF2	✓	-	-	-
	T32A04OUTA	Output	PF0	✓	✓	✓	-
	T32A04INB0	Input	-	-	-	-	-
	T32A04INB1	Input	-	-	-	-	-
	T32A04OUTB	Output	-	-	-	-	-
	T32A04INC0	Input	PF1	✓	-	-	-
	T32A04INC1	Input	PF2	✓	-	-	-
	T32A04OUTC	Output	PF0	✓	✓	✓	-
ch5	T32A05INA0	Input	PB1	✓	✓	✓	-
	T32A05INA1	Input	-	-	-	-	-
	T32A05OUTA	Output	PB0	✓	✓	✓	-
	T32A05INB0	Input	-	-	-	-	-
	T32A05INB1	Input	-	-	-	-	-
	T32A05OUTB	Output	PB1	✓	✓	✓	-
	T32A05INC0	Input	PB1	✓	✓	✓	-
	T32A05INC1	Input	-	-	-	-	-
	T32A05OUTC	Output	PB0	✓	✓	✓	-

2.4.3. Clock for prescaler

The 32-bit timer event counter uses the clock of the following table as a prescaler clock.

Table 2.15 T32A clock for prescaler

Clock
ΦT0

2.4.4. Internal signal connection specification

2.4.4.1. Capture trigger signal connection

In the 32-bit timer event counter, capture trigger signal is connected to signals of the following table.
The input trigger signal which has a register name in the trigger selector column of the following table should choose the input trigger used by a trigger selector.

Table 2.16 T32A Capture trigger connection (1/3)

Channel		Input signal name of capture trigger	Trigger source		
	Timer		Trigger selector	Input trigger signal	Signal name
ch0	Timer A	T32A00TRGINAPHCK (Other timer output)	-	-	-
		T32A00TRGINAPCK (Internal trigger input)	***[TSEL0CR5]*** <INSEL23>	PF0(TRGIN0)	TRGIN0
				PB1(TRGIN1)	TRGIN1
				PF2(TRGIN2)	TRGIN2
				UART ch0 transmission completion trigger	UART0TXTRG
				UART ch0 reception completion trigger	UART0RXTRG
				TSPI ch0 transmit completion	TSPI0TXEND
				TSPI ch0 receive completion	TSPI0RXEND
	Timer B	T32A00TRGINBPHCK (Other timer output)	T32A ch0 timer A output		T32A00OUTA
		T32A00TRGINBPCK (other timer input)	***[TSEL0CR6]*** <INSEL24>	T32A ch0 timer register A0 match trigger	T32A00TRGOUTCMPA0
				T32A ch0 timer register A1 match trigger	T32A00TRGOUTCMPA1
				T32A ch0 timer A overflow trigger	T32A00TRGOUTOFA
				T32A ch0 timer A underflow trigger	T32A00TRGOUTUFA
	Timer C	T32A00TRGINCPHCK (Other timer output)	-	-	-
		T32A00TRGINCPCK (Internal trigger input)	***[TSEL0CR6]*** <INSEL25>	T32A ch5 timer register C0 match trigger	T32A05TRGOUTCMPC0
				T32A ch5 timer register C1 match trigger	T32A05TRGOUTCMPC1
				T32A ch5 timer C overflow trigger	T32A05TRGOUTOFC
				T32A ch5 timer C underflow trigger	T32A05TRGOUTUFC
ch1	Timer A	T32A01TRGINAPHCK (Other timer output)	-	-	-
		T32A01TRGINAPCK (Internal trigger input)	***[TSEL0CR6]*** <INSEL26>	PF0 (TRGIN0)	TRGIN0
				PB1 (TRGIN1)	TRGIN1
				PF2 (TRGIN2)	TRGIN2
				UART ch1 transmission completion trigger	UART1TXTRG
				UART ch1 reception completion trigger	UART1RXTRG
				TSPI ch1 transmit completion	TSPI1TXEND
				TSPI ch1 receive completion	TSPI1RXEND
	Timer B	T32A01TRGINBPHCK (Other timer output)	T32A ch1 timer A output		T32A01OUTA
		T32A01TRGINBPCK (Internal trigger input)	***[TSEL0CR6]*** <INSEL27>	T32A ch1 timer register A0 match trigger	T32A01TRGOUTCMPA0
				T32A ch1 timer register A1 match trigger	T32A01TRGOUTCMPA1
				T32A ch1 timer A overflow trigger	T32A01TRGOUTOFA
				T32A ch1 timer A underflow trigger	T32A01TRGOUTUFA
	Timer C	T32A01TRGINCPHCK (Other timer output)	-	-	-
		T32A00TRGINCPCK (Internal trigger input)	***[TSEL0CR7]*** <INSEL28>	T32A ch0 timer register C0 match trigger	T32A00TRGOUTCMPC0
				T32A ch0 timer register C1 match trigger	T32A00TRGOUTCMPC1
				T32A ch0 timer C overflow trigger	T32A00TRGOUTOFC
				T32A ch0 timer C underflow trigger	T32A00TRGOUTUFC

Note: ***[TSEL0CRn]***<INSELm> is set the internal trigger of trigger source by trigger selector. For the detail of connection, refer to the "2.2 Trigger Selector".

Table 2.17 T32A Capture trigger connection (2/3)

Channel		Input signal name of capture trigger	Trigger source		
	Timer		Trigger selector	Input trigger signal	Signal name
ch2	Timer A	T32A02TRGINAPHCK (Other timer output)	-	-	-
		T32A02TRGINAPCK (Internal trigger input)	***[TSEL0CR7]*** <INSEL29>	PF0 (TRGIN0)	TRGIN0
				PB1 (TRGIN1)	TRGIN1
				PF2 (TRGIN2)	TRGIN2
				UART ch2 transmission completion trigger	UART2TXTRG
				UART ch2 reception completion trigger	UART2RXTRG
				TSPI ch2 transmit completion	TSPI2TXEND
				TSPI ch2 receive completion	TSPI2RXEND
	Timer B	T32A02TRGINBPHCK (Other timer output)	T32A ch2 timer A output		T32A02OUTA
		T32A02TRGINBPCK (Internal trigger input)	***[TSEL0CR7]*** <INSEL30>	T32A ch2 timer register A0 match trigger	T32A02TRGOUTCMPA0
				T32A ch2 timer register A1 match trigger	T32A02TRGOUTCMPA1
				T32A ch2 timer A overflow trigger	T32A02TRGOUTOFA
				T32A ch2 timer A underflow trigger	T32A02TRGOUTUFA
	Timer C	T32A02TRGINCPHCK (Other timer output)	-	-	-
		T32A02TRGINCPCK (Internal trigger input)	***[TSEL0CR7]*** <INSEL31>	T32A ch1 timer register C0 match trigger	T32A01TRGOUTCMPC0
				T32A ch1 timer register C1 match trigger	T32A01TRGOUTCMPC1
				T32A ch1 timer C overflow trigger	T32A01TRGOUTOFC
				T32A ch1 timer C underflow trigger	T32A01TRGOUTUFC
ch3	Timer A	T32A03TRGINAPHCK (Other timer output)	-	-	-
		T32A03TRGINAPCK (Internal trigger input)	***[TSEL0CR8]*** <INSEL32>	PF0 (TRGIN0)	TRGIN0
				PB1 (TRGIN1)	TRGIN1
				PF2 (TRGIN2)	TRGIN2
				UART ch3 transmission completion trigger	UART3TXTRG
				UART ch3 reception completion trigger	UART3RXTRG
				TSPI ch3 transmit completion	TSPI3TXEND
				TSPI ch3 receive completion	TSPI3RXEND
				I^2C ch0 I^2C interrupt	INTI2C0
	Timer B	T32A03TRGINBPHCK (Other timer output)	T32A ch3 timer A output		T32A03OUTA
		T32A03TRGINBPCK (Internal trigger input)	***[TSEL0CR8]*** <INSEL33>	T32A ch3 timer register A0 match trigger	T32A03TRGOUTCMPA0
				T32A ch3 timer register A1 match trigger	T32A03TRGOUTCMPA1
				T32A ch3 timer A overflow trigger	T32A03TRGOUTOFA
				T32A ch3 timer A underflow trigger	T32A03TRGOUTUFA
	Timer C	T32A03TRGINCPHCK (Other timer output)	-	-	-
		T32A03TRGINCPCK (Internal trigger input)	***[TSEL0CR8]*** <INSEL34>	T32A ch2 timer register C0 match trigger	T32A02TRGOUTCMPC0
				T32A ch2 timer register C1 match trigger	T32A02TRGOUTCMPC1
				T32A ch2 timer C overflow trigger	T32A02TRGOUTOFC
				T32A ch2 timer C underflow trigger	T32A02TRGOUTUFC

Note: ***[TSEL0CRn]***<INSELm> is set the internal trigger of trigger source by trigger selector. For the detail of connection, refer to the "2.2 Trigger Selector".

Table 2.18 T32A Capture trigger connection (3/3)

Channel		Input signal name of capture trigger	Trigger source		
	Timer		Trigger selector	Input trigger signal	Signal name
ch4	Timer A	T32A04TRGINAPHCK (Other timer output)	-	-	-
		T32A04TRGINAPCK (Internal trigger input)	***[TSEL0CR8]*** <INSEL35>	PF0 (TRGIN0)	TRGIN0
				PB1 (TRGIN1)	TRGIN1
				PF2 (TRGIN2)	TRGIN2
				A-ENC divided plus signal	ENC0TIMPLS
	Timer B	T32A04TRGINBPHCK (Other timer output)	T32A ch4 timer A output		T32A04OUTA
		T32A04TRGINBPCK (Internal trigger input)	***[TSEL0CR9]*** <INSEL36>	T32A ch4 timer register A0 match trigger	T32A04TRGOUTCMPA0
				T32A ch4 timer register A1 match trigger	T32A04TRGOUTCMPA1
				T32A ch4 timer A overflow trigger	T32A04TRGOUTOFA
				T32A ch4 timer A underflow trigger	T32A04TRGOUTUFA
	Timer C	T32A04TRGINCPHCK (Other timer output)	-	-	-
		T32A04TRGINCPCK (Internal trigger input)	***[TSEL0CR9]*** <INSEL37>	T32A ch3 timer register C0 match trigger	T32A03TRGOUTCMPC0
				T32A ch3 timer register C1 match trigger	T32A03TRGOUTCMPC1
				T32A ch3 timer C overflow trigger	T32A03TRGOUTOFC
				T32A ch3 timer C underflow trigger	T32A03TRGOUTUFC
ch5	Timer A	T32A05TRGINAPHCK (Other timer output)	-	-	-
		T32A05TRGINAPCK (Internal trigger input)	***[TSEL0CR9]*** <INSEL38>	PF0 (TRGIN0)	TRGIN0
				PB1 (TRGIN1)	TRGIN1
				PF2 (TRGIN2)	TRGIN2
				ADC general purpose trigger interrupt	INTADATRG
				ADC single conversion interrupt	INTADASGL
				ADC continuous conversion interrupt	INTADACNT
				ADC monitor function 0 interrupt	INTADACP0
				ADC monitor function 1 interrupt	INTADACP1
	Timer B	T32A05TRGINBPHCK (Other timer output)	T32A ch5 timer A output		T32A05OUTA
		T32A05TRGINBPCK (Internal trigger input)	***[TSEL0CR9]*** <INSEL39>	T32A ch5 timer register A0 match trigger	T32A05TRGOUTCMPA0
				T32A ch5 timer register A1 match trigger	T32A05TRGOUTCMPA1
				T32A ch5 timer A overflow trigger	T32A05TRGOUTOFA
				T32A ch5 timer A underflow trigger	T32A05TRGOUTUFA
	Timer C	T32A05TRGINCPHCK (Other timer output)	-	-	-
		T32A05TRGINCPCK (Internal trigger input)	***[TSEL0CR10]*** <INSEL40>	T32A ch4 timer register C0 match trigger	T32A04TRGOUTCMPC0
				T32A ch4 timer register C1 match trigger	T32A04TRGOUTCMPC1
				T32A ch4 timer C overflow trigger	T32A04TRGOUTOFC
				T32A ch4 timer C underflow trigger	T32A04TRGOUTUFC

Note: ***[TSEL0CRn]***<INSELm> is set the internal trigger of trigger source by trigger selector. For the detail of connection, refer to the "2.2 Trigger Selector".

2.4.4.2. Synchronous control connection

In the 32-bit timer event counter, as shown in the following tables, synchronous connection of the timer is carried out within the same channel.

Table 2.19 T32A Synchronous control connection specifications

Channel	Timer	Master		Timer	Slave	
		Function(output)	Signal name		Function(input)	Signal name
ch0	Timer A	Synchronous start output A	T32A00SYNCSTARTOUTA	Timer B	Synchronous start B	T32A00SYNCSTARTB
		Synchronous stop output A	T32A00SYNCSTOPOUTA		Synchronous stop B	T32A00SYNCSTOPB
		Synchronous Reload output A	T32A00SYNCRELOADOUTA		Synchronous Reload B	T32A00SYNCRELOADB
ch1	Timer A	Synchronous start output A	T32A01SYNCSTARTOUTA	Timer B	Synchronous start B	T32A01SYNCSTARTB
		Synchronous stop output A	T32A01SYNCSTOPOUTA		Synchronous stop B	T32A01SYNCSTOPB
		Synchronous Reload output A	T32A01SYNCRELOADOUTA		Synchronous Reload B	T32A01SYNCRELOADB
ch2	Timer A	Synchronous start output A	T32A02SYNCSTARTOUTA	Timer B	Synchronous start B	T32A02SYNCSTARTB
		Synchronous stop output A	T32A02SYNCSTOPOUTA		Synchronous stop B	T32A02SYNCSTOPB
		Synchronous Reload output A	T32A02SYNCRELOADOUTA		Synchronous Reload B	T32A02SYNCRELOADB
ch3	Timer A	Synchronous start output A	T32A03SYNCSTARTOUTA	Timer B	Synchronous start B	T32A03SYNCSTARTB
		Synchronous stop output A	T32A03SYNCSTOPOUTA		Synchronous stop B	T32A03SYNCSTOPB
		Synchronous Reload output A	T32A03SYNCRELOADOUTA		Synchronous Reload B	T32A03SYNCRELOADB
ch4	Timer A	Synchronous start output A	T32A04SYNCSTARTOUTA	Timer B	Synchronous start B	T32A04SYNCSTARTB
		Synchronous stop output A	T32A04SYNCSTOPOUTA		Synchronous stop B	T32A04SYNCSTOPB
		Synchronous Reload output A	T32A04SYNCRELOADOUTA		Synchronous Reload B	T32A04SYNCRELOADB
ch5	Timer A	Synchronous start output A	T32A05SYNCSTARTOUTA	Timer B	Synchronous start B	T32A05SYNCSTARTB
		Synchronous stop output A	T32A05SYNCSTOPOUTA		Synchronous stop B	T32A05SYNCSTOPB
		Synchronous Reload output A	T32A05SYNCRELOADOUTA		Synchronous Reload B	T32A05SYNCRELOADB

2.4.5. Pulse Counter List for each product

In the 32-bit timer event counter, as shown in the following tables, correspondence of a pulse counter changes with products.

Table 2.20 T32A Pulse counter list for each product

Channel	M4K4	M4K2	M4K1	M4K0
ch0	1-phase pulse count			
ch1	2-phase pulse count /1-phase pulse count	1-phase pulse count	-	
ch2	2-phase pulse count /1-phase pulse count			
ch3	2-phase pulse count /1-phase pulse count	-		
ch4	2-phase pulse count /1-phase pulse count	-		
ch5	1-phase pulse count			-

2.4.6. DMA request

In the 32-bit timer event counter, DMA request are shown in the following table.

What has the statement of a register name in the trigger selector column of a table should choose the request used by a trigger selector.

Table 2.21 T32A DMA request (1/2)

Channel	Request	Signal name	Trigger selector	DMA request channel		
					Single transfer	Burst transfer
ch0	DMA request at match A1 register	T32A00DMAREQCMPA1	*[TSEL0CR0]* <INSEL1>	19	-	✓
	DMA request at match C1 register	T32A00DMAREQCMPC1				
	DMA request at match B1 register	T32A00DMAREQCMPB1	*[TSEL0CR1]* <INSEL4>	22	-	✓
	DMA request at capture A0 register	T32A00DMAREQCAPA0	*[TSEL0CR1]* <INSEL5>	23	-	✓
	DMA request at capture A1 register	T32A00DMAREQCAPA1				
	DMA request at capture C0 register	T32A00DMAREQCAPC0				
	DMA request at capture C1 register	T32A00DMAREQCAPC1				
	DMA request at capture B0 register	T32A00DMAREQCAPB0	*[TSEL0CR2]* <INSEL8>	26	-	✓
	DMA request at capture B1 register	T32A00DMAREQCAPB1				
ch1	DMA request at match A1 register	T32A01DMAREQCMPA1	*[TSEL0CR0]* <INSEL1>	19	-	✓
	DMA request at match C1 register	T32A01DMAREQCMPC1				
	DMA request at match B1 register	T32A01DMAREQCMPB1	*[TSEL0CR1]* <INSEL4>	22	-	✓
	DMA request at capture A0 register	T32A01DMAREQCAPA0	*[TSEL0CR1]* <INSEL5>	23	-	✓
	DMA request at capture A1 register	T32A01DMAREQCAPA1				
	DMA request at capture C0 register	T32A01DMAREQCAPC0				
	DMA request at capture C1 register	T32A01DMAREQCAPC1				
	DMA request at capture B0 register	T32A01DMAREQCAPB0	*[TSEL0CR2]* <INSEL8>	26	-	✓
	DMA request at capture B1 register	T32A01DMAREQCAPB1				

Note: ✓: Available, - : N/A

Table 2.22 T32A DMA request (2/2)

Channel	Request	Signal name	Trigger selector	DMA request channel		
					Single transfer	Burst transfer
ch2	DMA request at match A1 register	T32A02DMAREQCMPA1	*[TSEL0CR0]* <INSEL2>	20	-	✓
	DMA request at match C1 register	T32A02DMAREQCMPC1				
	DMA request at match B1 register	T32A02DMAREQCMPB1	*[TSEL0CR1]* <INSEL4>	22	-	✓
	DMA request at capture A0 register	T32A02DMAREQCAPA0	*[TSEL0CR1]* <INSEL6>	24	-	✓
	DMA request at capture A1 register	T32A02DMAREQCAPA1				
	DMA request at capture C0 register	T32A02DMAREQCAPC0				
	DMA request at capture C1 register	T32A02DMAREQCAPC1				
	DMA request at capture B0 register	T32A02DMAREQCAPB0	*[TSEL0CR2]* <INSEL8>	26	-	✓
	DMA request at capture B1 register	T32A02DMAREQCAPB1				
ch3	DMA request at match A1 register	T32A03DMAREQCMPA1	*[TSEL0CR0]* <INSEL2>	20	-	✓
	DMA request at match C1 register	T32A03DMAREQCMPC1				
	DMA request at match B1 register	T32A03DMAREQCMPB1	*[TSEL0CR1]* <INSEL4>	22	-	✓
	DMA request at capture A0 register	T32A03DMAREQCAPA0	*[TSEL0CR1]* <INSEL6>	24	-	✓
	DMA request at capture A1 register	T32A03DMAREQCAPA1				
	DMA request at capture C0 register	T32A03DMAREQCAPC0				
	DMA request at capture C1 register	T32A03DMAREQCAPC1				
	DMA request at capture B0 register	T32A03DMAREQCAPB0	*[TSEL0CR2]* <INSEL9>	27	-	✓
	DMA request at capture B1 register	T32A03DMAREQCAPB1				
ch4	DMA request at match A1 register	T32A04DMAREQCMPA1	*[TSEL0CR0]* <INSEL3>	21	-	✓
	DMA request at match C1 register	T32A04DMAREQCMPC1				
	DMA request at match B1 register	T32A04DMAREQCMPB1	*[TSEL0CR1]* <INSEL4>	22	-	✓
	DMA request at capture A0 register	T32A04DMAREQCAPA0	*[TSEL0CR2]* <INSEL7>	25	-	✓
	DMA request at capture A1 register	T32A04DMAREQCAPA1				
	DMA request at capture C0 register	T32A04DMAREQCAPC0				
	DMA request at capture C1 register	T32A04DMAREQCAPC1				
	DMA request at capture B0 register	T32A04DMAREQCAPB0	*[TSEL0CR2]* <INSEL9>	27	-	✓
	DMA request at capture B1 register	T32A04DMAREQCAPB1				
ch5	DMA request at match A1 register	T32A05DMAREQCMPA1	*[TSEL0CR0]* <INSEL3>	21	-	✓
	DMA request at match C1 register	T32A05DMAREQCMPC1				
	DMA request at match B1 register	T32A05DMAREQCMPB1	*[TSEL0CR1]* <INSEL4>	22	-	✓
	DMA request at capture A0 register	T32A05DMAREQCAPA0	*[TSEL0CR2]* <INSEL7>	25	-	✓
	DMA request at capture A1 register	T32A05DMAREQCAPA1				
	DMA request at capture C0 register	T32A05DMAREQCAPC0				
	DMA request at capture C1 register	T32A05DMAREQCAPC1				
	DMA request at capture B0 register	T32A05DMAREQCAPB0	*[TSEL0CR2]* <INSEL9>	27	-	✓
	DMA request at capture B1 register	T32A05DMAREQCAPB1				

Note: ✓: Available, - : N/A

2.4.7. Internal signal connection specification

Every count interrupt (INTT32AxEVRYC) does not correspond in the TMPM4K Group(1).

2.5. Universal Asynchronous Receiver Transmitter Circuit(UART)

2.5.1. Built-in channel

Following table show the UART built-in channel of each product.
In TMPM4K Group(1), Maximum Communication speed of UART is 5 Mbps.

Table 2.23 UART built-in channel

Product	UART channel (✓: Available, - : N/A)			
	ch0	ch1	ch2	ch3
M4K4	✓	✓	✓	✓
M4K2	✓	✓	✓	-
M4K1	✓	-	✓	-
M4K0	✓	-	✓	-

2.5.2. Function pin and port

The functional pins are assigned to the port of the following tables.
Please do not use simultaneously the same function currently assigned to two or more pins.
There is also a channel which does not have functional pins depending on a product.

Table 2.24 UART functional pin and port

Channel	Function Pin (signal name)		Port	Products list(✓: Available, - : N/A)			
				M4K4	M4K2	M4K1	M4K0
ch0	UT0TXDA	Output	PK1	✓	✓	✓	✓
			PK3	✓	✓	✓	✓
			PK0	✓	✓	✓	✓
			PK2	✓	✓	✓	✓
	UT0RXD	Input	PK0	✓	✓	✓	✓
			PK2	✓	✓	✓	✓
			PK1	✓	✓	✓	✓
			PK3	✓	✓	✓	✓
ch1	UT1TXDA	Output	PA0	✓	✓	-	-
			PA1	✓	✓	-	-
	UT1RXD	Input	PA1	✓	✓	-	-
			PA0	✓	✓	-	-
ch2	UT2TXDA	Output	PG0	✓	✓	✓	✓
	UT2RXD	Input	PG1	✓	✓	✓	✓
ch3	UT3TXDA	Output	PC0	✓	-	-	-
			PC1	✓	-	-	-
	UT3RXD	Input	PC1	✓	-	-	-
			PC0	✓	-	-	-

2.5.3. Half Clock mode support

Half clock mode of the UART corresponds to 1-pin mode only.

2.5.4. Clock for Prescaler

The UART use the clock of the following table as a prescaler clock.

Table 2.25 UART Clock for prescaler

Clock
ΦT0

2.5.5. DMA request

The following table shows the DMA request in the UART.
"-" in the table does not have an applicable function.

Table 2.26 UART DMA request

Channel	Request	Signal Name	Trigger selector	DMA request channel		
					Single transfer	Burst transfer
ch0	UART ch0 reception	UART0RX_DMAREQ	-	8	✓	✓
	UART ch0 transmission	UART0TX_DMAREQ		9	✓	✓
ch1	UART ch1 reception	UART1RX_DMAREQ	-	10	✓	✓
	UART ch1 transmission	UART1TX_DMAREQ		11	✓	✓
ch2	UART ch2 reception	UART2RX_DMAREQ	-	12	✓	✓
	UART ch2 transfer	UART2TX_DMAREQ		13	✓	✓
ch3	UART ch3 reception	UART3RX_DMAREQ	-	14	✓	✓
	UART ch3 transmission	UART3TX_DMAREQ	-	15	✓	✓

Note: ✓: Available, - : N/A

2.5.6. Internal signal connection specification

2.5.6.1. Trigger transfer signal connection

Transfer function of the UART has a trigger signal control.
A trigger control signal is selected with the trigger source and use it as the following table.

Table 2.27 UART trigger transfer signal connection

Channel		Trigger source		
	Signal	Trigger selector	Input trigger signal	Signal name
ch0	UART0TRGIN	***[TSEL0CR4]*** <INSEL19>	PF0(TRGIN0)	TRGIN0
			PB1(TRGIN1)	TRGIN1
			PF2(TRGIN2)	TRGIN2
			T32A ch5 timer register A1 match trigger	T32A05TRGOUTCMPA1
			T32A ch5 timer register B1 match trigger	T32A05TRGOUTCMPB1
			T32A ch5 timer register C1 match trigger	T32A05TRGOUTCMPC1
ch1	UART1TRGIN	***[TSEL0CR5]*** <INSEL20>	PF0(TRGIN0)	TRGIN0
			PB1(TRGIN1)	TRGIN1
			PF2(TRGIN2)	TRGIN2
			T32A ch5 timer register A1 match trigger	T32A05TRGOUTCMPA1
			T32A ch5 timer register B1 match trigger	T32A05TRGOUTCMPB1
			T32A ch5 timer register C1 match trigger	T32A05TRGOUTCMPC1
ch2	UART2TRGIN	***[TSEL0CR5]*** <INSEL21>	PF0(TRGIN0)	TRGIN0
			PB1(TRGIN1)	TRGIN1
			PF2(TRGIN2)	TRGIN2
			T32A ch5 timer register A1 match trigger	T32A05TRGOUTCMPA1
			T32A ch5 timer register B1 match trigger	T32A05TRGOUTCMPB1
			T32A ch5 timer register C1 match trigger	T32A05TRGOUTCMPC1
ch3	UART3TRGIN	***[TSEL0CR5]*** <INSEL22>	PF0(TRGIN0)	TRGIN0
			PB1(TRGIN1)	TRGIN1
			PF2(TRGIN2)	TRGIN2
			T32A ch5 timer register A1 match trigger	T32A05TRGOUTCMPA1
			T32A ch5 timer register B1 match trigger	T32A05TRGOUTCMPB1
			T32A ch5 timer register C1 match trigger	T32A05TRGOUTCMPC1

Note: ***[TSEL0CRn]***<INSELm> is set the internal trigger of trigger source by trigger selector. For the detail of connection, refer to the "2.2 Trigger Selector".

2.5.6.2. T32A connection

In the UART, there is a signal connected with the peripheral function inside in addition to this as shown in the following table.

Table 2.28 UART inside connection list: output

Channel	Function output		Trigger selector	Output destination	
		Signal name			Signal name
ch0	UART ch0 transmission completion trigger output	UART0TXTRG	***[TSEL0CR5]*** <INSEL23>	T32A ch0 Timer A	T32A00TRGINAPCK
	UART ch0 reception completion trigger output	UART0RXTRG			
ch1	UART ch1 transmission completion trigger output	UART1TXTRG	***[TSEL0CR6]*** <INSEL26>	T32A ch1 Timer A	T32A01TRGINAPCK
	UART ch1 reception completion trigger output	UART1RXTRG			
ch2	UART ch2 transmission completion trigger output	UART2TXTRG	***[TSEL0CR7]*** <INSEL29>	T32A ch2 Timer A	T32A02TRGINAPCK
	UART ch2 reception completion trigger output	UART2RXTRG			
ch3	UART ch3 transmission completion trigger output	UART3TXTRG	***[TSEL0CR8]*** <INSEL32>	T32A ch3 Timer A	T32A03TRGINAPCK
	UART ch3 reception completion trigger output	UART3RXTRG			

2.6. Serial Peripheral Interface(TSPI)

2.6.1. Built-in channel

The following table shows the TSPI built-in channel of each product.
In TMPM4K Group(1), Maximum Communication speed of TSPI is 20 Mbps.

Table 2.29 TSPI built-in channel

Product	TSPI channel (✓: Available, - : N/A)			
	ch0	ch1	ch2	ch3
M4K4	✓	✓	✓	✓
M4K2	✓	-	✓	-
M4K1	✓	-	✓	-
M4K0	-	-	✓	-

2.6.2. Function pin and port

The functional pins are assigned to the port of the following tables.
Please do not use simultaneously the same function currently assigned to two or more pins.
There is also a channel which does not have functional pins depending on a product.

Table 2.30 TSPI function functional pin and port

Channel	function pin (signal name)		Port	Products list (✓: Available, - : N/A)			
				M4K4	M4K2	M4K1	M4K0
ch0	TSPI0SCK	I/O	PK4	✓	✓	✓	-
	TSPI0TXD	Output	PK3	✓	✓	✓	-
	TSPI0RXD	Input	PK2	✓	✓	✓	-
ch1	TSPI1SCK	I/O	PA2	✓	-	-	-
	TSPI1TXD	Output	PA0	✓	-	-	-
	TSPI1RXD	Input	PA1	✓	-	-	-
ch2	TSPI2SCK	I/O	PG2	✓	✓	✓	✓
	TSPI2TXD	Output	PG0	✓	✓	✓	✓
	TSPI2RXD	Input	PG1	✓	✓	✓	✓
ch3	TSPI3SCK	I/O	PC2	✓	-	-	-
	TSPI3TXD	Output	PC0	✓	-	-	-
	TSPI3RXD	Input	PC1	✓	-	-	-

Note: In TMPM4K Group(1), there is no TSPIxCS2 pin and TSPIxCS3 pin.

2.6.3. Transfer mode of each product

The transfer modes which can be used with the product as TSPI is shown in the following tables differ.

Table 2.31 TSPI mode list

Channel	Support Mode			
	M4K4	M4K2	M4K1	M4K0
ch0	SIO mode			-
ch1	SIO mode	-	-	-
ch2	SIO mode			
ch3	SIO mode	-	-	-

2.6.4. *[TSPIxCR2]*<RXDLY> set value

For the setting value of TSPI control register 2 (***[TSPIxCR2]***<RXDLY>), set the values in the following table.

Table 2.32 TSPI *[TSPIxCR2]*<RXDLY> set value

Register name	Value
[TSPIxCR2]<RXDLY>	1(fsys>40MHz)

2.6.5. Clock for Prescaler

The TSPI use the clock of the following table as a prescaler clock.

Table 2.33 TSPI clock for prescaler

Clock
ΦT0

2.6.6. Internal signal connection specification

2.6.6.1. Trigger Transfer signal connection

Transfer function of the TSPI has a trigger signal control.
A trigger control signal is selected with the trigger source and use it as the following table.

Table 2.34 TSPI trigger transfer

Channel		Trigger source		
	Signal name	Trigger selector	Input trigger signal	Signal name
ch0	TSPI0TRG (input)	***[TSEL0CR3]*** <INSEL15>	PF0(TRGIN0) (Note2)	TRGIN0
			PB1(TRGIN1) (Note2)	TRGIN1
			PF2(TRGIN2) (Note2)	TRGIN2
			T32A ch5 timer register A1 match trigger	T32A05TRGOUTCMPA1
			T32A ch5 timer register B1 match trigger	T32A05TRGOUTCMPB1
			T32A ch5 timer register C1 match trigger	T32A05TRGOUTCMPC1
ch1	TSPI1TRG (input)	***[TSEL0CR4]*** <INSEL16>	PF0(TRGIN0) (Note2)	TRGIN0
			PB1(TRGIN1) (Note2)	TRGIN1
			PF2(TRGIN2) (Note2)	TRGIN2
			T32A ch5 timer register A1 match trigger	T32A05TRGOUTCMPA1
			T32A ch5 timer register B1 match trigger	T32A05TRGOUTCMPB1
			T32A ch5 timer register C1 match trigger	T32A05TRGOUTCMPC1
ch2	TSPI2TRG (input)	***[TSEL0CR4]*** <INSEL17>	PF0(TRGIN0) (Note2)	TRGIN0
			PB1(TRGIN1) (Note2)	TRGIN1
			PF2(TRGIN2) (Note2)	TRGIN2
			T32A ch5 timer register A1 match trigger	T32A05TRGOUTCMPA1
			T32A ch5 timer register B1 match trigger	T32A05TRGOUTCMPB1
			T32A ch5 timer register C1 match trigger	T32A05TRGOUTCMPC1
ch3	TSPI3TRG (input)	***[TSEL0CR4]*** <INSEL18>	PF0(TRGIN0) (Note2)	TRGIN0
			PB1(TRGIN1) (Note2)	TRGIN1
			PF2(TRGIN2) (Note2)	TRGIN2
			T32A ch5 timer register A1 match trigger	T32A05TRGOUTCMPA1
			T32A ch5 timer register B1 match trigger	T32A05TRGOUTCMPB1
			T32A ch5 timer register C1 match trigger	T32A05TRGOUTCMPC1

Note1: ***[TSEL0CR3]***<INSELm>, ***[TSEL0CR4]***<INSELm> is set the trigger source by trigger selector. For the detail of connection, refer to the "2.2 Trigger Selector".

Note2: M4K2 and M4K1 do not have the PF2 pin, M4K0 does not have the PB1, PF0, PF2 pin.

2.6.6.2. T32A connection

In the TSPI, there is a signal connected with the peripheral function inside in addition to this as shown in the following table.

Table 2.35 TSPI inside connection (output)

Channel	Function output		Trigger selector	Output destination	
		Signal name			Signal name
ch0	TSPI ch0 transmission completion	TSPI0TXEND	*[TSEL0CR5]* <INSEL23>	T32A ch0 Timer A	T32A00TRGINAPCK
	TSPI ch0 reception completion	TSPI0RXEND			
ch1	TSPI ch1 transmission completion	TSPI1TXEND	*[TSEL0CR6]* <INSEL26>	T32A ch1 Timer A	T32A01TRGINAPCK
	TSPI ch1 reception completion	TSPI1RXEND			
ch2	TSPI ch2 transmission completion	TSPI2TXEND	*[TSEL0CR7]* <INSEL29>	T32A ch2 Timer A	T32A02TRGINAPCK
	TSPI ch2 reception completion	TSPI2RXEND			
ch3	TSPI ch3 transmission completion	TSPI3TXEND	*[TSEL0CR8]* <INSEL32>	T32A ch3 Timer A	T32A03TRGINAPCK
	TSPI ch3 reception completion	TSPI3RXEND			

2.6.7. DMA request

The following table shows the DMA request in the TSPI.
"-" in the table does not have an applicable function.

Table 2.36 TSPI DMA request

Channel	Request	Signal name	Trigger selector	DMA request channel		
					Single transfer	Burst transfer
ch0	TSPI ch0 reception	TSPI0RX_DMA	-	0	✓	✓
	TSPI ch0 transmission	TSPI0TX_DMA		1	✓	✓
ch1	TSPI ch1 reception	TSPI1RX_DMA	-	2	✓	✓
	TSPI ch1 transmission	TSPI1TX_DMA		3	✓	✓
ch2	TSPI ch2 reception	TSPI2RX_DMA	-	4	✓	✓
	TSPI ch2 transmission	TSPI2TX_DMA		5	✓	✓
ch3	TSPI ch3 reception	TSPI3RX_DMA	-	6	✓	✓
	TSPI ch3 transmission	TSPI3TX_DMA		7	✓	✓

Note: ✓: Available, - : N/A

2.7. I²C interface

2.7.1. Built-in channel

The following table show the I²C built-in channel of each product.
The I²C interface of TMPM4K Group(1) products supports "Standard Mode" and "Fast Mode".

Table 2.37 I²C interface built-in channel

Product	I²C channel (✓: Available, - : N/A)
	ch0
M4K4	✓
M4K2	✓
M4K1	✓
M4K0	-

2.7.2. Function pin and port

The functional pins are assigned to the port of the following tables.

Table 2.38 I²C interface function pin and port

Channel	Function pin(signal name)		Port	Product list (✓: Available, - : N/A)			
				M4K4	M4K2	M4K1	M4K0
ch0	I2C0SCL	I/O	PB1	✓	✓	✓	-
	I2C0SDA	I/O	PB0	✓	✓	✓	-

2.7.3. Clock for Prescaler

The I²C use the clock of the following table as a prescaler clock.

Table 2.39 I²C interface clock for prescaler

Clock
fsys

2.7.4. DMA request

The following table shows the DMA request in the I²C.
"-" in the table does not have an applicable function.

Table 2.40 I²C interface DMA request

Channel	Request	Signal name	Trigger selector	DMA request channel		
					Single transfer	Burst transfer
ch0	I²C ch0 reception	I2C0RXDMAREQ	-	16	-	✓
	I²C ch0 transmission	I2C0TXDMAREQ		17	-	✓

Note: ✓: Available, - : N/A

2.8. 12-bit Analog to Digital Converter(ADC)

2.8.1. Built-in unit

The following table shows the ADC built-in unit of each product.

Table 2.41 ADC built-in unit

Product	ADC unit (✓: Available, - : N/A)
	Unit A
M4K4	✓
M4K2	✓
M4K1	✓
M4K0	✓

2.8.2. Function pin and port

The functional pins are assigned to the port of the following tables.
There is also a channel which does not have functional pins depending on a product.

Table 2.42 ADC function pin and port

Input channel	Function pin (signal name)	Port	Product list (✓: Available, - : N/A)			
			M4K4	M4K2	M4K1	M4K0
ch0	AINA00	PD0	✓	✓	✓	✓
ch1	AINA01	PD1	✓	✓	✓	✓
ch2	-	-	-	-	-	-
ch3	AINA03	PD2	✓	✓	✓	✓
ch4	AINA04	PD3	✓	✓	✓	-
ch5	-	-	-	-	-	-
ch6	AINA06	PD4	✓	✓	✓	✓
ch7	AINA07	PD5	✓	✓	✓	-
ch8	-	-	-	-	-	-
ch9	AINA09	PD6	✓	✓	✓	✓
ch10	AINA10	PE0	✓	✓	✓	-
ch11	AINA11	PE1	✓	✓	✓	-
ch12	AINA12	PE2	✓	✓	-	-
ch13	AINA13	PE3	✓	-	-	-
ch14	AINA14	PE4	✓	-	-	-
ch15	AINA15(VREFH)	PE5	✓	✓	✓	✓
ch16	AVDD5(Note2)	-	✓	✓	✓	✓
ch17	VREFL(Note3)	-	✓	✓	✓	✓
ch18	Reference power	-	✓	✓	✓	✓

Note1: The Ch16 to 18 are connected to internal signal of MCU for self-check function.
Note2: VREFH is chosen as AINA15 and, in the case of VREFH<AVDD5, ch16 cannot be used.
Note3: The VREFL is connected to AVSS.

2.8.3. Conversion clock of ADC

The 12-bit ADC uses the clock of the following table as a conversion clock.

Table 2.43 Conversion clock of ADC

Clock
ADCLK

2.8.4. Startup trigger

The 12-bit ADC has an AD conversion function with the Trigger signal.

The input trigger signal which has the register name in the trigger group selector column of the following table should choose the input trigger used by the trigger selector.

"-" in the table does not have an applicable function.

Table 2.44 ADC Startup trigger

Connection (Signal name)	Startup trigger		
	Trigger selector	Input trigger signal	Signal name
PMD0TRG0	-	A-PMD ch0 trigger 0	PMD0TRG0
PMD0TRG1	-	A-PMD ch0 trigger 1	PMD0TRG1
PMD0TRG2	-	A-PMD ch0 trigger 2	PMD0TRG2
PMD0TRG3	-	A-PMD ch0 trigger 3	PMD0TRG3
PMD0TRG4	-	A-PMD ch0 trigger 4	PMD0TRG4
PMD0TRG5	-	A-PMD ch0 trigger 5	PMD0TRG5
PMD1TRG0	-	A-PMD ch1 trigger 0	PMD1TRG0
PMD1TRG1	-	A-PMD ch1 trigger 1	PMD1TRG1
PMD1TRG2	-	A-PMD ch1 trigger 2	PMD1TRG2
PMD1TRG3	-	A-PMD ch1 trigger 3	PMD1TRG3
PMD1TRG4	-	A-PMD ch1 trigger 4	PMD1TRG4
PMD1TRG5	-	A-PMD ch1 trigger 5	PMD1TRG5
ADATRGIN	***[TSEL0CR3]*** <INSEL14>	PF0(TRGIN0)	TRGIN0
		PB1(TRGIN1)	TRGIN1
		PF2(TRGIN2)	TRGIN2
		T32A ch5 timer register A1 match trigger	T32A05TRGOUTCMPA1
		T32A ch5 timer register B1 match trigger	T32A05TRGOUTCMPB1
		T32A ch5 timer register C1 match trigger	T32A05TRGOUTCMPC1

Note: ***[TSEL0CR3]***<INSEL14> is set the trigger source by trigger selector. For the detail of connection, refer to the "2.2 Trigger Selector".

2.8.5. DMA request

The following table shows the DMA request in the 12-bit ADC.

Table 2.45 ADC DMA request

Unit	Request	Signal name	Trigger selector	DMA request channel		
					Single transfer	Burst transfer
A	General purpose trigger DMA request	ADATRG_DMAREQ	*[TSEL0CR0]* <INSEL0>	18	-	✓
	Single conversion DMA request	ADASGL_DMAREQ			-	✓
	Continuous conversion DMA request	ADACNT_DMAREQ			-	✓

Note: ✓: Available, - : N/A

2.8.6. Other connection

In the 12-bit ADC, there is a signal connected with the peripheral function inside in addition to this as shown in the following table.

"-" in the table does not have an applicable function.

Table 2.46 ADC inside connection: output

Unit	Function output		Trigger selector	Output destination	
		Signal name			Signal name
A	General purpose trigger interrupt	INTADATRG	*[TSEL0CR9]* <INSEL38>	T32A ch5 Timer A	-
	Single conversion interrupt	INTADASGL			
	Continuous conversion interrupt	INTADACNT			
	Monitor function 0 interrupt	INTADACP0			
	Monitor function 1 interrupt	INTADACP1			
	Monitor function 0 output for PMD protect function	ADACP0L_N	-	A-PMD ch0	ADACMP0L_N
			-	A-PMD ch1	ADACMP0L_N
	Monitor function 1 output for PMD protect function	ADACP1L_N	-	A-PMD ch0	ADACMP1L_N
			-	A-PMD ch1	ADACMP1L_N
	PMD trigger interrupt A	INTADAPDA	-	A-PMD/ A-VE+	INTADAPDA
	PMD trigger interrupt B	INTADAPDB	-		INTADAPDB
	PMD trigger interrupt C	INTADAPDC	-		INTADAPDC
	PMD trigger interrupt D	INTADAPDD	-		INTADAPDD
	priority ADC interrupt	INTADAPFLG	-	A-PMD	INTADAPFLG
	AD conversion flag	ADABUSY	-		ADABUSY
	Conversion result store register	VADAREG0	-	A-VE+	VADAREG0
		VADAREG1	-		VADAREG1
		VADAREG2	-		VADAREG2
		VADAREG3	-		VADAREG3

2.9. Advanced Programmable Motor Control Circuit(A-PMD)

2.9.1. Built-in channel

The following table shows the A-PMD built-in channel of each product.

Table 2.47 A-PMD built-in channel

Product	A-PMD channel (✓: Available, - : N/A)	
	ch0	ch1
M4K4	✓	✓
M4K2	✓	✓
M4K1	✓	✓ (Note)
M4K0	✓	✓ (Note)

Note: This product cannot be used for 3 phase motor drive, but some pins are assigned.

2.9.2. Function pin and port

The functional pins are assigned to the port of the following tables.

Table 2.48 A-PMD function pin

Channel	Function pin		Signal name	Port	Product list (✓: Available, - : N/A)			
					M4K4	M4K2	M4K1	M4K0
ch0	XO0	Output	XO0	PJ1	✓	✓	✓	✓
	YO0	Output	YO0	PJ3	✓	✓	✓	✓
	ZO0	Output	ZO0	PJ5	✓	✓	✓	✓
	UO0	Output	UO0	PJ0	✓	✓	✓	✓
	VO0	Output	VO0	PJ2	✓	✓	✓	✓
	WO0	Output	WO0	PJ4	✓	✓	✓	✓
	EMG0	Input	EMG0	PD6	✓	✓	✓	✓
				PH2	✓	✓	✓	-
				PJ6	✓	✓	✓	✓
	OVV0	Input	OVV0	PJ7	✓	-	-	-
	Debug output	Output	PMD0DBG	PB0	✓	✓	✓	-
				PG0	✓	✓	✓	✓
				PJ0	✓	✓	✓	✓
ch1	XO1	Output	XO1	PG3	✓	✓	-	-
	YO1	Output	YO1	PG4	✓	✓	-	-
	ZO1	Output	ZO1	PG5	✓	✓	-	-
	UO1	Output	UO1	PG0	✓	✓	✓	✓
	VO1	Output	VO1	PG1	✓	✓	✓	✓
	WO1	Output	WO1	PG2	✓	✓	✓	✓
	EMG1	Input	EMG1	PF0	✓	✓	✓	-
	OVV1	Input	OVV1	-	-	-	-	-
	Debug output	Output	PMD1DBG	PB1	✓	✓	✓	-
				PG1	✓	✓	✓	✓
				PJ1	✓	✓	✓	✓

2.9.3. DMA request

The following table shows the DMA request in the A-PMD.

Table 2.49 A-PMD DMA request

Channel	Request	Signal name	Trigger selector	DMA request channel		
					Single transfer	Burst transfer
ch0	A-PMD ch0 PWM interrupt	INTPWM0	*[TSEL0CR0]* <INSEL1>	19	-	✓
ch1	A-PMD ch1 PWM interrupt	INTPWM1	*[TSEL0CR0]* <INSEL2>	20	-	✓

Note: ✓: Available, - : N/A

2.9.4. Internal signal connection specification

2.9.4.1. Other connection

In the A-PMD, there is a signal connected with the peripheral function inside in addition to this as shown in the following table.

Table 2.50 A-PMD inside connection list: input

Channel	Function input		Input source	
		Signal name		Signal name
ch0	ADC conversion completion interrupt A	INTADAPDA	ADC	INTADAPDA
	ADC conversion completion interrupt B	INTADAPDB		INTADAPDB
	ADC conversion completion interrupt C	INTADAPDC		INTADAPDC
	ADC conversion completion interrupt D	INTADAPDD		INTADAPDD
	ADC conversion priority interrupt	INTADAPFLG		INTADAPFLG
	ADC conversion signal	ADABUSY		ADABUSY
	ADC monitor function 0 (OVV detection)	ADACMP0L_N		ADACP0L_N
	ADC monitor function 1 (OVV detection)	ADACMP1L_N		ADACP1L_N
	Commutation trigger (A-ENC position detect synchronous)	INTENC00	A-ENC	INTENC00
	Commutation trigger (General purpose timer synchronous)	PMD0TMR	T32A ch0	T32A00TRGOUTCMPA0
	Commutation trigger (A-ENC MCMP completion synchronous)	ENC0CTRGO	A-ENC	ENC0CTRG0
	VE U-phase PWM duty	VE0CMPU	A-VE+	VE0CMPU
	VE V-phase PWM duty	VE0CMPV		VE0CMPV
	VE W-phase PWM duty	VE0CMPW		VE0CMPW
	VE Trigger comparison 0	VE0TRGCMP0		VE0TRGCMP0
	VE Trigger comparison 1	VE0TRGCMP1		VE0TRGCMP1
	VE Trigger output selection	VE0TRGSEL		VE0TRGSEL
	VE Conduction control / Output control	VE0OUTCR		VE0OUTCR
	VE EMG release	VE0EMGRS		VE0EMGRS
	VE Task transition signal	VE0TASKP		VE0DBGO
	VE interrupt	INTVCN0		INTVCN0
ch1	ADC conversion completion interrupt A	INTADAPDA	ADC	INTADAPDA
	ADC conversion completion interrupt B	INTADAPDB		INTADAPDB
	ADC conversion completion interrupt C	INTADAPDC		INTADAPDC
	ADC conversion completion interrupt D	INTADAPDD		INTADAPDD
	ADC conversion priority interrupt	INTADAPFLG		INTADAPFLG
	ADC conversion signal	ADABUSY		ADABUSY
	ADC monitor function 0 (OVV detection)	ADACMP0L_N		ADACP0L_N
	ADC monitor function 1 (OVV detection)	ADACMP1L_N		ADACP1L_N
	Commutation trigger (General purpose timer synchronous)	PMD1TMR	T32A ch2	T32A02TRGOUTCMPA0
	VE Task transition signal	VE0TASKP	A-VE+	VE0DBGO
	VE interrupt	INTVCN1		INTVCN0

Table 2.51 A-PMD inside connection list: output

Channel	Function output		Output destination	
		Signal name		Signal name
ch0	ADC synchronous trigger output 0	PMD0TRG0	ADC	PMD0TRG0
	ADC synchronous trigger output 1	PMD0TRG1		PMD0TRG1
	ADC synchronous trigger output 2	PMD0TRG2		PMD0TRG2
	ADC synchronous trigger output 3	PMD0TRG3		PMD0TRG3
	ADC synchronous trigger output 4	PMD0TRG4		PMD0TRG4
	ADC synchronous trigger output 5	PMD0TRG5		PMD0TRG5
	PWM signal for the encoder input	PMD0PWMON	A-ENC	ENC0PWMON
	PWM interrupt	INTPWM0	A-VE+	INTPWM0
ch1	ADC synchronous trigger output 0	PMD1TRG0	ADC	PMD1TRG0
	ADC synchronous trigger output 1	PMD1TRG1		PMD1TRG1
	ADC synchronous trigger output 2	PMD1TRG2		PMD1TRG2
	ADC synchronous trigger output 3	PMD1TRG3		PMD1TRG3
	ADC synchronous trigger output 4	PMD1TRG4		PMD1TRG4
	ADC synchronous trigger output 5	PMD1TRG5		PMD1TRG5

2.9.4.2. Inter-channel synchronous control connection

The PMD is synchronously connected between the channels as shown in the table below.

Table 2.52 PMD Inter-channel synchronous control connection

Master			Slave		
Channel	Function(output)	Signal name	Channel	Function(input)	Signal name
ch0	Synchronization output for PWM enable	PMD0SYNCMDENO	ch1	Synchronization input for PWM enable	PMD1SYNCMDENI
	Synchronization output for EMG protection	PMD0SYNCEMGO		Synchronization input for EMG protection	PMD1SYNCEMGI
	Synchronization output for OVV protection	PMD0SYNCOVVO		Synchronization input for OVV protection	PMD1SYNCOVVI

2.10. Advanced Vector Engine Plus(A-VE+)

2.10.1. Built-in channel

The following table shows the A-VE+ built-in channel of each product.

Table 2.53 A-VE+ built-in channel

Product	A-VE+ channel (✓: Available, - : N/A)
	ch0
M4K4	✓
M4K2	✓
M4K1	✓
M4K0	✓

2.10.2. Other connection

In the A-VE+, there is a signal connected with the peripheral function inside in addition to this as shown in the following table.

Table 2.54 A-VE+ Internal connection specification: Input

Channel	Function input		Input source	
		Signal name		Signal name
ch0	ADC conversion end interrupt A	INTADAPDA	ADC	INTADAPDA
	ADC conversion end interrupt B	INTADAPDB		INTADAPDB
	AD conversion result 0	VADAREG0		VADAREG0
	AD conversion result 1	VADAREG1		VADAREG1
	AD conversion result 2	VADAREG2		VADAREG2
	AD conversion result 3	VADAREG3		VADAREG3
	PWM interrupt	INTPWM0	A-PMD ch0	INTPWM0

Table 2.55 A-VE+ Internal connection specification: Output

Channel	Function output		Output destination	
		Signal name		Signal name
ch0	U-phase PWM duty	VE0CMPU	A-PMD ch0	VE0CMPU
	V-phase PWM duty	VE0CMPV		VE0CMPV
	W-phase PWM duty	VE0CMPW		VE0CMPW
	Trigger compare 0	VE0TRGCMP0		VE0TRGCMP0
	Trigger compare 1	VE0TRGCMP1		VE0TRGCMP1
	Synchronous trigger output selection	VE0TRGSEL		VE0TRGSEL
	Conduction control / Output control	VE0OUTCR		VE0OUTCR
	EMG release signal	VE0EMGRS		VE0EMGRS
	Task transition signal	VE0DBGO	A-PMD ch0	VETASKP
			A-PMD ch1	VETASKP

There is no difference of the A-VE+ in every product.

2.11. Advanced Encoder input circuit(A-ENC)

2.11.1. Built-in channel

The following table shows the A-ENC built-in channel of each product.

Table 2.56 A-ENC built-in channel

Product	A-ENC channel (✓: Available, - : N/A)
	ch0
M4K4	✓
M4K2	✓
M4K1	✓
M4K0	✓

2.11.2. Function Pin and Port

The functional pins are assigned to the port of the following tables.

Table 2.57 A-ENC function pin

Channel	Function		(Signal Name)	Port	Product list (✓: Available, - : N/A)			
					M4K4	M4K2	M4K1	M4K0
ch0	ENC0A	Input	ENC0A	PG0	✓	✓	✓	✓
	ENC0B	Input	ENC0B	PG1	✓	✓	✓	✓
	ENC0Z	Input	ENC0Z	PG2	✓	✓	✓	✓

2.11.3. Internal signal connection specification

2.11.3.1. T32A/A-PMD Connection

In the A-ENC, there is a signal connected with the peripheral function inside in addition to this as shown in the following table.

"-" in the table does not have an applicable function.

Table 2.58 A-ENC Internal connection specification: Input

Channel	Function Input		Input source	
		Signal		Signal Name
ch0	General purpose timer output signal	ENC0PSGI	T32A ch0 Timer output A	T32A00OUTA
	PWM signal for sampling	ENC0PWMON	A-PMD ch0 PWM signal	PMD0PWMON

Table 2.59 A-ENC Internal connection specification: Output

Channel	Function output		Trigger selector	Output destination	
		Signal			Signal name
ch0	Divided pulse signal	ENC0TIMPLS	***[TSEL0CR8]*** <INSEL35>	T32A ch4 Timer A Capture trigger input	T32A04TRGINAPHCK
	Commutation trigger	ENC0CTRGO	-	A-PMD ch0 commutation trigger (Electrical angle synchronous)	ENC0CTRGO
	Encoder input interrupt 0	INTENC00	-	A-PMD ch0 commutation trigger (ENC position detection synchronous)	INTENC00

2.12. Operational amplifier (OPAMP)

2.12.1. Built-in unit

The following table shows the OPAMP built-in unit of each product.

Table 2.60 OPAMP built-in unitl

Product	OPAMP unit (✓: Available, - : N/A)		
	A	B	C
M4K4	✓	✓	✓
M4K2	✓	✓	✓
M4K1	✓	✓	✓
M4K0	✓	-	-

2.12.2. Connected pin

The terminal of the AD converter which can connect OPAMP is as follows.

Table 2.61 OPAMP connected pin

OPAMP	ADC pin	Products (✓: Available, - : N/A)			
		M4K4	M4K2	M4K1	M4K0
AMPA	AINA00/ AINA01	✓	✓	✓	✓
AMPB	AINA03/ AINA04	✓	✓	✓	-
AMPC	AINA06/ AINA07	✓	✓	✓	-

2.12.3. Internal connection

The internal connection of OPAMP and an AD converter is as follows.

Table 2.62 OPAMP internal connection

ADC input pin	OPAMP input pin	OPAMP output pin	OPAMP output to ADC
AINA00	AINAM	AMPOUTA	AINA00
AINA01	AINAP		
AINA03	AINBM	AMPOUTB	AINA04
AINA04	AINBP		
AINA06	AINCM	AMPOUTC	AINA07
AINA07	AINCP		

2.13. Clock Selective Watchdog Timer(SIWDT)

2.13.1. Built-in channel

The following table shows the SIWDT built-in channel of each product.

Table 2.63 SIWDT built-in channel

Product	SIWDT channel (✓: Available, - : N/A)
M4K4	✓
M4K2	✓
M4K1	✓
M4K0	✓

2.13.2. Count Clock

The Clock Selective Watchdog Timer can select the clock to count.
The following table shows the selectable clock.

Table 2.64 SIWDT count clock

Clock	Signal	Selection
System clock	fsys	Selected by ***[SIWD0MOD]***<WDCLS>
Internal High speed oscillator1 clock	f_{IHOSC1}	
Internal High speed oscillator2 clock	f_{IHOSC2}	

2.13.3. Output control

To select the Internal High speed oscillator 2(f_{IHOSC2}), Rewriting of the internal High speed oscillator2 can be forbidden.

Table 2.65 SIWDT output control

Output control	Signal name	Remark
Protect signal of Internal High speed oscillator 2 control bit (***[CGOSCCR]***<IHOSC2EN>)	OSCPRO	Setting by ***[SIWD0OSCCR]***<OSCPRO>

2.14. CRC calculation circuit(CRC)

The following table shows the CRC built-in channel of each product.

Table 2.66 CRC built-in channel

Product	CRC built-in (✓: Available, - : N/A)
M4K4	✓
M4K2	✓
M4K1	✓
M4K0	✓

2.15. RAM Parity(RAMP)

2.15.1. Built-in channel

The following table shows the RAMP built-in channel of each product.

Table 2.67 RAMP built-in channel

Product	RAMP built-in (✓: Available, - : N/A)
M4K4	✓
M4K2	✓
M4K1	✓
M4K0	✓

2.15.2. Error detection block area

The following table shows the detection RAM block area of each product.

Table 2.68 RAM area and address of RAMP

Register name	RAM area address	Products (✓: Available, - : N/A)			
		M4K4	M4K2	M4K1	M4K0
[RPARST]<RPARFG2>	0x20002000-0x200047FF	✓	✓	✓	✓
[RPARST]<RPARFG1>	0x20001000-0x20001FFF	✓	✓	✓	✓
[RPARST]<RPARFG0>	0x20000000-0x20000FFF	✓	✓	✓	✓

2.16. Oscillation Frequency Detection circuit(OFD)

2.16.1. Support products

The OFD is supported by the following products.

Table 2.69 OFD support product

Product	OFD support (✓: Available, - : N/A)
M4K4	✓
M4K2	✓
M4K1	✓
M4K0	✓

2.16.2. Reference Clock

The Oscillation frequency detection circuit operates considering the clock of the following tables as a reference clock.

Table 2.70 OFD reference clock

Reference clock	Signal name	Divide value
Internal High speed oscillator 2	f_{IHOSC2}	256

2.16.3. Clock for detection

The Oscillation frequency detection circuit chooses the clock to monitor from the detection object clock of the following tables.

Table 2.71 OFD clock for detection

Clock for detection		Signal name
Input signal	External High speed oscillator clock	f_{EHOSC}
	Selected clock by the ***[CGOSCCR]***<OSCSEL> and ***[CGPLL0SEL]***<PLL0SEL> in CG(Clock control block)	fc

2.17. Debug interface

2.17.1. Debug interface List for each product

Table 2.72 Debug interface List

Debug function	Debug Pin (Signal name)	Port	support Pin list (✓: Available, - : N/A)			
			M4K4	M4K2	M4K1	M4K0
Serial wire	SWDIO	PK2	✓	✓	✓	✓
	SWCLK	PK3	✓	✓	✓	✓
	SWV	PK1	✓	✓	✓	✓
JTAG	TMS	PK2	✓	✓	✓	✓
	TCK	PK3	✓	✓	✓	✓
	TDO	PK1	✓	✓	✓	✓
	TDI	PK0	✓	✓	✓	✓
	TRST_N	PK4	✓	✓	✓	-
ETM trace	TRACECLK	PL4	✓	-	-	-
	TRACEDATA0	PL0	✓	-	-	-
	TRACEDATA1	PL1	✓	-	-	-
	TRACEDATA2	PL2	✓	-	-	-
	TRACEDATA3	PL3	✓	-	-	-

2.18. Non Break Debug Interface (NBDIF)

2.18.1. Correspondence table

The following table shows the NBDIF correspondence of each product.

Table 2.73 NBDIF correspondence table

Product	Function (✓: Available, - : N/A)
M4K4	✓
M4K2	-
M4K1	-
M4K0	-

2.18.2. NBDIF List for each product

Table 2.74 NBDIF interface List

Debug Pin (Signal name)	Port	Pin (✓: Available, - : N/A)			
		M4K4	M4K2	M4K1	M4K0
NBDSYNC	PK4	✓	-	-	-
NBDCLK	PL4	✓	-	-	-
NBDDATA0	PL0	✓	-	-	-
NBDDATA1	PL1	✓	-	-	-
NBDDATA2	PL2	✓	-	-	-
NBDDATA3	PL3	✓	-	-	-

2.19. Digital Noise Filter(DNF)

2.19.1. Built-in unit

The following table shows the DNF built-in unit of each product.

Table 2.75 DNF built-in unit

Product	DNF unit (✓: Available, - : N/A)
	A
M4K4	✓
M4K2	✓
M4K1	✓
M4K0	✓

2.19.2. External Interrupt list for the each product

The digital noise filter circuit corresponds to the following external interrupt pins.

Table 2.76 External interrupt and DNF

External interrupt pin (Signal name)	Port	Setting register name	DNF (✓: Available, - : N/A)			
			M4K4	M4K2	M4K1	M4K0
INT00a	PK0	***[DNFAENCR]***<NFEN0>	✓	✓	✓	✓
INT00b	PF1	***[DNFAENCR]***<NFEN11>	✓	-	-	-
INT01a	PK1	***[DNFAENCR]***<NFEN1>	✓	✓	✓	✓
INT01b	PF2	***[DNFAENCR***]<NFEN12>	✓	-	-	-
INT02a	PK2	***[DNFAENCR]***<NFEN2>	✓	✓	✓	✓
INT02b	PB0	***[DNFAENCR]***<NFEN13>	✓	✓	✓	-
INT03a	PK3	***[DNFAENCR]***<NFEN3>	✓	✓	✓	✓
INT03b	PB1	***[DNFAENCR]***<NFEN14>	✓	✓	✓	-
INT04	PG0	***[DNFAENCR]***<NFEN4>	✓	✓	✓	✓
INT05	PG1	***[DNFAENCR]***<NFEN5>	✓	✓	✓	✓
INT06	PK4	***[DNFAENCR]***<NFEN6>	✓	✓	✓	-
INT07a	PA0	***[DNFAENCR***]<NFEN7>	✓	✓	✓	-
INT07b	PC2	***[DNFAENCR]***<NFEN15>	✓	-	-	-
INT08	PC0	***[DNFAENCR]***<NFEN8>	✓	✓	✓	-
INT09	PA1	***[DNFAENCR]***<NFEN9>	✓	✓	-	-
INT10	PC1	***[DNFAENCR]***<NFEN10>	✓	-	-	-

2.19.3. Sampling source clock

The clock which shows a digital noise filter circuit in the following tables as a sauce clock of a sampling is used.

Table 2.77 DNF sampling source clock

Clock
fc

2.20. Trimming Circuit(TRM)

2.20.1. Support products

The TRM is supported by the following products.

Table 2.78 TRM support product

Product	TRM support (✓: Available, - : N/A)
M4K4	✓
M4K2	✓
M4K1	✓
M4K0	✓

2.20.2. Target oscillator

The target oscillator of the trimming circuit is the oscillator shown in the following tables.

Table 2.79 TRM trimming target oscillator

Target oscillator	Oscillator
Internal High speed oscillator	IHOSC1

2.21. Voltage Detection Circuit(LVD)

2.21.1. Support products

The LVD is supported by the following products.

Table 2.80 LVD support product

Product	LVD support (✓: Available, - : N/A)
M4K4	✓
M4K2	✓
M4K1	✓
M4K0	✓

2.21.2. Detection power supply

A voltage detecting circuit monitors the power supply of the following tables

Table 2.81 LVD detection power supply

Detection power supply	Power supply name
Digital power source	DVDD5

2.22. Flash Memory

2.22.1. Clock for the Programming/Erasing

As for flash memory, the clock of the following tables is used for programming/erasing of the code flash or the data flash.

Table 2.82 Clock for Programming/Erasing

Clock for Programming/Erasing
f_{IHOSC1}

2.22.2. The code flash block configuration of each product

The code flash memory differs in the block configuration of the memory with the product, as shown in the following table.

Table 2.83 The code flash of each product

Block name		M4K4FYAUG M4K4FYAFG M4K2FYADUG M4K1FYAUG	M4K4FWAUG M4K4FWAFG M4K2FWADUG M4K1FWAUG	M4K4FUAUG M4K4FUAFG M4K2FUADUG M4K1FUAUG	M4K4FSAUG M4K4FSAFG M4K2FSADUG M4K1FSAUG M4K0FSADUG	Block Size (KB)
Block0	PG0	✓	✓	✓	✓	4
	PG1	✓	✓	✓	✓	4
	PG2	✓	✓	✓	✓	4
	PG3	✓	✓	✓	✓	4
	PG4	✓	✓	✓	✓	4
	PG5	✓	✓	✓	✓	4
	PG6	✓	✓	✓	✓	4
	PG7	✓	✓	✓	✓	4
Block1		✓	✓	✓	✓	32
Block2		✓	✓	✓	-	32
Block3		✓	✓	-	-	32
Block4		✓	-	-	-	32
Block5		✓	-	-	-	32
Block6		✓	-	-	-	32
Block7		✓	-	-	-	32

Note: ✓: Available, -: N/A

2.22.3. Single boot resource

The peripheral function of the following table is used in single boot.

Table 2.84 Single boot resource

Peripheral function	Channel	Function	Pin Name
BOOT	-	-	PJ6 (BOOT_N)
UART	ch0	RXD	PK0(UT0RXD)
		TXD	PK1(UT0TXDA)
T32A	ch0	-	-

3. Revision History

Table 3.1 Revision History

Revision	Date	Description
1.0	2017-11-22	First release
2.0	2018-04-10	Revised (Revision No, Date, Copy Right) Revised Related documents table(added Exception & NBDIF, and IP Symbol) Revised Terms and Abbreviations(Op-Amp → OPAMP) Revised Table 2.5 (ch No of INSEL24) Revised Table 2.6 (ch No of INSEL40) Revised 2.2.4.3, 2.2.4.4 (INTDMAACTCx → INTDMAACTx) Change Style of Table 2.20 Revised signal name of Table 2.18(A-ENC divided signal) Sentence added about the Maximum communication speed of UART in 2.5.1 Sentence added about the Maximum communication speed of TSPI in 2.6.1 Paragraph added about the <RXDLY> set value on after 2.6.3 Sentence added about the supported Mode of I2C in 2.7.1 Deleted the section of "2.7.4. Filter selection". Revised the Function input and the signal name in Table 2.50(VE+ → VE, ch1:VE1TASKP → VE0TASKP) Paragraph added in 2.15(2.15.1 Built-in channel ,2.15.2 Error detection block area) Paragraph added in 2.16(2.16.1 Support products) Divide value added in Table 2.69. Paragraph added in 2.19(2.19.1 Built-in unit). Paragraph added in 2.20(2.20.1 Support products) Paragraph added in 2.21(2.21.1 Support products) Change section title of 2.22 (128KB → 256KB)
2.1	2018-09-18	- "Conventions" Revised SST registered trademarks - “Terms and Abbreviations” NBD I/F→NBDIF - "2.2.Trigger Selector" Figure 2.1: Change input trigger Table2.2 INSEL0: general-purpose trigger→ general purpose trigger DMA request program→ DMA request Table2.4 INSEL23, Table2.5 INSEL26,INSEL29, Table2.6 INSEL32 UART: completion→ completion trigger TSPI: transmission→transmit, reception → receive Table2.6 INSEL32 I^2C: interrupt→I^2C interrupt INSEL33: overflow A→Timer A overflow trigger underflow A→Timer A underflow trigger INSEL35: timer clock→ divided pulse signal, delete TIMPLS INSEL38: general-purpose trigger→ general purpose trigger interrupt program→ interrupt "2.2.4.1." to "2.2.4.11." Added connection destination to Function of INSELn "2.2.4.1." INSEL0: general-purpose trigger→ general purpose trigger DMA request program→ DMA request “2.2.4.6.” to “2.2.4.9.” INSEL23, INSEL26, INSEL29, INSEL32 UART: completion→ completion trigger TSPI: transmission→transmit, reception → receive "2.2.4.9." INSEL35: TIMPLS→ divided pulse signal INSEL34: overflow C→Timer C overflow trigger underflow C→Timer C underflow trigger INSEL33: overflow A→Timer A overflow trigger underflow A→Timer A underflow trigger INSEL32 I^2C: transmission & reception completion→I^2C interrupt "2.2.4.10." INSEL38: general-purpose trigger→ general purpose trigger interrupt program→ interrupt

		- "2.4. 32-bit Timer Event Counter" Table 2.16, Table 2.17, Table 2.19: Added T32A to the title. Table 2.16 ch0/Timer A, ch1/Timer A: UART: completion → completion trigger TSPI: transmission→ transmit, reception→ receive ch0, 1/Timer B, C: compare matched trigger→match trigger Table 2.17 ch2/Timer A: UART: completion → completion trigger TSPI: transmission→ transmit, reception→ receive ch2, 3/Timer B, C: compare matched trigger→match trigger ch3/Timer A: UART: completion → completion trigger TSPI: transmission→ transmit, reception→ receive I^2C: transmission & reception completion→ I^2C interrupt Table 2.18 ch4, 5/Timer B, C: compare matched trigger→match trigger ch5/Timer A: ADC: trigger→ trigger interrupt program→ interrupt monitor interrupt n → monitor function n interrupt Table 2.21,Table 2.22 Modified name of Request column - "2.5. Universal Asynchronous Receiver Transmitter Circuit" "2.5.6.1." Table 2.27: matched trigger→ match trigger "2.5.6.2." Table 2.28: Changed I/O column to Channel column. Deleted Peripheral function column. Output→Output destination - "2.6. Serial Peripheral Interface" "2.6.6.1." Table 2.34: matched trigger→ match trigger "2.6.6.2." Table 2.35: Changed I/O column to Channel column. Added signal name column. Output→Output destination - "2.8. 12-bit Analog to Digital Converter" "2.8.4." Table 2.44 ADATRGIN: matched trigger→ match trigger "2.8.5." Table 2.45: Changed Cannel column to Unit column. Modified name of Request column. "2.8.6." Table 2.46: Changed I/O column to Unit column. ADC general purpose trigger → General purpose trigger interrupt ADC single conversion program→ Single conversion interrupt ADC continuous conversion program →Continuous conversion interrupt ADC monitor interrupt n→ Monitor function n interrupt Monitor level output n→ Monitor function n output for PMD protect function Output→Output destination - "2.9. Advanced Programmable Motor Control Circuit" "2.9.4." Divided into "2.9.4.1." and "2.9.4.2.". Table 2.50 and Table 2.51: Deleted I/O column. Deleted rows of PMD synchronous signals. Table 2.50: Corrected Function input column. Table 2.51: Corrected Function output column. - "2.10. Advanced Vector Engine Plus" "2.10.2." Table 2.54, Table 2.55: Changed I/O column to Channel column. Table 2.54: Corrected Function input column. Table 2.55: Corrected Function output column. - "2.11. Advanced Encoder input circuit" Table 2.58, Table 2.59: Changed I/O column to Channel column. Combined peripheral function column and signal name column Table 2.58: Cycle signal input → General purpose timer output signal PWM ON signal input→PWM signal for sampling Table 2.59: Clock output of A-ENC Timer→Divided pulse signal Commutation trigger output→Commutation trigger - "2.12. Operational amplifier" Table 2.62: Added OPAMP to title. - "2.17 JTAG " deleted , Debug interface shifted, Table 2.72 changed. - "2.18. Non Break Debug Interface " added - "2.22. Flash Memory" : Change title. - "RESTRICTIONS ON PRODUCT USE" Revised

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